CAMAC Quad Ramp Controller
(CAMAC Module C473)

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General Description

The C473 is a programmable ramp controller capable of generating four semi-independent, time-based analog outputs. These outputs are updated at a 100 kHz rate.

The C473 also contains digital control capabilities to turn on, turn off, and reset four power supplies. It can also return eight status bits, a ramp enable bit, and a power supply enable bit from each of the regulator supplies.

Features

Output Functions

The ramp outputs will have the form:

output = scale_factor * f(t) + offset

where:

- scale_factor is a constant scale factor having a range of -128.0 to +127.9
- f(t) is an interpolated function of time which is initiated by a TCLK event. f(t) defines the overall shape of the output function
- offset is a constant offset having a range of -32768 to +32767

The output functions of all four channels share a common trigger. Each channel has an independent delay, programmable from 0 to 65535 μsec, between the TCLK trigger event and the start of the output functions.

Note: Although the shortest programmable delay is 0 μsec, at least 30 μsec must be allowed for the processor to service the trigger interrupt. The C473 will enforce a 30 μsec minimum delay.

Scale Factors

Scale factors are 16 bits long. The upper byte is interpreted as the whole number part and the lower byte is interpreted as the fractional part of the scale factor. Positive and negative scale factors are allowed. The largest negative scale factor is -128.000. The largest positive scale factor is approximately 127.996.

A separate scale factor is programmed for each interrupt level for each channel.

Changes to active scale factors are updated at the start of the next ramp.

Offsets

Offsets are 16 bits long. Positive and negative offsets are allowed. The largest negative offset is -32768. The largest positive offset is 32767.

A separate offset is programmed for each interrupt level for each channel.

Changes to active offsets are updated at the start of the next ramp.

Overflow Errors

The FPGA checks for overflow errors following each calculation and maintains the previously calculated value if an overflow is detected.

Sine Wave Mode (Amplitude Modulation)

The C473 can be configured to play a sine wave with ramping amplitude. The piecewise linear curve defined by f(t), scale factor, and offset becomes the amplitude of the sine wave. Additionally, a programmable frequency and phase are applied to the sine wave.

output = (scale_factor * f(t) + offset) * sin(2πfreq + phase)

Frequency is programmable from 0 Hz (0x0000) to 50 kHz (0x8000). Because the DAC output is updated at 100 kHz, larger values (0x8000 to 0xFFFF) will progressively fold back from 50 kHz to 0 Hz due to aliasing. In practice, the output frequency is limited by the slew rate of the output opamp to a few kHz, depending on the desired maximum amplitude of the sine wave.

Phase is programmable from -180° (0x8000 signed) to 179.99° (0x7FFF). When a ramp starts, the sine wave will discontinuously jump to the starting phase.

At the end of a ramp, the sine wave can be configured to free-run at the final amplitude or hold the last value sent to the DAC at a DC level.

Frequency and phase are programmed in the same way as scale factors and offsets. Tables of frequencies and phases are defined for each channel, and entries from these tables are mapped to interrupt levels.

Sweep Mode (Amplitude and Frequency Modulation)

The C473 can also be programmed to play a sine wave with a frequency sweep. This is done by ramping the sine wave's frequency as well as amplitude. The frequency ramp is generated by the next channel's ramp generator. For instance, to play a frequency sweep on Channel 0, we define a ramp (f(t), sf, and offset) on Channel 1 to vary the frequency.

Ch0 output = (scale_factor0 * f0(t) + offset0) * sin(2π[scale_factor1 * f1(t) + offset1] + phase0)

At the end of Channel 0's ramp, the sine wave can be configured to free-run at the final amplitude or hold the last value sent to the DAC at a DC level. If configured to free run, at the end of Channel 1's ramp, the sine wave will free run at the final frequency.

Any Channel N can be used to sweep the frequency of any Channel N-1. Channel 0 will sweep the frequency of Channel 3. The channel being used to sweep frequency will still put out a voltage waveform.

Ramp Output

The outputs are provided in analog format (16 bits, +/- 10.000V).

Bias Input

An analog input is supplied that will accept a +/- 5V input. The voltage is not monitored or processed by the C473's FPGA or firmware. This signal will be doubled and analog-added to each channel's ramp output.

ADC Monitoring

Each channel's final output (after adding the Bias Input) is constantly compared to a voltage feedback signal from that channel's power supply. This is accomplished by applying the final output and feedback input to the inputs of a differential instrumentation amplifier. The output of this amplifier is monitored by the FPGA through an ADC and compared to a programmable error threshold value.

Tables

The overall shape of the output function is defined by f(t). Each f(t) is programmed into a table in the C473 as a piecewise linear curve. Each channel will have seventeen possible tables with a maximum of 64 points each. Fifteen of the tables (1-15) are user-definable. The other (table 0) is defined as the "null" ramp. Each point consists of a ramp value V and a delta-t value. The delta-t value is in increments of 10 µsec (1/100 kHz). The last delta-t value of each table must be zero. At the end of each function, the final value will be held.

The null ramp is a flat line at 0. A non-zero offset can still be mapped by the interrupt level calling the null ramp. The scale factor mapped to this interrupt level is irrelevant, since zero times anything is still zero.

Table selection is effected by an interrupt. Thirty-two interrupt levels are available. Each is asserted by the 'or' of up to 8 programmed TCLK events. It is impossible to program one given TCLK event to trigger multiple interrupt levels at the same time. Attempts to program a given TCLK event to trigger a second interrupt level will not be processed and will generate an error. Interrupt levels can also be asserted via an F(17)A(10) CAMAC command. The complete list of TCLK events can be found in the TCLK Event Definitions document.

The FPGA constantly monitors the TCLK input. When a TCLK event is detected that is programmed to trigger an interrupt level, the FPGA will interrupt the processor and start a delay timer. The processor reads from the FPGA which interrupt level has begun, and downloads to the FPGA a scale factor, offset, and ramp table for each channel. At the end of the programmable delay, the FPGA will begin generating the output function.

Note: The FPGA will begin generating the output function after the delay, regardless of whether or not the processor has completed the parameter download. A very short delay may not allow the processor enough time to complete the download and may result in unexpected operation. **A minimum delay of 30 µsec is recommended.**

Tables are selected via pointers with values of 0 to 15 indicating ramp numbers 0 through 15.

Changes to an active table are implemented at the start of the next ramp. Changes to table pointers are updated at the start of the next ramp.

Initialized State

When the C473 is powered up or reset, all scale factors will be set to unity (0x0100) and all offsets, frequencies, and phases will be set to zero. All table pointers will be set to zero, and all table values will be set to zero. The clock event table will be filled with 0xFE, which is defined as the “Null Event”.

CAMAC Functions (Summary)

Fn/Addr	Description	Precede With…
F(0)A(0)	Read f(t) table data	F(16)A(12)
F(0)A(5)	Read ramp table map data	F(16)A(13)
F(0)A(7)	Read scale factor map data	F(16)A(13)
F(0)A(8)	Read scale factor data	F(16)A(13)
F(0)A(9)	Read TCLK trigger map data	F(16)A(11)
F(0)A(11)	Read active F(t) ramp table segment	F(19)A(1)
F(0)A(14)	Read Calculation Overflow Count	F(19)A(1)
F(1)A(2)	Read most recent DAC setting	F(19)A(1)
F(1)A(7)	Read power supply status nominal	F(19)A(1)
F(1)A(8)	Read power supply status mask	F(19)A(1)
F(1)A(9)	Read LAM mask	
F(1)A(11)	Read and clear power supply status error	F(19)A(1)
F(1)A(12)	Read and clear LAM source register	
F(1)A(13)	Read most recent CAMAC command	
F(1)A(14)	Read interrupt level TCLK trigger source	
F(1)A(15)	Read raw TCLK event count	
F(2)A(0)	Read TCLK interrupt level count	F(17)A(0)
F(2)A(2)	Read active F(t) ramp table	F(19)A(1)
F(2)A(3)	Read active scale factor	F(19)A(1)
F(2)A(4)	Read active offset	F(19)A(1)
F(2)A(9)	Read time remaining in current ramp segment	F(19)A(1)
F(3)A(11)	Read TCLK event error count	
F(3)A(14)	Read 1Hz interrupt count	
F(3)A(15)	Read CAMAC interrupt count	
F(4)A(1)	Read power supply status	F(19)A(1)
F(4)A(2)	Read current active interrupt level	
F(4)A(3)	Read power supply tracking tolerance	F(19)A(1)
F(4)A(6)	Read last invalid TCLK event received	
F(4)A(8)	Read most recent invalid CAMAC command	
F(4)A(10)	Read TCLK event mask data	F(20)A(11)
F(4)A(11)	Read TCLK event image data	F(20)A(11)
F(4)A(12)	Read, but do not clear, LAM source register	
F(4)A(15)	Read TCLK-triggered interrupt levels disabled flag	
F(5)A(0)	Read ADC	F(19)A(1)
F(6)A(0)	Read module ID number	
F(6)A(1)	Read firmware version number	
F(6)A(2)	Read a word in memory	F(16)A(14)
F(6)A(3)	Read a block of memory	F(16)A(14)
F(6)A(4)	Read diagnostic counter	F(19)A(2)
F(6)A(8)	Read FPGA version number	
F(6)A(9)	CAMAC Data Bus Diagnostic Read	F(20)A(12)
F(7)A(0)	Read offset map data	F(16)A(13)
F(7)A(1)	Read offset data	F(16)A(13)
F(7)A(3)	Read delay data	F(16)A(13)
F(7)A(4)	Read frequency map data	F(23)A(9)
F(7)A(5)	Read frequency data	F(23)A(9)
F(7)A(6)	Read phase map data	F(23)A(9)
F(7)A(7)	Read phase data	F(23)A(9)

Fn/Addr	Description	Precede With…
F(7)A(8)	Read sine wave mode	F(19)A(1)
F(7)A(9)	Read active sine wave frequency	F(19)A(1)
F(7)A(10)	Read active sine wave phase	F(19)A(1)
F(7)A(11)	Read final sine wave frequency	F(19)A(1)
F(7)A(12)	Read final sine wave phase	F(19)A(1)
F(8)A(0)	Read LAM status	
F(9)A(0)	Reset module	

Fn/Addr	Description	Precede With…
F(16)A(0)	Write f(t) table data	F(16)A(12)
F(16)A(5)	Write ramp table map data	F(16)A(13)
F(16)A(7)	Write scale factor map data	F(16)A(13)
F(16)A(8)	Write scale factor data	F(16)A(13)
F(16)A(9)	Write TCLK event data	F(16)A(11)
F(16)A(11)	Set up TCLK event table pointer	
F(16)A(12)	Set up pointer for ramp data read/write	
F(16)A(13)	Set up pointer for map, scale factor, offset, and delay read/write	
F(16)A(14)	Set up diagnostic memory pointer	
F(17)A(0)	Write TCLK Interrupt Level Counter Pointer	
F(17)A(2)	Write directly to DAC	F(19)A(1)
F(17)A(7)	Write power supply status nominal	F(19)A(1)
F(17)A(8)	Write power supply status mask	F(19)A(1)
F(17)A(9)	Write LAM Mask	
F(17)A(10)	Manual Interrupt Level Trigger	
F(19)A(1)	Write Channel Pointer	
F(19)A(2)	Select Diagnostic Counter	
F(20)A(3)	Write power supply tracking tolerance	F(19)A(1)
F(20)A(11)	Write generic clock event table diagnostic pointer	
F(20)A(12)	CAMAC Data Bus Diagnostic Write	
F(23)A(0)	Write offset map data	F(16)A(13)
F(23)A(1)	Write offset data	F(16)A(13)
F(23)A(3)	Write delay data	F(16)A(13)
F(23)A(4)	Read frequency map data	F(23)A(9)
F(23)A(5)	Read frequency data	F(23)A(9)
F(23)A(6)	Read phase map data	F(23)A(9)
F(23)A(7)	Read phase data	F(23)A(9)
F(23)A(8)	Enable/Disable sine wave mode	F(19)A(1)
F(23)A(9)	Set up pointer for frequency and phase read/write	
F(24)A(0)	Disable LAM	
F(24)A(2)	Disable Channel Waveform	F(19)A(1)
F(24)A(5)	Disable TCLK-Triggered Interrupt Levels	
F(24)A(6)	Turn off power supply	F(19)A(1)
F(25)A(0)	Decrement the DAC	F(19)A(1)
F(25)A(1)	Increment the DAC	F(19)A(1)
F(26)A(0)	Enable LAM	
F(26)A(2)	Enable Channel Waveform	F(19)A(1)
F(26)A(5)	Enable TCLK-Triggered Interrupt Levels	
F(26)A(6)	Turn on power supply	F(19)A(1)
F(26)A(8)	Reset power supply	F(19)A(1)
F(26)A(12)	Clear TCLK Event Table	
F(26)A(13)	Clear Diagnostic Counters	

CAMAC Functions (Detailed Description)

It should be noted that this section uses CAMAC notation when describing data bits. CAMAC data bits are R16:R1 for reads and W16:W1 for writes, with R16 and W16 being most significant. The most significant bytes are R16:R9 and W16:W9. The least significant bytes are R8:R1 and W8:W1.

F(0)A(0) – Read f(t) table data

F(t) data will be returned in f(t), delta-t order, starting at the point defined with a write to F(16)A(12). Data is read directly out of processor memory. The channel number, table number, and table entry number written to F(16)A(12) set the memory pointer as follows:

```
ptr = Channel * 16 * 64 * 2 +
            Table# * 64 * 2 +
            Table Entry * 2
```

The data pointer is auto-incremented with each successive call to F(0)A(0). When the end of one ramp is reached, successive reads will return data for the next ramp. When the end of one channel's ramps is reached, successive reads will return data for the next channel, starting with Table #1 (Table #0 is the null ramp and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be returned.

F(0)A(0)

Bits	Bit Definitions
R16:R1	F(t) table data

F(0)A(5) – Read ramp table map data

Ramp table map data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(0)A(5). When the end of one channel's ramp table map is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(0)A(5) indicates the number of the ramp profile that will be used when this interrupt level is triggered.

F(0)A(5)

Bits	Bit Definitions
R16:R5	Reserved
R4:R1	Ramp Profile Number (0-15)

F(0)A(7) – Read scale factor map data

Scale factor map data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(0)A(7). When the end of one channel's scale factor map data is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(0)A(7) is the entry in the scale factor table that will be used when this interrupt level is triggered.

F(0)A(7)

Bits	Bit Definitions
R16:R1	Scale factor map (0 - 31)

F(0)A(8) – Read scale factor data

Scale factor data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

The data pointer is auto-incremented with each successive call to F(0)A(8). When the end of one channel's scale factor data is reached, successive reads will return data for the next channel, starting with Scale Factor #1 (Scale Factor 0 is the "null" scale factor and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(0)A(8) is the scale factor that will be used when this entry of the scale factor table is selected (see F(0)A(7)). See the section on Scale Factors for an explanation of how scale factor data is interpreted.

F(0)A(8)

Bits	Bit Definitions
R16:R1	Scale factor (-128.0 – 127.9)

F(0)A(9) – Read TCLK trigger map data

TCLK event data will be returned, starting at the point defined with a write to F(16)A(11). Data is read directly out of processor memory. The TCLK event written to F(16)A(11) sets the memory pointer as follows:

```
ptr = Interrupt Level * 8 + TCLK Event Slot
```

The TCLK event table pointer is auto-incremented with each successive call to F(0)A(9). After data for the eighth TCLK event for interrupt level 31 is read (ptr = 127), the next call will read data for the first TCLK event for interrupt level 0 (ptr = 0).

F(0)A(9)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	TCLK Event

F(0)A(11) – Read active F(t) ramp table segment

The number of the active segment of the active F(t) ramp table for the channel selected by F(19)A(1) will be returned. The channel number is auto-incremented with each successive call to F(0)A(11). After Channel 3 is read, the next read will return data for Channel 0

F(0)A(11)

Bits	Bit Definitions
R16:R1	Active segment of active F(t) ramp table

F(0)A(14) – Read Calculation Overflow Count

The number of calculation overflow errors detected on the channel selected by F(19)A(1) will be returned. Note that because the outputs are updated at a 100kHz rate, this register can count up at a rather high rate. F(26)A(13) will reset this counter.

F(0)A(14)

Bits	Bit Definitions
R16:R1	Calculation overflow count

F(1)A(2) – Read most recent DAC setting

The most recent DAC setting will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(2). After Channel 3 is read, the next read will return data for Channel 0.

F(1)A(2)

Bits	Bit Definitions
R16:R1	DAC setting (-32768 – +32767)

F(1)A(7) – Read power supply status nominal

The nominal power supply status will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(7). After Channel 3 is read, the next read will return data for Channel 0.

This is the value "expected" to be returned by a read of power supply status.

F(1)A(7)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset (1 = Reset output active)
R13	Ramp Active
R12	Unused
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs (1 = Input Active)

F(1)A(8) – Read power supply status mask

The power supply status mask will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(8). After Channel 3 is read, the next read will return data for Channel 0.

A bit cleared in the status mask will suppress errors when the actual power supply status bit does not match the nominal status bit.

F(1)A(8)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset
R13	Ramp Active
R12	Unused
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs

F(1)A(9) – Read LAM mask

The CAMAC Look-At-Me (LAM) mask will be returned.

A bit cleared in the LAM mask will suppress LAM when the corresponding bit is set in the LAM Source.

F(1)A(9)

Bits	Bit Definitions
R16	CAMAC Command Error
R15	Calculation Error (Overflow)
R14	Unused
R13	TCLK Missing
R12	Unused
R11	Unused
R10	Power Supply Tracking Error
R9:R5	Unused
R4	Power Supply 3 Error
R3	Power Supply 2 Error
R2	Power Supply 1 Error
R1	Power Supply 0 Error

F(1)A(11) – Read and clear power supply status error

The power supply status error register will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(11). After Channel 3 is read, the next read will return data for Channel 0.

A bit set in the status error register indicates the value of that bit in the power supply status register(F(4)A(1)) did not match that bit in the power supply status nominal register(F(1)A(7)), and that bit was not cleared in the power supply status mask register(F(1)A(9)). Mismatches are latched into the error register.

Reading F(1)A(11) clears the power supply error register.

F(1)A(11)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset
R13	Ramp Active
R12	Unused
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs (1 = Input Active)

F(1)A(12) – Read and clear LAM source register

The CAMAC Look-At-Me (LAM) source register will be returned and cleared.

F(1)A(12)

Bits	Bit Definitions
R16	CAMAC Command Error
R15	Calculation Error (Overflow)
R14	Unused
R13	TCLK Missing
R12	Unused
R11	Unused
R10	Power Supply Tracking Error
R9:R5	Unused
R4	Power Supply 3 Error
R3	Power Supply 2 Error
R2	Power Supply 1 Error
R1	Power Supply 0 Error

F(1)A(13) – Read most recent CAMAC command

The most recent CAMAC command is returned.

F(1)A(13)

Bits	Bit Definitions
R16:R9	Function
R8:R1	Subaddress

F(1)A(14) – Read interrupt level TCLK trigger source

Returns which TCLK event triggered the current (or most recent) interrupt level. If $FE is returned, the interrupt level was triggered manually (with F(17)A(10)), or no interrupt levels have been triggered since reset.

F(1)A(14)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	Interrup level TCLK trigger source

F(1)A(15) – Read raw TCLK event count

Returns the number of raw TCLK events have been detected since reset.

F(1)A(15)

Bits	Bit Definitions
R16:R1	Raw TCLK Event Count

F(2)A(0) – Read TCLK interrupt level count

Returns the number of times a particular interrupt level has been triggered. First select a particular interrupt level with F(17)A(0).

F(2)A(0)

Bits	Bit Definitions
R16:R1	Interrupt Level Count

F(2)A(2) – Read active F(t) ramp table

The number of the active F(t) ramp table for the channel selected by F(19)A(1) will be returned. The channel number is auto-incremented with each successive call to F(2)A(2). After Channel 3 is read, the next read will return data for Channel 0

F(2)A(2)

Bits	Bit Definitions
R16:R1	Active F(t) ramp table

F(2)A(3) – Read active scale factor

The value of the active scale factor for the channel selected by F(19)A(1) will be returned. The channel number is auto-incremented with each successive call to F(2)A(2). After Channel 3 is read, the next read will return data for Channel 0

F(2)A(3)

Bits	Bit Definitions
R16:R1	Active scale factor

F(2)A(4) – Read active offset

The value of the active offset for the channel selected by F(19)A(1) will be returned. The channel number is auto-incremented with each successive call to F(2)A(2). After Channel 3 is read, the next read will return data for Channel 0

F(2)A(4)

Bits	Bit Definitions
R16:R1	Active offset

F(2)A(9) – Read time remaining in current ramp segment

The number of samples remaining in the current ramp segment is returned. First select a channel with F(19)A(1).

F(2)A(9)

Bits	Bit Definitions
R16:R1	Sample Count Remaining

F(3)A(11) – Read TCLK Error Count

This counter is incremented each time an interrupt level is erroneously triggered by an invalid TCLK event. F(26)A(13) will reset this counter.

F(3)A(11)

Bits	Bit Definitions
R16:R1	TCLK Error Count

F(3)A(14) – Read 1Hz interrupt count

A counter in the C473 increments once per second. Returns the number of 1Hz interrupts. F(26)A(13) will reset this counter.

F(3)A(14)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	Count

F(3)A(15) – Read CAMAC interrupt count

A counter in the C473 increments once every time the CAMAC service routine is entered. Returns the number of CAMAC interrupts.

F(3)A(15)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	Count

F(4)A(1) – Read power supply status

The power supply status will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(4)A(1). After Channel 3 is read, the next read will return data for Channel 0.

F(4)A(1)

Bits	Bit Definitions
R16	Unused
R15	Power Supply Tracking Error
R14	Power Supply Reset (1 = Reset output active)
R13	Ramp Active
R12	Unused
R11	Power Supply Enabled
R10	Overflow
R9	Ramp Enabled
R8:R1	State of power supply status inputs (1 = Input Active)

F(4)A(2) – Read current active interrupt level

The currently (or most recently) active interrupt level will be returned.

F(4)A(2)

Bits	Bit Definitions
R16:R6	Reserved
R5:R1	Current interrupt level

F(4)A(3) – Read power supply tracking tolerance

The power supply tracking tolerance is returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(4)A(3). After Channel 3 is read, the next read will return data for Channel 0.

The voltage difference between channel output (after analog summer) and power supply feedback is constantly monitored. If the magnitude (absolute value) of the error exceeds the tolerance for 16 consecutive samples, a power supply tracking error is declared.

F(4)A(3)

Bits	Bit Definitions
R16:R1	Tolerance (0 – +32767)

F(4)A(6) – Read most recent invalid TCLK Event

The last TCLK event that erroneously triggered an interrupt level will be returned.

F(4)A(6)

Bits	Bit Definitions
R16:R1	Most recent invalid TCLK Event

F(4)A(8) – Read most recent invalid CAMAC command

The most recent invalid CAMAC command will be returned. If 0xFFFF (-1) is returned, then no invalid CAMAC commands have been received since reset.

F(4)A(8)

Bits	Bit Definitions
R16:R10	Reserved (Or 0x3F if no invalid CAMAC commands received)
R9:5	Function code of most recent invalid CAMAC Function
R4:1	Subaddress of most recent invalid CAMAC Function

F(4)A(10) – Read TCLK event mask data

Returns the mask state of a given TCLK event. First select a particular TCLK event with F(20)A(1).

The TCLK event (pointer to event mask data) is auto-incremented with each successive call to F(4)A(10). After reading data for TCLK Event $FF, the next call will return data for TCLK event $00.

F(4)A(10)

Bits	Bit Definitions
R16:R2	Unused
R1	TCLK event mask state 1 = Active (used to trigger some interrupt level) 0 = Inactive (event is unused)

F(4)A(11) – Read TCLK event image data

Returns the interrupt level that a given TCLK event will trigger. This data is valid only if the TCLK event mask for this TCLK event is active (See F(4)A(10). First select a particular TCLK event with F(20)A(1).

The TCLK event (pointer to event image data) is auto-incremented with each successive call to F(4)A(11). After reading data for TCLK Event $FF, the next call will return data for TCLK event $00.

F(4)A(11)

Bits	Bit Definitions
R16:R6	Unused
R5:R1	Interrupt level

F(4)A(12) – Read, but do not clear, LAM source register

The CAMAC Look-At-Me (LAM) source register will be returned, but not cleared.

F(4)A(12)

Bits	Bit Definitions
R16	CAMAC Command Error
R15	Calculation Error (Overflow)
R14	Unused
R13	TCLK Missing
R12	Unused
R11	Unused
R10	Power Supply Tracking Error
R9:R5	Unused
R4	Power Supply 3 Error
R3	Power Supply 2 Error
R2	Power Supply 1 Error
R1	Power Supply 0 Error

F(4)A(15) – Read TCLK-triggered interrupt levels disabled flag

Returns the status of TCLK events being able to trigger interrupt levels.

F(4)A(10)

Bits	Bit Definitions
R16:R2	Unused
R1	TCLK event interrupt level trigger enable flag 1 = Disabled (TCLK events disabled to trigger interrupt levels) 0 = Enabled (TCLK events enabled to trigger interrupt levels)

F(5)A(0) – Read ADC

The ADC value will be returned for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(1)A(2). After Channel 3 is read, the next read will return data for Channel 0.

This reading is the voltage difference between the card output (after analog summer) and the power supply feedback signal.

F(5)A(0)

Bits	Bit Definitions
R16:R1	ADC reading (-32768 – +32767)

F(6)A(0) – Read module ID number

F(6)A(0)

Bits	Bit Definitions
R16:R1	0x01D9 (473)

F(6)A(1) – Read firmware version number

F(6)A(1)

Bits	Bit Definitions
R16:R9	Major Revision
R8:R1	Minor Revision

F(6)A(2) – Read a word in memory

Return a word in memory from an address defined by writing to F(16)A(14).

F(6)A(2)

Bits	Bit Definitions
R16:R1	Memory Data

F(6)A(3) – Read a block of memory

Return a word in memory from an address defined by writing to F(16)A(14). The address is auto-incremented with each successive read from F(6)A(3).

F(6)A(3)

Bits	Bit Definitions
R16:R1	Memory Data

F(6)A(4) – Read diagnostic counter

Returns the value of the diagnostic counter selected by F(19)A(2). All diagnostic counters can be cleared by F(26)A(13)

F(6)A(4)

Bits	Bit Definitions
R16:R1	Count

F(6)A(8) – Read FPGA version number

F(6)A(8)

Bits	Bit Definitions
R16:R9	Major Revision
R8:R1	Minor Revision

F(6)A(9) – CAMAC Data Bus Diagnostic Read

F(6)A(9) is a purely diagnostic function. Data sent with F(20)A(12) will be echoed in the first read from F(6)A(9). Subsequent reads from F(6)A(9) will return data in a continuous loop:

F(20)A(12) Data
0x0000
0xFFFF
0x00FF
0xFF00
0x0F0F
0xF0F0
0x3333
0xCCCC
0x5555
0xAAAA
F(20)A(12) Data (start of repeating loop)

F(6)A(9) Read CAMAC Data Bus Diagnostic Data

Bits	Bit Definitions
R16:R1	CAMAC Data Bus Diagnostic Data

F(7)A(0) – Read offset map data

Offset map data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(7)A(0). When the end of one channel's offset map data is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(7)A(0) is the entry in the offset table that will be used when this interrupt level is triggered.

F(7)A(0)

Bits	Bit Definitions
R16:R1	Offset map (0 - 31)

F(7)A(1) – Read offset data

Offset data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

The data pointer is auto-incremented with each successive call to F(7)A(1). When the end of one channel's offset data is reached, successive reads will return data for the next channel, starting with Offset #1 (Offset 0 is the "null" offset and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(7)A(1) is the offset that will be used when this this entry of the offset table is selected (see F(7)A(0)).

F(7)A(1)

Bits	Bit Definitions
R16:R1	Offset (-32768 – +32767)

F(7)A(3) – Read delay data

Ramp delay data will be returned, starting at the point defined with a write to F(16)A(13). Data is read directly out of processor memory. The entry number written to F(16)A(13) sets the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(7)A(3). When the end of one channel's delay data is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(7)A(3) indicates the length of the delay that will be used when this interrupt level is triggered.

F(7)A(3)

Bits	Bit Definitions
R16:R9	Reserved
R8:R1	Ramp Delay (0-65535 microseconds)

F(7)A(4) – Read frequency map data

Frequency map data will be returned, starting at the point defined with a write to F(23)A(9). Data is read directly out of processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(7)A(4). When the end of one channel's frequency map data is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(7)A(4) is the entry in the frequency table that will be used when this interrupt level is triggered.

F(7)A(4)

Bits	Bit Definitions
R16:R1	Frequency map (0 - 31)

F(7)A(5) – Read frequency data

Frequency data will be returned, starting at the point defined with a write to F(23)A(9). Data is read directly out of processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

The data pointer is auto-incremented with each successive call to F(7)A(5). When the end of one channel's frequency data is reached, successive reads will return data for the next channel, starting with Frequency #1 (Frequency 0 is the "null" frequency and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(7)A(5) is the frequency that will be used when this this entry of the freqency table is selected (see F(7)A(4)).

F(7)A(5)

Bits	Bit Definitions
R16:R1	Frequency (0 – +32767) = 0 Hz – 50 kHz

F(7)A(6) – Read phase map data

Phase map data will be returned, starting at the point defined with a write to F(23)A(9). Data is read directly out of processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(7)A(6). When the end of one channel's phase map data is reached, successive reads will return data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(7)A(6) is the entry in the phase table that will be used when this interrupt level is triggered.

F(7)A(6)

Bits	Bit Definitions
R16:R1	Phase map (0 - 31)

F(7)A(7) – Read phase data

Phase data will be returned, starting at the point defined with a write to F(23)A(9). Data is read directly out of processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

The data pointer is auto-incremented with each successive call to F(7)A(7). When the end of one channel's phase data is reached, successive reads will return data for the next channel, starting with Phase #1 (Phase 0 is the "null" phase and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be returned.

The value returned by F(7)A(7) is the sine wave frequency that will be used when this this entry of the freqency table is selected (see F(7)A(6)).

F(7)A(7)

Bits	Bit Definitions
R16:R1	Phase (-32768 – +32767) = -180° - 180°

F(7)A(8) – Read Sine wave mode

Sine wave mode data will be returned

F(7)A(8)

Bits	Bit Definitions
R16:R4	Reserved
R3	Free Run Mode (Sine wave mode only) 1 = Sine wave will free-run at the end of a ramp 0 = Output will hold the last value at DC at the end of a ramp
R2	Sweep Mode (Sine wave mode only) 1 = Channel N will play a sine wave with frequency determined by Channel N+1's ramp 0 = Channel N will play a sine wave with frequency from the frequency table
R1	Sine Wave Mode 1 = Channel will play a sine wave with amplitude defined by f(t) 0 = Channel will play a piecewise linear curve defined by f(t)

F(7)A(9) – Read active frequency

The value of the active frequency for the channel selected by F(19)A(1) will be returned. The channel number is auto-incremented with each successive call to F(7)A(9). After Channel 3 is read, the next read will return data for Channel 0.

Note: This frequency is valid only if Sweep Mode is turned off. This frequency is taken from the frequency table, not the real-time frequency of the sine wave.

F(7)A(9)

Bits	Bit Definitions
R16:R1	Active frequency

F(7)A(10) – Read active phase

The value of the active phase for the channel selected by F(19)A(1) will be returned. The channel number is auto-incremented with each successive call to F(7)A(10). After Channel 3 is read, the next read will return data for Channel 0.

Note: The phase returned is the starting phase used at the beginning of the ramp, taken from the phase table, not the real-time phase of the sine wave.

F(7)A(10)

Bits	Bit Definitions
R16:R1	Active phase

F(7)A(11) – Read final frequency

The value of the sine wave frequency at the end of the last ramp will be returned. This information is useful when tuning a ramp to end with the sine wave at a particular phase. The channel is selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(7)A(11). After Channel 3 is read, the next read will return data for Channel 0.

Note: This frequency data represents the step size used to reach the final phase in the sine wave look-up table.

F(7)A(11)

Bits	Bit Definitions
R16:R1	Final frequency

F(7)A(12) – Read final phase

The value of the sine wave phase at the end of the last ramp will be returned. This information is useful when tuning a ramp to end with the sine wave at a particular phase. The channel is selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(7)A(12). After Channel 3 is read, the next read will return data for Channel 0.

F(7)A(12)

Bits	Bit Definitions
R16:R1	Final phase

F(8)A(0) – Read LAM status

No data is returned with F(8)A(0). If LAM is active, the card will return a Q. If LAM is NOT active, the card will return no Q.

F(8)A(0)

Bits	Bit Definitions
R16:R1	Reserved

F(9)A(0) – Reset module

The C473 will be reset. This function is handled by hardware.

F(16)A(0) – Write f(t) table data

F(t) data will be written in f(t), delta-t order, starting at the point defined with a write to F(16)A(12). Data is entered directly into processor memory. The channel number, table number, and table entry number written to F(16)A(12) set the memory pointer as follows:

```
ptr = Channel * 16 * 64 * 2 +
            Table# * 64 * 2 +
            Table Entry * 2
```

The data pointer is auto-incremented with each successive call to F(16)A(0). When the end of one ramp is reached, successive calls will write data for the next ramp. When the end of one channel's ramps is reached, successive calls will write data for the next channel, starting with Table #1 (Table #0 is the null ramp and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be written.

F(16)A(0)

Bits	Bit Definitions
W16:W1	F(t) table data

F(16)A(5) – Write ramp table map data

Ramp table map data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(16)A(5). When the end of one channel's ramp table map is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(16)A(5) indicates the number of the ramp profile that will be used when this interrupt level is triggered.

F(16)A(5)

Bits	Bit Definitions
W16:W5	Reserved
W4:W1	Ramp Profile Number (0-15)

F(16)A(7) – Write scale factor map data

Scale factor map data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(16)A(7). When the end of one channel's scale factor data is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be returned.

The value written by F(16)A(7) is the entry in the scale factor table that will be used when this interrupt level is triggered.

F(16)A(7)

Bits	Bit Definitions
W16:W1	Scale factor map (0 - 31)

F(16)A(8) – Write scale factor data

Scale factor data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

The data pointer is auto-incremented with each successive call to F(16)A(8). When the end of one channel's scale factor data is reached, successive calls will write data for the next channel, starting with Scale Factor #1 (Scale Factor 0 is the "null" scale factor and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(16)A(8) is the scale factor that will be used when this entry of the scale factor table is selected (see F(16)A(7)). See the section on Scale Factors for an explanation of how scale factor data is interpreted.

F(16)A(8)

Bits	Bit Definitions
W16:W1	Scale factor (-128.0 – 127.9)

F(16)A(9) – Write TCLK event data

TCLK event data will be written, starting at the point defined with a write to F(16)A(11). Data is written directly into processor memory. The TCLK event table pointer written to F(16)A(11) sets the memory pointer as follows:

```
ptr = Interrupt Level * 8 + TCLK Event Slot
```

For instance, if TCLK events $0D, $77, and $34 already trigger interrupt level 22, and we would like to add $45, we would write 22*8 + 3 = 179 to F(16)A(11), then write 0x45 to F(16)A(9).

0xFE is defined as the "Null Event". Writing 0xFE will effectively erase this entry from the TCLK event table. For instance, continuing the example given above, if we would like to now erase TCLK $45 from the TCLK event table, we would write 179 to F(16)A(11), then write 0xFE to F(16)A(9).

Note: Attempts to program a given TCLK event to trigger a second interrupt level will not be processed and will generate an error.

The TCLK event table pointer is auto-incremented with each successive call to F(16)A(9). After data for the eighth TCLK event for interrupt level 31 is written (ptr = 127), the next call will write data for the first TCLK event for interrupt level 0 (ptr = 0).

F(16)A(9)

Bits	Bit Definitions
W16:W9	Reserved
W8:W1	TCLK Event

F(16)A(11) – Set up TCLK event table pointer

The TCLK event table pointer will be written

F(16)A(11)

Bits	Bit Definitions
W16:W9	Reserved
W8:W1	TCLK event table pointer

F(16)A(12) – Set up pointer for ramp data read/write

F(16)A(12)

Bits	Bit Definitions
W16:W11	Table Entry #
W10:W6	Table # (Write 0 – 14 to select ramp tables 1 – 15. Ramp table 0 is the null ramp and cannot be selected)
W5:W3	Reserved
W2:W1	Channel #

F(16)A(13) – Set up pointer for ramp table map, scale factor map, scale factor, offset map, offset, and delay read/write

F(16)A(13)

Bits	Bit Definitions
W16:W11	Reserved
W10:W6	Entry #
W5:W3	Data Type 0 = Ramp Table Map 2 = Scale Factor Map 3 = Scale Factor * 4 = Offset Map 5 = Offset ** 7 = Delay
W2:W1	Channel #

* When selecting an entry in the scale factor table (data type 3), write 0 – 30 to select scale factor table entry 1 – 31. Example: writing 7 in the "Entry #" field will select scale factor table entry 8. Scale factor table entry 0 is the null scale factor and cannot be selected.

** When selecting an entry in the offset table (data type 5), write 0 – 30 to select offset table entry 1 – 31. Example: writing 7 in the "Entry #" field will select offset table entry 8. Offset table entry 0 is the null offset and cannot be selected.

F(16)A(14) – Set up diagnostic memory pointer

Two successive writes to F(16)A(14) define the 32-bit Diagnostic Memory Pointer. The first write will define the lower (least significant) 16 bits. The second write will define the upper (most significant) 16 bits.

F(16)A(14)

Bits	Bit Definitions
W16:W1	Diagnostic memory pointer

F(17)A(0) – Write TCLK Interrupt Level Counter Pointer

F(17)A(0)

Bits	Bit Definitions
W16:W1	TCLK Interrupt Level Counter Pointer

F(17)A(2) – Write directly to DAC

Write directly to the DAC for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(17)A(2). After Channel 3 is written, the next call will write data for Channel 0.

F(17)A(2)

Bits	Bit Definitions
W16:W1	DAC setting (-32768 – +32767)

F(17)A(7) – Write power supply status nominal

The nominal power supply status will be written for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(17)A(7). After Channel 3 is written, the next call will write data for Channel 0.

This is the value "expected" to be returned by a read of power supply status.

F(17)A(7)

Bits	Bit Definitions
W16	Reserved
W15	Power Supply Tracking Error
W14	Power Supply Reset (1 = Reset output active)
W13	Ramp Active
W12	Unused
W11	Power Supply Enabled
W10	Overflow
W9	Ramp Enabled
W8:W1	State of power supply status inputs

F(17)A(8) – Write power supply status mask

The power supply status mask will be written for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(17)A(8). After Channel 3 is written, the next call will write data for Channel 0.

A bit cleared in the status mask will suppress errors when the actual power supply status bit does not match the nominal status bit.

F(17)A(8)

Bits	Bit Definitions
W16	Reserved
W15	Power Supply Tracking Error
W14	Power Supply Reset
W13	Ramp Active
W12	Unused
W11	Power Supply Enabled
W10	Overflow
W9	Ramp Enabled
W8:W1	State of power supply status inputs

F(17)A(9) – Write LAM Mask

The CAMAC Look-At-Me (LAM) mask will be written.

A bit cleared in the LAM mask will suppress LAM when the corresponding bit is set in the LAM Source.

F(17)A(9)

Bits	Bit Definitions
W16	CAMAC Command Error
W15	Calculation Error (Overflow)
W14	Unused
W13	TCLK Missing
W12	Unused
W11	Unused
W10	Power Supply Tracking Error
W9:W5	Unused
W4	Power Supply 3 Error
W3	Power Supply 2 Error
W2	Power Supply 1 Error
W1	Power Supply 0 Error

F(17)A(10) – Manual Interrupt Level Trigger

Manually trigger an interrupt level. Issuing this command will trigger an interrupt level, just as if a TCLK event occurred that was mapped to that interrupt level, including delay. If a ramp is active at the time this command is sent, it will be ignored, just as if a mapped TCLK event had come along while a ramp was active.

F(17)A(10)

Bits	Bit Definitions
W16:6	Reserved
W5:W1	Interrupt Level

F(19)A(1) – Write Channel Pointer

F(19)A(1)

Bits	Bit Definitions
W16:W1	Channel Pointer

F(19)A(2) – Select Diagnostic Counter

Select a diagnostic counter to be read by F(6)A(4).

F(19)A(2)

Bits	Bit Definitions
W16:W1	Diagnostic counter selection 0 = CAMAC interrupt counter 1 = TCLK event counter (indicates the number of raw TCLK events received since reset) 2 = 1Hz counter 3 = TCLK Error Counter (Invalid TCLK event) 4 = TCLK Parity Error Counter 5 = TCLK Signal Error Counter

F(20)A(3) – Write power supply tracking tolerance

The power supply tracking tolerance is written for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(20)A(3). After Channel 3 is written, the next call will write data for Channel 0.

The voltage difference between channel output (after analog summer) and power supply feedback is constantly monitored. If the magnitude (absolute value) of the error exceeds the tolerance for 16 consecutive samples, a power supply tracking error is declared.

F(20)A(3)

Bits	Bit Definitions
W16:W1	Tolerance (0 – +32767)

F(20)A(11) – Write generic clock event table diagnostic pointer

F(20)A(11)

Bits	Bit Definitions
W16:W1	Generic clock event table diagnostic pointer (0 – 255)

F(20)A(12) – CAMAC Data Bus Diagnostic Write

F(20)A(12) is a purely diagnostic function. Data sent with F(20)A(12) will be echoed in the first read from F(6)A(9).

F(20)A(12)

Bits	Bit Definitions
W16:W1	CAMAC Data Bus Diagnostic Data

F(23)A(0) – Write offset map data

Offset map data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(23)A(0). When the end of one channel's offset map data is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(23)A(0) is the entry in the offset table that will be used when this interrupt level is triggered.

F(23)A(0)

Bits	Bit Definitions
W16:W1	Offset map (0 - 31)

F(23)A(1) – Write offset data

Offset data will be written, starting at the point defined with a write to F(16)A(13). Data is written directly into processor memory. The channel number and entry number written to F(16)A(13) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(23)A(1). When the end of one channel's offset data is reached, successive calls will write data for the next channel, starting with Offset #1 (Offset 0 is the "null" offset and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(23)A(1) is the offset that will be used when this interrupt level is triggered.

F(23)A(1)

Bits	Bit Definitions
W16:W1	Offset (-32768 – +32767)

F(23)A(3) – Write delay data

Ramp delay data will be written, starting at the point defined with a write to F(16)A(13). Data is read directly into processor memory. The entry number written to F(16)A(13) sets the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(23)A(3). When the end of one channel's delay data is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(23)A(3) indicates the length of the delay that will be used when this interrupt level is triggered.

F(23)A(3)

Bits	Bit Definitions
W16:W9	Reserved
W8:W1	Ramp Delay (0-65535 microseconds)

F(23)A(4) – Write frequency map data

Frequency map data will be written, starting at the point defined with a write to F(23)A(9). Data is written directly into processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(23)A(4). When the end of one channel's frequency map data is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(23)A(4) is the entry in the frequency table that will be used when this interrupt level is triggered.

F(23)A(4)

Bits	Bit Definitions
W16:W1	Frequency map (0 - 31)

F(23)A(5) – Write frequency data

Frequency data will be written, starting at the point defined with a write to F(23)A(9). Data is written directly into processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(23)A(5). When the end of one channel's frequency data is reached, successive calls will write data for the next channel, starting with Frequency #1 (Frequency 0 is the "null" frequency and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(23)A(5) is the sine wave frequency that will be used when this interrupt level is triggered.

F(23)A(5)

Bits	Bit Definitions
W16:W1	Frequency (0 – +32767) = 0 Hz to 50 kHz

F(23)A(6) – Write phase map data

Phase map data will be written, starting at the point defined with a write to F(23)A(9). Data is written directly into processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(23)A(6). When the end of one channel's phase map data is reached, successive calls will write data for the next channel. After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(23)A(4) is the entry in the frequency table that will be used when this interrupt level is triggered.

F(23)A(6)

Bits	Bit Definitions
W16:W1	Phase map (0 - 31)

F(23)A(7) – Write phase data

Phase data will be written, starting at the point defined with a write to F(23)A(9). Data is written directly into processor memory. The channel number and entry number written to F(23)A(9) set the memory pointer as follows:

```
ptr = Channel * 32 + Entry + 1
```

In this case, "Entry" is an interrupt level. The data pointer is auto-incremented with each successive call to F(23)A(7). When the end of one channel's frequency data is reached, successive calls will write data for the next channel, starting with Phase #1 (Phase 0 is the "null" phase and cannot be accessed). After the end of data for Channel 3, data for Channel 0 will be written.

The value written by F(23)A(7) is the sine wave starting phase that will be used when this interrupt level is triggered.

F(23)A(7)

Bits	Bit Definitions
W16:W1	Phase (-32768 – +32767) = -180° - 180°

F(23)A(8) – Write Sine wave mode

Sine wave mode data will be written.

F(23)A(8)

Bits	Bit Definitions
W16:W4	Reserved
W3	Free Run Mode (Sine wave mode only) 1 = Sine wave will free-run at the end of a ramp 0 = Output will hold the last value at DC at the end of a ramp
W2	Sweep Mode (Sine wave mode only) 1 = Channel N will play a sine wave with frequency determined by Channel N+1's ramp 0 = Channel N will play a sine wave with frequency from the frequency table
W1	Sine Wave Mode 1 = Channel will play a sine wave with amplitude defined by f(t) 0 = Channel will play a piecewise linear curve defined by f(t)

F(23)A(9) – Set up pointer for frequency map, frequency, phase map, and phase read/write

F(23)A(9)

Bits	Bit Definitions
W16:W7	Entry #
W6:W3	Data Type 0 = Frequency Map 1 = Frequency * 2 = Phase Map 3 = Phase **
W2:W1	Channel #

* When selecting an entry in the frequency table (data type 1), write 0 – 30 to select frequency table entry 1 – 31. Example: writing 7 in the "Entry #" field will select frequency table entry 8. Frequency table entry 0 is the null frequency and cannot be selected.

** When selecting an entry in the phase table (data type 3), write 0 – 30 to select phase table entry 1 – 31. Example: writing 7 in the "Entry #" field will select phase table entry 8. Phase table entry 0 is the null offset and cannot be selected.

F(24)A(0) – Disable LAM

CAMAC Look-At-Me (LAM) will be Disabled.

All data sent with F(24)A(0) is ignored.

F(24)A(2) – Disable Channel Waveform

Disable the waveform output for the channel selected by F(19)A(1). The next TCLK trigger will result in no waveform output for this channel. The last value written to the DAC will be held. Manual DAC writes will still have effect. The channel number is auto-incremented with each successive call to F(24)A(2). After Channel 3, the next call will disable Channel 0.

All data sent with F(24)A(2) is ignored.

F(24)A(5) – Disable TCLK-Triggered Interrupt Levels

After sending F(24)A(5), no TCLK event will trigger an interrupt level. Interrupt levels can still be triggered using F(17)A(10). The TCLK event tables remain intact, but will have no effect.

All data sent with F(24)A(5) is ignored.

F(24)A(6) – Turn off power supply

Turn off the power supply for the channel selected by F(19)A(1). The power supply will immediately be turned off. The channel number is auto-incremented with each successive call to F(24)A(6). After Channel 3, the next call will turn off Channel 0.

All data sent with F(24)A(6) is ignored.

F(25)A(0) – Decrement the DAC

Decrement the DAC for the channel selected by F(19)A(1). If the DAC is already at -32768, this command will be ignored.

Unlike most other commands, the channel number will not be auto-incremented with each successive call to F(25)A(0) or F(25)A(1), allowing one channel's DAC to be incremented or decremented several times in a row without resetting the channel number.

All data sent with F(25)A(0) is ignored.

F(25)A(1) – Increment the DAC

Increment the DAC for the channel selected by F(19)A(1). If the DAC is already at +32767, this command will be ignored.

Unlike most other commands, the channel number will not be auto-incremented with each successive call to F(25)A(0) or F(25)A(1), allowing one channel's DAC to be incremented or decremented several times in a row without resetting the channel number.

All data sent with F(25)A(1) is ignored.

F(26)A(0) – Enable LAM

CAMAC Look-At-Me (LAM) will be Enabled.

All data sent with F(26)A(0) is ignored.

F(26)A(2) – Enable Channel Waveform

Enable the waveform output for the channel selected by F(19)A(1). The next TCLK trigger will result in normal waveform output for this channel. The channel number is auto-incremented with each successive call to F(26)A(2). After Channel 3, the next call will enable Channel 0.

All data sent with F(26)A(2) is ignored.

F(26)A(5) – Enable TCLK-Triggered Interrupt Levels

After sending F(26)A(5), TCLK events are once again enabled to trigger interrupt levels, as defined by the TCLK event tables.

All data sent with F(26)A(5) is ignored.

F(26)A(6) – Turn on power supply

Turn on the power supply for the channel selected by F(19)A(1). The channel number is auto-incremented with each successive call to F(26)A(6). After Channel 3, the next call will turn on Channel 0.

All data sent with F(26)A(6) is ignored.

F(26)A(8) – Reset power supply

Reset the power supply for the channel selected by F(19)A(1). The power supply's reset signal will be activated for one second. The channel number is auto-incremented with each successive call to F(26)A(8). After Channel 3, the next call will turn on Channel 0.

All data sent with F(26)A(8) is ignored.

F(26)A(12) – Clear TCLK Clock Event Table

The entire TCLK Event Table will be cleared. This can take a second or so.

All data sent with F(26)A(12) is ignored.

F(26)A(13) – Clear Diagnostic Counters

All diagnostic counters will be reset to 0x0000.

All data sent with F(26)A(13) is ignored.

Theory of Operation

Ramp Outputs

The C473 user programs the card with the following data:

- Which TCLK events will cause triggers
- Which interrupt levels will activate as a result of TCLK event triggers. Each TCLK event will trigger either zero or one interrupt level, never more than one. Every channel will execute the same interrupt level, but each channel will have its own ramp profile, scale factor, offset, delay, frequency, and phase.
- Delay between TCLK event and start of ramp outputs. Each channel can be programmed with an independent delay.
- A table of ramp profiles (the basic shape of the ramp output). Each channel gets its own table of ramp profiles.
- Which ramp profile to use by each channel for each interrupt level
- A scale factor to use for each interrupt level. Each channel will have a unique scale factor.
- An offset to use for each interrupt level. Each channel will have a unique offset.
- Sine wave frequency and phase. Each channel will have a unique frequency and phase.

The C473 constantly monitors TCLK. Every time a TCLK event is received, the FPGA uses that event as an address to read a RAM containing interrupt level map data. Bit 7 of this data will have been set if this TCLK event is enabled to cause a trigger. Bits 4:0 indicate which interrupt level will be triggered.

If an enabled TCLK event is detected, an abort signal will be sent to each ramp controller to terminate any active ramps, and the FPGA will interrupt the processor. Simultaneously, the FPGA will use the decoded interrupt level as an address to another RAM containing delay data and preset a counter with this data. The counter decrements once every microsecond.

Once interrupted, the processor must very quickly start downloading ramp parameters to the FPGA. The scale factors, offsets, frequencies, phases, and first (f(t), delta-t) data points must be downloaded to the FPGA before the counter reaches zero. After this first set of data, the rest of the (f(t), delta-t) data points must be downloaded fast enough to stay ahead of the ramp (10 μsec per data point).

Typically, it takes about 15 μsec for the processor to download the initial data set, and 3 μsec to download each data point for four channels after that. Care must be taken not to write code that will interfere with servicing this interrupt. If other interrupts will be serviced by the processor (for timers, CAMAC communications, etc), it is highly recommended that those routines start and end with alt_irq_interruptible() and alt_irq_non_interruptible(), respectively, to allow the ramp download service routine to interrupt them.

When the delay counter reaches zero, the FPGA starts sending ramp data to the DAC. The FPGA does not know the difference between “old” and “new” data, “good” or “bad”. If the user

has not programmed a long enough delay to allow the processor to download the new ramp, the FPGA will simply start sending data from the previous ramp.

The ramp output will take the following form:
output = scale_factor * f(t) + offset

where:

- scale_factor is a constant scale factor having a range of -128.0 to +127.9
- f(t) is an interpolated function of time which is initiated by a TCLK event. f(t) defines the overall shape of the output function
- offset is a constant offset having a range of -32768 to +32767

The function f(t) is downloaded to the FPGA as a piecewise linear curve. Each point consists of a ramp value V (before being scaled and offset) and a delta-t value. Delta-t_n defines the number of samples (at 10 µsec per sample) between V_n and V_{n+1}.

Samples between points n and n+1 are interpolated as follows:

$$V = scale\_factor * \left(V_{n+1} - \left(\frac{(V_{n+1} - V_n)}{deltat(n)} * samples\_remaining \right) \right) + offset$$

The final delta-t value of f(t) must be zero. A delta-t of zero is the flag the FPGA uses to indicate the end of the ramp. The final V value will be held until the next ramp (or manual set, increment/decrement, etc).

The FPGA constantly monitors ramp calculations for overflows. An overflow will occur if a data point's value would be less than -32768 or greater than 32767. If an overflow is detected, the last valid value is held.

Sine Wave Mode

In sine wave mode, the ramp output calculated above will be used as the amplitude of a sine wave rather than being sent directly to the DAC.

The output will take the following form:
output = (scale_factor * f(t) + offset) * sin(2πfreq + phase)

Sine waves are generated by a look-up table (LUT). The LUT is 4096 steps long. A LUT entry is selected by the upper 12 bits of a 16-bit counter. The counter increments at a 100 kHz rate. The raw data of the frequency setting sets the step size of the counter. The raw data of the phase setting defines the counter's initialization point when a ramp starts.

Each channel has its own LUT. Physically, each LUT exists as a 1024x16-bit RAM in the FPGA. At boot-up, the processor programs the LUT with the first quadrant (first 90 degrees) of a sine wave. This quadrant is used to generate all four quadrants of the sine wave by decoding the top two bits of the LUT pointer.

- Bit 14 = 1: Play quadrant in reverse
- Bit 15 = 1: Invert quadrant value

The wave in the LUT is assumed to be unity amplitude, with signed values. When a ramp value is multiplied by the LUT value, the lower 14 bits of the result are simply dropped.

Because the LUT is a programmable RAM, we are in theory not restricted to playing a sine wave. Any odd wave that could be defined in four symmetrical quadrants could be used (square wave, triangle, etc). For now, the processor is hard-coded to download a sine wave.

Sweep Mode

In sweep mode, the ramp output calculated by channel N will be sent to channel N-1 and used as a frequency.

For example, the output of channel 0 will take the following form:
output = (scale_factor0 * f0(t) + offset0) * sin(2π[scale_factor1 * f1(t) + offset1] + phase)

The ramp output of channel N is still sent to the DAC, generating a waveform that can be used as a reference.

Free-Run Mode

In free-run mode, a sine wave will continue to play at after an amplitude ramp ends. If sweep mode is selected, the amplitude is held constant after the ramp, but the frequency will continue to be modified by channel N+1's ramp until channel N+1's ramp ends. With free-run mode disabled, the last value send to the DAC will be held as a DC value.

ADC Inputs

The output of the C473 (after summer) is compared to an analog feedback signal from the power supply. An error signal is created by applying these two signals to the two sides of a differential instrumentation amplifier. The error signal is read by a sixteen-bit ADC every time the DAC is loaded with new data or every 25.6 μsec (1024 clocks @ 40 MHz), whichever comes first. The digitized error signal is compared to a threshold value, programmed by the user. If the absolute value of the error is greater than the threshold value for sixteen consecutive samples, the power supply is declared "out of tolerance" and an error flag is set.

Processor I/O Memory Map

This section is intended for people who wish to write code to run in the C473. Users of the C473 may also gain greater insight into the C473's sequence of operations.

The C473's software runs on an Altera NiosII processor, embedded in the FPGA. The processor is connected to all of its peripherals automatically by Altera's SOPC Builder tool. SOPC builder automatically assigns base addresses to all of the peripherals. Adding, deleting, or modifying these peripherals usually results in completely different base addresses being assigned. These base addresses are aliased by #define's in the file system.h. System.h is automatically generated by Altera's NiosII IDE. Because the actual base addresses are constantly shifting, the system.h aliases are used in this document instead. The one device that has a locked base address is the flash memory.

1. Flash Memory
Flash memory is hard coded to a base address of 0x00000000. Memory space is reserved for as much as 16 megabytes of flash memory. The C473 board is laid out to accommodate a Spansion (AMD) AM29LV128M or equivalent. A smaller part with equivalent pinout may be substituted.

2. SRAM
Up to two megabytes of SRAM is located at EXT_SSRAM_BASE. The C473 is laid out to accommodate a Cypress CY7C1380 synchronous SRAM or equivalent. A smaller part with equivalent pinout may be substituted.

3. Timers
Three timer peripherals are included. See Chapter 12 of Altera's QuartusII Handbook Volume 5: Embedded Peripherals, "Timer Core With Avalon Interface" for programming information.

The system clock timer (SYS_CLK_TIMER_BASE) is used by the processor to generate system delays, such as when using the usleeep() function.

Two other timers are included (TIMER_1SEC_BASE and TIMER_100HZ_BASE) and are intended to be used to generate interrupts at regular 1 second and 10 msec intervals.

4. Ramp Controller (TCLK_RAMP.VHD)

The Ramp Controller is mapped to TCLK_RAMP_0_BASE. It contains the TCLK Decoder, Ramp Launch Control, the Ramp Generators, and the DAC Controller. Only the Ramp Launch Control and Ramp Generators are addressable.

4.1. Ramp Launch Control(RAMP_LAUNCH.VHD)

TCLK Trigger Map: Word32 Offset 0x0000 – 0x00FF

The TCLK Trigger Map is stored in a 256x8 SRAM in the FPGA. The Word32 offset is decoded as 0000_0000_TTTT_TTTT, where:

TTTT_TTTT = TCLK Event

This SRAM is write-only from the processor.

The FPGA will read this SRAM every time a TCLK event is received, using the TCLK event as the read address. The FPGA determines whether or not this event is enabled for triggering, and if enabled, the FPGA will interrupt the processor, load the Active Interrupt Level register, and start a delay timer.

TCLK Trigger Map

Bits	Bit Definitions
31:8	Reserved
7	TCLK Event Enable 1 = This TCLK event is enabled to launch the interrupt level in bits 4:0 0 = This TCLK event is disabled
6:5	Reserved
4:0	Interrupt level to be launched by this TCLK event

Ramp Launch Delay: Word32 Offset 0x0100 – 0x017F

The Ramp Launch Delays are stored in a 32x8 SRAM in the FPGA. The Word32 offset is decoded as 0000_0001_0CCL_LLLL, where:

CC = Channel Number
LLLLL = Interrupt Level

This SRAM is write-only from the processor.

The FPGA will read this SRAM every time an enabled TCLK event is received, using the triggered interrupt level number as the read address. A delay timer is preset with this data and will decrement once every µsec. When this timer expires, the Ramp Launch Control issues the Ramp Start signal.

Ramp Launch Delay

Bits	Bit Definitions
31:8	Reserved
7:0	Ramp Launch Delay, in µsec

Active Interrupt Level: Word32 Offset 0x0200 (Read)

This register is read-only to the processor.

When the processor enters the ramp load interrupt service routine, the first thing it should do is come here and read the Active Interrupt Level register.

Active Interrupt Level

Bits	Bit Definitions
31:5	Reserved
4:0	Active Interrupt Level

IRQ Clear: Word32 Offset 0x0200 (Write)

When the processor completes the ramp load interrupt service routine, it should issue a write to this address to clear the interrupt. The simple act of writing to this register clears the interrupt. Data is ignored.

IRQ Clear

Bits	Bit Definitions
31:0	Reserved – Ignored

Manual Interrupt Level Trigger: Word32 Offset 0x0201

Writing to this register will trigger an interrupt level, just as if a TCLK event occurred that was mapped to that interrupt level, including delay. If a ramp is active at the time this command is sent, it will be ignored, just as if a mapped TCLK event had come along while a ramp was active.

This register is write-only.

Manual Ramp Trigger

Bits	Bit Definitions
31:5	Reserved
4:0	Interrupt Level

Interrupt Level TCLK Source: Word32 Offset 0x0202

This register indicates which TCLK event triggered the current (or most recent) interrupt level. If 0xFE is returned, the interrupt level was triggered manually, or there have been no interrupt levels triggered since reset.

This register is read-only.

Interrupt Level TCLK Source

Bits	Bit Definitions
31:8	Reserved
7:0	Interrupt Level TCLK source

Disable TCLK-Triggered Interrupt Levels: Word32 Offset 0x0203

Use this register to disable TCLK-triggered interrupt levels for all four channels. When this register is set, the TCLK trigger map remains intact, but the state machine that watches for mapped TCLK events is inhibited. Interrupt levels can still be manually triggered.

Disable TCLK-Triggered Interrupt Levels

Bits	Bit Definitions
31:1	Reserved
0	1 = Disable 0 = Enable

Abort Current Ramp: Word32 Offset 0x0204

This register will terminate any currently running ramp. The last value sent to the DAC will be held until the next ramp starts or until the DAC is manually written.

This register is write-only.

Abort Current Ramp

Bits	Bit Definitions
31:4	Reserved
3	Abort Channel 3 Ramp
2	Abort Channel 2 Ramp
1	Abort Channel 1 Ramp
0	Abort Channel 0 Ramp

Ramp Generation (RAMP_CTRL.VHD)

Each channel has its own ramp generator. The memory map is:

Channel 0: TCLK_RAMP_0_BASE + 0x2000
Channel 1: TCLK_RAMP_0_BASE + 0x2400
Channel 2: TCLK_RAMP_0_BASE + 0x2800
Channel 3: TCLK_RAMP_0_BASE + 0x2C00

F(t) Table: Word32 Offset 0x0000 – 0x007F

F(t) data is stored in a 128x16 SRAM in the FPGA. The Word32 offset is decoded as 0000_0000_0NNN_NNNB, where:

NNNNNN = F(t) table entry number (0 – 63)
B = Voltage data or delta-t data:
0 = Voltage data V(n)
1 = delta-t data $\Delta t(n)$

This SRAM is write-only to the processor.

The Ramp Generator begins reading this SRAM after the Ramp Start signal is received from the Ramp Launch module. The Ramp Generator updates the DAC every 10 μsec until it reads zero for delta-t.

F(t) Table

Bits	Bit Definitions
31:16	Reserved
15:0	Voltage or delta-t data (-32768 – +32767)

DAC Value: Word32 Offset 0x0080

Reading this register returns the most recent programmed DAC value.

Writing this register while the ramp is active has no effect. Otherwise, writing this register sends data to the DAC.

Note: From the processor's point of view, this data value is read and written as a signed, 16-bit value between -32768 and +32767, representing a desired voltage between -10V and +10V. The actual data sent to the DAC is translated to account for actual hardware requirements. See the DAC Controller section for more information.

Each Ramp Generator sends its own DAC Update signal to the DAC Controller every 10 µsec during an active ramp, or in response to a manual DAC write.

DAC Value

Bits	Bit Definitions
31:16	Reserved
15:0	DAC Value (-32768 – +32767 = -10V to +10V)

Ramp/Power Supply Status: Word32 Offset 0x0081

This register returns ramp and power supply status. Writes are necessary only to clear the Overflow Status bit.

Ramp/Power Supply Status

Bits	Bit Definitions
31:14	Reserved
13	Power Supply Reset Status 1 = PS reset output active
12	Ramp Active 1 = Ramp is active
11	Power Supply Interlock Status 1 = PS Interlock input is active (Tied Active in FPGA, ignore)
10	Power Supply Enable Status 1 = PS Enable output is active
9	Overflow Status 1 = A mathematical overflow has occurred. Write 0 to this bit to clear.
8	Ramp Enabled 1 = Ramp is enabled. This is a status bit only. Writes will have no effect.
7:0	Reserved

Sample Count Remaining: Word32 Offset 0x0083

This read-only register returns the number of samples remaining in the current segment of the active F(t) piecewise-linear curve.

Sample Count Remaining

Bits	Bit Definitions
31:12	Reserved
11:0	Samples remaining

Scale Factor: Word32 Offset 0x0084

Writing this register during an active ramp will have no immediate effect. Data written here will be loaded into the Ramp Generator's scale factor register at the end of the active ramp. Writing this register while no ramp is active will immediately load the scale factor register.

Reading this register returns the scale factor register. Data may not reflect most recent write if the write occurred during an active ramp and that ramp is still active.

Scale Factor

Bits	Bit Definitions
31:16	Reserved
15:0	Scale Factor (-32768 – +32767 = -128.0 to +127.9)

Offset: Word32 Offset 0x0085

Writing this register during an active ramp will have no immediate effect. Data written here will be loaded into the Ramp Generator's offset register at the end of the active ramp. Writing this register while no ramp is active will immediately load the offset register.

Reading this register returns the offset register. Data may not reflect most recent write if the write occurred during an active ramp and that ramp is still active.

Offset

Bits	Bit Definitions
31:16	Reserved
15:0	Offset (-32768 – +32767 = -10V to +10V)

Power Supply Enable: Word32 Offset 0x0086

Writing to this register enables or disables the power supply.

This register is write-only. The power supply enable state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Power Supply Enable 1 = Enable

Power Supply Reset: Word32 Offset 0x0087

Writing to this register sets the state of the Power Supply Reset output.

This register is write-only. The power supply reset state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Power Supply Reset 1 = Reset output active

Ramp Enable: Word32 Offset 0x0088

Writing to this register enables or disables the ramp controller. Writing during an active ramp will have no immediate effect. The ramp enable bit inhibits the ramp controller's state machine from starting, but has no effect while the state machine is running.

This register is write-only. The ramp enable state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Ramp Enable 1 = Enable

Ramp Active Segment: Word32 Offset 0x0089

This register indicates which segment of an F(t) ramp profile is currently active. This register is read-only.

Ramp Active Segment

Bits	Bit Definitions
31:6	Reserved
5:0	Active Segment

Calculation Overflow Count: Word32 Offset 0x008A

This register increments every time a calculation overflow is detected. As calculations happen at a 100kHz rate, this register can wrap up rather quickly.

Any write to this register will clear it to 0x0000.

Calculation Overflow Count

Bits	Bit Definitions
31:16	Reserved
15:0	Calculation Overflow Count

LUT Step Size (Frequency): Word32 Offset 0x00A0

This register defines the step size used by the LUT pointer counter.

LUT Step Size

Bits	Bit Definitions
31:16	Reserved
15:0	LUT Step Size

LUT Phase: Word32 Offset 0x00A1

This register defines the point to which the LUT pointer counter is initialized when a ramp starts.

LUT Phase

Bits	Bit Definitions
31:16	Reserved
15:0	LUT Phase

LUT Mode: Word32 Offset 0x00A2

This register is used to enable and disable LUT Mode (Sine Wave Mode), Sweep Mode, and Free-Run Mode.

LUT Phase

Bits	Bit Definitions
31:3	Reserved
2	1 = Enable Free-Run Mode
1	1 = Enable Sweep Mode
0	1 = Enable LUT Mode (Sine Wave Mode)

Final LUT Step Size: Word32 Offset 0x00A3

This register will return the final LUT step size at the end of a ramp. The value returned is the step size used to reach the final phase at the end of a ramp. This information may be useful when tuning a ramp to end with the sine wave at a particular phase.

This register is read-only.

Final LUT Step Size

Bits	Bit Definitions
31:16	Reserved
15:0	Final LUT Step Size

Final LUT Phase: Word32 Offset 0x00A4

This register will return the final LUT phase at the end of a ramp. This information may be useful when tuning a ramp to end with the sine wave at a particular phase.

This register is read-only.

Final LUT Phase

Bits	Bit Definitions
31:16	Reserved
15:0	Final LUT Phase

4.2. TCLK Receiver

Information about the TCLK Receiver is located starting at TCLK_RAMP_0_BASE + 0x3400.

TCLK Status: Word32 Offset 0x0000

This register indicates the status of the TCLK signal. A '1' in any bit position can be cleared by writing a '0' to that bit.

TCLK Status

Bits	Bit Definitions
31:3	Reserved
2	1 = TCLK signal error detected
1	1 = TCLK parity error detected
0	1 = TCLK signal is present

Raw TCLK Event Count: Word32 Offset 0x0001

This register indicates how many TCLK events the card has detected since reset. It will count up to 65535, then roll over to 0 and continue counting.

This is a count of raw TCLK events, not a TCLK interrupt level count.

Any write to this register will clear it to 0x0000.

Raw TCLK Event Count

Bits	Bit Definitions
31:16	Reserved
15:0	TCLK Event Count

4.3. Look-Up Tables

The Look-Up Tables (LUTs) are mapped starting at TCLK_RAMP_0_BASE + 0x4000. Each channel's LUT data is stored in a 1024x16 SRAM in the FPGA. The Word32 offset is decoded as 0000_CCNN_NNNN_NNNN, where:

CC = Channel number (0 – 3)
NNNNNNNNNN = LUT table entry number (0 – 1023)

The Look-Up Tables contain only the first quadrant of a wave. The other three quadrants are reproduced by time-reversal and data inversion.

It is assumed that the data in the LUT is signed and that the amplitude of the wave described is unity (1).

5. ADC Controller (ADC_CTRL.VHD)
The ADC Controller is mapped to ADC_CTRL_0_BASE. The ADC data is automatically updated every time the DAC is updated or every 25.6 µsec (1024 clocks @ 40MHz), whichever comes first.

ADC0 Data: Word32 Offset 0x0000

Reading this register returns ADC0 data. ADC0 reads the difference between the Channel 0 output (after analog summer) and the power supply 0 feedback input.

ADC0 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC0 Data (-32768 – 32767 = -10V to 10V)

ADC1 Data: Word32 Offset 0x0001

Reading this register returns ADC1 data. ADC1 reads the difference between the Channel 1 output (after analog summer) and the power supply 1 feedback input.

ADC1 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC1 Data (-32768 – 32767 = -10V to 10V)

ADC2 Data: Word32 Offset 0x0002

Reading this register returns ADC2 data. ADC2 reads the difference between the Channel 2 output (after analog summer) and the power supply 2 feedback input.

ADC2 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC2 Data (-32768 – 32767 = -10V to 10V)

ADC3 Data: Word32 Offset 0x0003

Reading this register returns ADC3 data. ADC3 reads the difference between the Channel 3 output (after analog summer) and the power supply 3 feedback input.

ADC3 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC3 Data (-32768 – 32767 = -10V to 10V)

Channel 0 Tolerance: Word32 Offset 0x0004

Sets or returns the Channel 0 tolerance.

If the absolute value of the ADC0 reading is greater than the Channel 0 Tolerance for sixteen consecutive samples, Channel 0 is declared “out of tolerance” and the Channel 0 Out Of Tolerance bit will be set.

Channel 0 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 0 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 1 Tolerance: Word32 Offset 0x0005

Sets or returns the Channel 1 tolerance.

If the absolute value of the ADC1 reading is greater than the Channel 1 Tolerance for sixteen consecutive samples, Channel 1 is declared “out of tolerance” and the Channel 1 Out Of Tolerance bit will be set.

Channel 1 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 1 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 2 Tolerance: Word32 Offset 0x0006

Sets or returns the Channel 2 tolerance.

If the absolute value of the ADC2 reading is greater than the Channel 2 Tolerance for sixteen consecutive samples, Channel 2 is declared “out of tolerance” and the Channel 2 Out Of Tolerance bit will be set.

Channel 2 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 2 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 3 Tolerance: Word32 Offset 0x0007

Sets or returns the Channel 3 tolerance.

If the absolute value of the ADC3 reading is greater than the Channel 3 Tolerance for sixteen consecutive samples, Channel 3 is declared “out of tolerance” and the Channel 3 Out Of Tolerance bit will be set.

Channel 3 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 3 Tolerance (-32768 – 32767 = -10V to 10V)

ADC Status: Word32 Offset 0x0008

Reading this register returns the Out Of Tolerance bits for all four channels. Writing 0 to a set bit will clear it.

ADC Status

Bits	Bit Definitions
31:4	Reserved
3	Channel 3 Out Of Tolerance 1 = Out Of Tolerance
2	Channel 2 Out Of Tolerance 1 = Out Of Tolerance
1	Channel 1 Out Of Tolerance 1 = Out Of Tolerance
0	Channel 0 Out Of Tolerance 1 = Out Of Tolerance

6. DAC Controller (DAC_CTRL.vhd)
The DAC Controller is mapped to TCLK_RAMP_0_BASE + 0x3000. The DAC Controller takes programmed DAC values from the Ramp Controller. The programmed DAC values are translated before actually going to the DAC to account for three things:

- The DAC output gets inverted by the summing amplifier, so the actual DAC data must be "pre-inverted"
- Because there are an even number of possible DAC codes, after inversion the DAC value is further shifted by one count, to ensure that zero still maps to zero, and not -1.
- The Burr-Brown DAC7744 used on the C473 expects a different data format: 0 to 65535 (unsigned 16 bit) for -10V to +10V, instead of -32768 to +32767 (signed 16 bit).

Anyone watching actual data transactions between the FPGA and the DAC should keep this translation in mind. The translation formula is:

```
Actual DAC Data = not(Programmed DAC Data) + 0x8001
```

Any carry bit resulting from this calculation is dropped.

Exception: Programmed DAC Value 0x8000 maps directly to 0xFFFF. Otherwise, the single case of -10.0000V would come out as 10.0000V.

Translation examples:

Programmed Output Voltage	Programmed DAC Data	Actual DAC Data	DAC Output	Board Output
9.9997V	0x7FFF	0x0001	-9.9997V	9.9997V
0.0000V	0x0000	0x8000	0.0000V	0.0000V
-0.0003V	0xFFFF	0x8001	0.0003V	-0.0003V
-9.9997V	0x8001	0xFFFF	9.9997V	-9.9997V
-10.0000V	0x8000	0xFFFF	9.9997V	-9.9997V

For diagnostic purposes, the actual DAC data is made available, read-only.

Channel 0 Actual DAC Data: Word32 Offset 0x0000

This register returns the actual, post-translation data programmed into the DAC.

Channel 0 Actual DAC Data

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 0 DAC Data (0 – 65535)

Channel 1 Actual DAC Data: Word32 Offset 0x0001

This register returns the actual, post-translation data programmed into the DAC.

Channel 1 Actual DAC Data

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 1 DAC Data (0 – 65535)

Channel 2 Actual DAC Data: Word32 Offset 0x0002

This register returns the actual, post-translation data programmed into the DAC.

Channel 2 Actual DAC Data

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 2 DAC Data (0 – 65535)

Channel 3 Actual DAC Data: Word32 Offset 0x0003

This register returns the actual, post-translation data programmed into the DAC.

Channel 3 Actual DAC Data

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 3 DAC Data (0 – 65535)

7. Front Panel LEDs

The front panel LEDs are mapped to LED_DATA_0_BASE. Writing 0 to any of these bits will turn that LED on. The LED register is write-only.

Front Panel LEDs

Bits	Bit Definitions
31:8	Reserved
7	Heartbeat
6	Ramp 0 Enabled
5	Ramp 1 Enabled
4	Ramp 2 Enabled
3	Ramp 3 Enabled
2	LAM
1	Reserved for MDAT Present
0	TCLK Present

8. Power Supply Status

The 32 digital power supply status inputs (4 channels x 8 bits) are read here. Power supply status is mapped to PS_STATUS_0_BASE.

Power Supply Status

Bits	Bit Definitions
31:24	Power Supply 3 Status
23:16	Power Supply 2 Status
15:8	Power Supply 1 Status
7:0	Power Supply 0 Status

9. CAMAC Interface
The CAMAC interface is mapped to CAMAC_IF_OFFCHIP_0_BASE.

Read CAMAC R[16:1]: Word32 offset 0x0000 (Read)
Reading address offset 0x0000 will capture data from the CAMAC R bus (R[16:1]). Reading this address will clear the CAMAC Interface interrupt.

Bits	Bit Definitions
31:16	Reserved
15:0	CAMAC R[16:1]

Set CAMAC W[16:1]: Word32 offset 0x0000 (Write)
Writing address offset 0x0000 will set data on the CAMAC W bus (W[16:1]). Writing this address will clear the CAMAC Interface interrupt.

Bits	Bit Definitions
31:16	Reserved
15:0	CAMAC W[16:1]

Capture Function and Subaddress (F/A): Word32 offset 0x0002 (Read)
Reading address offset 0x0002 will capture the state of the F and A CAMAC dataway signals. Reading this address will clear the CAMAC Interface interrupt for Functions 9 – 31. Reading this address will have no effect on the state of the CAMAC Interface interrupt for Functions 0 – 8.

Bits	Bit Definitions
31:9	Reserved
8	F16
7	F8
6	F4
5	F2
4	F1
3	A8
2	A4
1	A2
0	A1

Clear Invalid Interrupt: Word32 offset 0x0002 (Write)
Writing address offset 0x0002 will clear the CAMAC interrupt, and no Q will be sent back to the CAMAC controller. Use this to clear an interrupt if an invalid Function or Subaddress is given, or if any other error occurs that does not allow the system to complete the CAMAC command.

Bits	Bit Definitions
31:0	Unused. Data will be ignored.

Set/Clear Look-At-Me (LAM): Word32 offset 0x0003 (Write)
Writing address offset 0x0003 will set the LAM CAMAC Dataway signal.

Bits	Bit Definitions
31:2	Unused. Data will be ignored.
1	LAM Mask 1 = Enable LAM 0 = Disable LAM
0	Logic state to set LAM to 1 = TRUE (Low) 0 = FALSE (High)

10. FPGA Version (FPGA_VERSION.VHD)

The FPGA version is contained in a small module dedicated to this purpose only. The module is mapped to FPGA_VERSION_0_BASE.

FPGA Version

Bits	Bit Definitions
R16:R9	Major Revision
R8:R1	Minor Revision

I/O Connections

NOTE: Power supply reference designators are listed in this table as 1 through 4 to match other documentation. Elsewhere in this document, all channel numbers are reference 0 through 3.

Viking Connector, 'A' Board

Terminal	Function
1L	MDAT Digital Gnd
1R	TCLK Digital Gnd
2L	TCLK Output
2R	TCLK Input
3L	MDAT Output
3R	MDAT Input
4L	TTL Output - Enable Supply 1
4R	TTL Output - Reset Supply 1
5L	TTL Output - Enable Supply 2
5R	TTL Output - Reset Supply 2
6L	Digital Gnd
6R	Digital Gnd
7L	TTL Output - Enable Supply 3
7R	TTL Output - Reset Supply 3
8L	TTL Output - Enable Supply 4
8R	TTL Output - Reset Supply 4
9L	Opto Anode Supply - 5 Volts provided by Supply 1
9R	Status Input 1-1 - (pull low for active state)
10L	Status Input 1-2
10R	Status Input 1-3
11L	Status Input 1-4
11R	Status Input 1-5
12L	Status Input 1-6
12R	Status Input 1-7
13L	Status Input 1-8
13R	Interlock Input 1 (Ignored)
14L	Opto Anode Supply - 5 Volts provided by Supply 2
14R	Status Input 2-1 - (pull low for active state)
15L	Status Input 2-2
15R	Status Input 2-3
16L	Status Input 2-4
16R	Status Input 2-5
17L	Status Input 2-6
17R	Status Input 2-7
18L	Status Input 2-8
18R	Interlock Input 2 (Ignored)

Viking Connector, 'B' Board

Terminal	Function
1L	Analog Reference Output 1
1R	Analog Reference Ground 1
2L	Analog Current Readback 1
2R	Analog Bias Input 1
3L	Analog Reference Output 2
3R	Analog Reference Ground 2
4L	Analog Current Readback 2
4R	Analog Bias Input 2
5L	Analog Reference Output 3
5R	Analog Reference Ground 3
6L	Analog Current Readback 3
6R	Analog Bias Input 3
7L	Analog Reference Output 4
7R	Analog Reference Ground 4
8L	Analog Current Readback 4
8R	Analog Bias Input 4
9L	Opto Anode Supply - 5 Volts provided by Supply 3
9R	Status Input 3-1 - (pull low for active state)
10L	Status Input 3-2
10R	Status Input 3-3
11L	Status Input 3-4
11R	Status Input 3-5
12L	Status Input 3-6
12R	Status Input 3-7
13L	Status Input 3-8
13R	Interlock Input 3 (Ignored)
14L	Opto Anode Supply - 5 Volts provided by Supply 4
14R	Status Input 4-1 - (pull low for active state)
15L	Status Input 4-2
15R	Status Input 4-3
16L	Status Input 4-4
16R	Status Input 4-5
17L	Status Input 4-6
17R	Status Input 4-7
18L	Status Input 4-8
18R	Interlock Input 4 (Ignored)