R24: Large Format CCD Image Sensors Fabricated on High Resistivity Silicon

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Abstract

We report the development of large format charge coupled device (CCD) image sensors fabricated on high resistivity, float-zone refined silicon. Previous prototype devices demonstrated much better near-infrared sensitivity when compared to existing CCD's, and good blue response was achieved with back illumination. Full depletion of a 300 μm thick substrate resulted in the improved near-infrared quantum efficiency. However, the small size of the prototype CCD (200 $\times$ 200) did not adequately address all key parameters regarding the expected performance of large format devices on fully depleted, high-resistivity silicon. In this work we describe initial results on the fabrication and testing of large format devices, the largest a 2048 $\times$ 2048, (15 μm)^2 pixel CCD.

1. Introduction

The large focal planes at astronomical telescopes require high quantum efficiency (QE), large format CCD detectors. Many science programs, such as the Supernova Cosmology Project [1] based at Lawrence Berkeley National Laboratory (LBNL), require imaging large areas of the sky in order to find rare events. Mosaic cameras, consisting of multiple large format CCD's, are necessary for efficient searches.

In order to achieve high quantum efficiency, the standard scientific CCD is thinned and back illuminated. Thinning is required because the relatively low resistivity silicon used to fabricate scientific CCD's limits the depth of the depletion region. In order to minimize field-free regions with resulting degradation in spatial resolution, the typical scientific CCD is thinned to about 20 μm. This process is expensive, degrades red response, and results in fringing in the near infrared where the absorption depth of the light becomes comparable to the CCD thickness.

Extended red response is extremely important to the Supernovae Cosmology Project due to the use of distant, high redshift supernovae for the determination of cosmological parameters. Detection and follow-up spectroscopy of high redshift objects would greatly benefit from CCD's with improved near-infrared response.

We have reported results on a small prototype CCD with high QE extended to 1000 nm [2, 3]. The device is a spin off of high-energy physics detector development at LBNL. By fabricating the device on high-resistivity silicon and applying a back-side bias voltage, full depletion of a 300 μm thick substrate with excellent near-infrared response has been demonstrated. In contrast, MOS CCD's developed in support of the major x-ray astronomy missions Chandra (AXAF) and XMM have typically 40–80 μm thick depletion regions, due to the use of more highly doped starting silicon and the lack of a back-side bias voltage [4, 5, 6]. The XMM mission also includes a fully depleted, 300 μm thick pn junction CCD [7]. In its present form the pn junction CCD has large pixels, (150 μm)^2, and requires two-sided lithography. The CCD reported here uses standard fabrication technologies.

In addition to good near-infrared response, we have developed a thin back-side contact technology that results in good blue response without the need for thinning [2, 8]. Spatial resolution, a concern for such a thick active volume, is controlled by the back-side bias voltage, and standard deviation values of about 10 μm have been achieved at a bias voltage of 33 V and a temperature of $-120°$C [9].

However, the small size of the prototype, 200 $\times$ 200 with (15 μm)^2 pixels, did not allow for the demonstration of science-quality charge transfer efficiency, nor did it address in any significant way yield issues related to fabrication of large area devices on high-resistivity silicon. In this work we report the initial results from a fabrication run of large format CCD's, up to a factor of 100 larger than the prototype device.

2. Technology

The CCD's are fabricated in a conventional triple polysilicon, single metal, 10 mask process. The majority of the processing is carried out at the LBNL MicroSystems Laboratory, a Class 10 clean room dedicated to high-resistivity silicon processing.

The CCD's are p-channel devices fabricated on n-type, high-resistivity silicon. The starting material is $> 10{,}000$ Ω-cm, float-zone refined silicon manufactured by Wacker Siltronic Corporation.

The gate dielectric consists of 50 nm of thermally grown

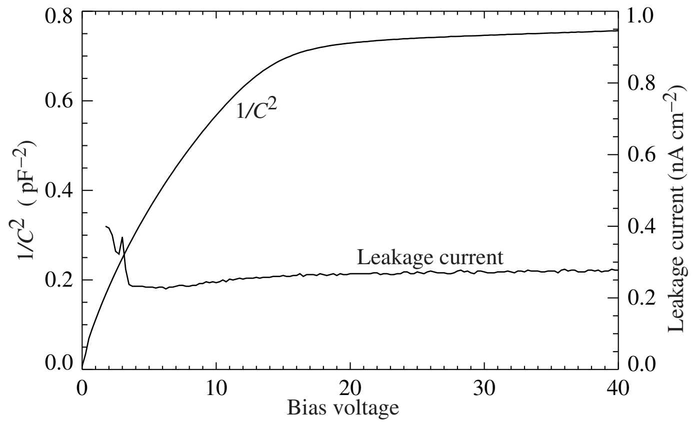

Figure 1: Inverse square capacitance and reverse leakage current measured at room temperature on a 2 mm^2 p-i-n diode test structure from a CCD wafer.

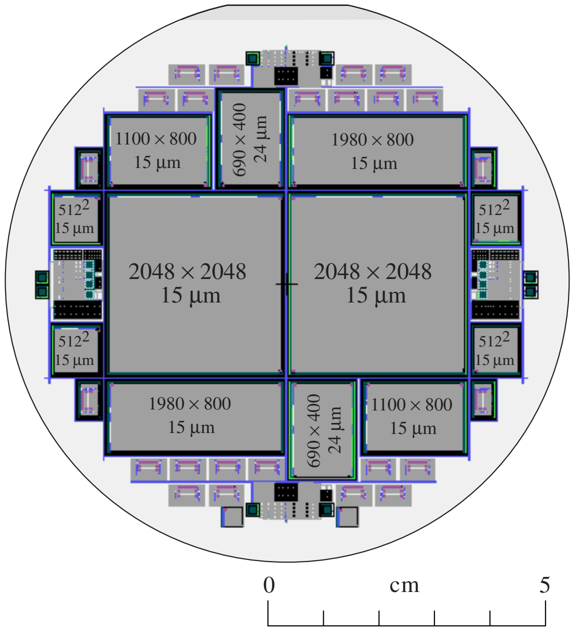

Figure 2: Mask layout used in this work.

SiO_2 capped by 50 nm of Si_3N_4 deposited by low-pressure chemical vapor deposition. The CCD channel is implanted with boron at a dose of 1–1.5$\times10^{12}$ cm^{-2}. A new feature of this run is a notch implant, used to improve charge transfer efficiency for low signal levels [10]. This 3 μm wide implant is placed in the serial register, which is relatively wide in order to allow for on-chip binning. The dose is 0.5 $\times10^{12}$ cm^{-2}.

Conventional CCD processing requires relatively high temperatures for such steps as polysilicon oxidation and implant anneals. A concern for high resistivity silicon processing is the introduction of undesired impurities that could affect dark current and resistivity. Given that 10,000 Ω-cm corresponds to a purity level of one part in 10^{11}, care must be taken during processing to achieve low dark currents. Key to this development is the use of efficient gettering. This is achieved by depositing approximately 1 μm of in-situ phosphorus doped polysilicon on the wafer back side near the beginning of the process [11]. A Si_3N_4 capping layer prevents oxidation of the gettering layer, which allows for efficient gettering during all high temperature processing.

For conventional p-i-n diode detectors such as those used in high-energy physics, the n^+ back-side gettering layer acts as the ohmic contact of the device. However, for back illumination this thick layer is removed and replaced by a much thinner layer in order to achieve good blue response [2, 8].

Figure 1 shows measured dark current and inverse square capacitance measured on a 2 mm^2 p-i-n diode test structure that is included on the CCD wafers. This wafer went through the entire CCD process, including the removal of the thick back-side polysilicon and replacement by a ~20 nm thick film. Several 950°C furnace steps are used in the process. The dark current at room temperature is about 0.3 nA/cm^2, and does not increase significantly for bias voltages above that necessary for full depletion, where the $1/C^2$ curve flattens out. The nominal thickness of this wafer is 280 μm.

The relatively low levels of oxygen in high resistivity, float-zone refined silicon make the material more susceptible to dislocation generation, which can lead to dark current and trapping problems [12]. All high temperature furnace steps in this process minimize thermal shock to the wafers by using slow, well controlled temperature ramp rates.

3. Experimental results

The 200 × 200 prototype CCD was fabricated using a wafer stepper, which limits the device size to the field size of the stepper, about 1.4 cm square. Although stitching has been used for large format development [6, 13], for both simplicity in mask design and flexibility in the number of CCD variants possible on one wafer we choose to fabricate the large format arrays using scanner lithography. This was facilitated by the acquisition, via donation from Intel Corporation, of a Perkin Elmer 641 aligner. Figure 2 shows the mask layout used to fabricate large format devices on 100 mm diameter wafers.

Both (15 μm)^2 and (24 μm)^2 pixel CCD's are included, with the largest device having 2048 × 2048 (15 μm)^2 pixels. The first wafer from this fabrication run was processed with the thick back-side polysilicon, and serves as a reference for subsequent back-illuminated devices. CCD's from this wafer were mounted for front illumination on a universal printed circuit board that could accommodate most of the CCD designs shown in Figure 2. These CCD's feature a split serial register, allowing for operation with one or two amplifiers, and a split vertical register for use in either frame transfer or frame store mode. The CCD's are tested cold, at typically −120°C. So far the 400 × 690, (24 μm)^2 and 2048 × 2048, (15 μm)^2 pixel CCD's have

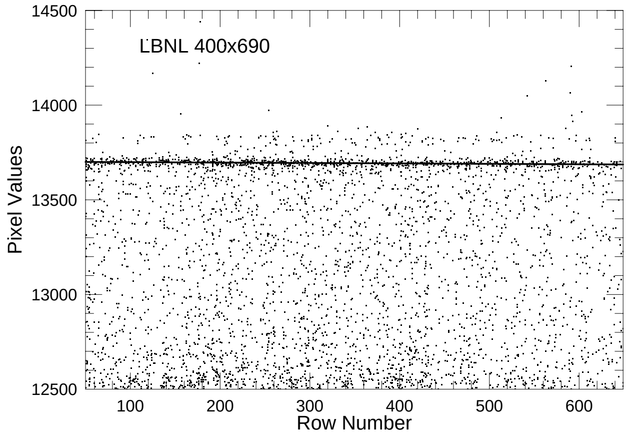

Figure 3: ^{55}Fe charge transfer efficiency measurement on a 400×690, $(24\ \mu\mathrm{m})^2$ pixel CCD.

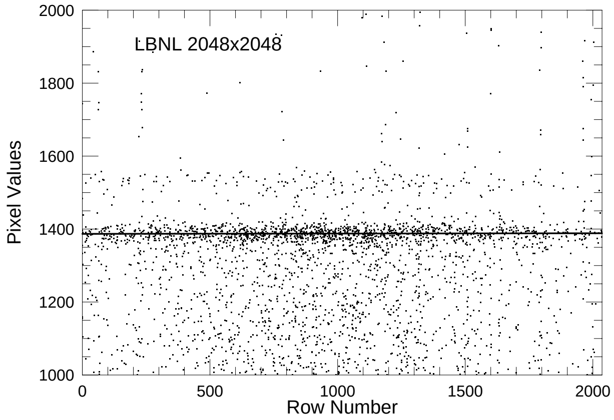

Figure 4: ^{55}Fe charge transfer efficiency measurement on a 2048×2048, $(15\ \mu\mathrm{m})^2$ pixel CCD.

been characterized at Lick Observatory.

As mentioned previously, one important parameter that was not well demonstrated on the 200×200 prototype CCD was charge transfer efficiency (CTE), defined as [14]

$$\mathrm{CTE} = 1 - \frac{Q_L}{Q_S N_P} \tag{1}$$

where Q_S in electrons is the charge produced by an ^{55}Fe x-ray event, and Q_L is the charge loss in electrons after N_P pixel transfers. Figures 3 and 4 show measured vertical CTE for both the 400×690, $(24\ \mu\mathrm{m})^2$ and 2048×2048, $(15\ \mu\mathrm{m})^2$ pixel CCD's. In both cases the CTE is basically indistinguishable from 1 (> 0.999995). Similar results are found for serial CTE.

The output amplifier for these CCD's consists of a single-stage source follower. The output transistor has a width to length ratio of 47/6, with a 1.5 μm gap between gate and drain to minimize overlap capacitance [15]. Figure 5 shows the measured noise for this amplifier versus the sample time of the correlated-double-sampler circuitry. At the longest sample time measured (8 μsec) the noise is 4.3 e$^-$ rms. The noise varies approximately as inverse square root of sample time, implying that the performance is white-noise limited over this range of sample time [14].

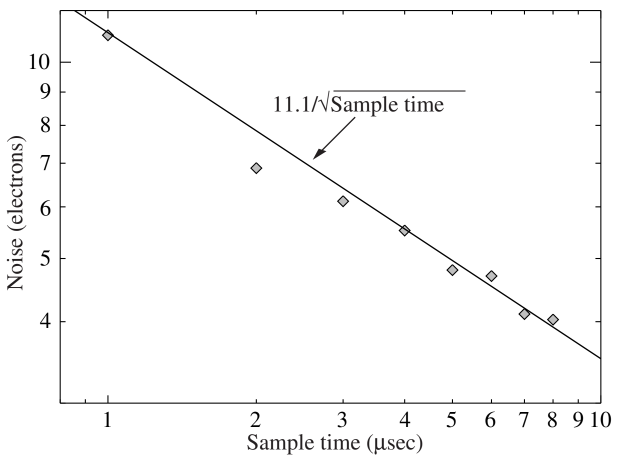

Figure 5: Noise in electrons versus sample time for the single-stage source follower amplifier on the 400×690, $(24\ \mu\mathrm{m})^2$ CCD. The CCD output is processed by a correlated-double-sampling circuit.

Dark current at $-133°$C was 11.8 e$^-$/pixel/hour for the 400×690, $(24\ \mu\mathrm{m})^2$ pixel CCD. Dark current was allowed to accumulate for 2000 seconds with the camera shutter closed. This was measured at a substrate bias voltage of 80V, a factor of 4 or so above what is needed for full depletion. Hence the front-side illuminated technology with thick back-side polysilicon contact is very robust in terms of the amount of over-voltage that can be applied to the substrate, with implications for spatial resolution where the standard deviation of the charge diffusion goes as (substrate bias voltage)$^{-0.5}$ [9]. Based on the result shown in Figure 1, we also expect good over-voltage performance for back-illuminated CCD's. No evidence of dislocations was observed after a 3000 second dark exposure, although more testing is required to determine the extent of the dislocation problem.

Full well capacity was measured by imaging a test pattern onto the CCD and determining the light level at which blooming occurred. A value of $\sim$320 ke$^-$ was measured on the $(15\ \mu\mathrm{m})^2$ pixel, 2048×2048 CCD. Nonlinearity in the amplifier was noted at $\sim$240 ke$^-$.

Quantum efficiency was measured on a front-illuminated 2048×2048 CCD using narrow-band filters. The QE peaked at a value of 56% at 900 nm, and was 39% at 1 μm. Our intent is to use back illumination, and evaluation of the first back-illuminated CCD's from this fabrication run is in progress. The predicted QE with back illumination and a two-layer AR coating is discussed in reference [16].

Figure 6 shows test pattern images taken with the 2048×2048 CCD. The CCD is cosmetically good, with only two bad columns.

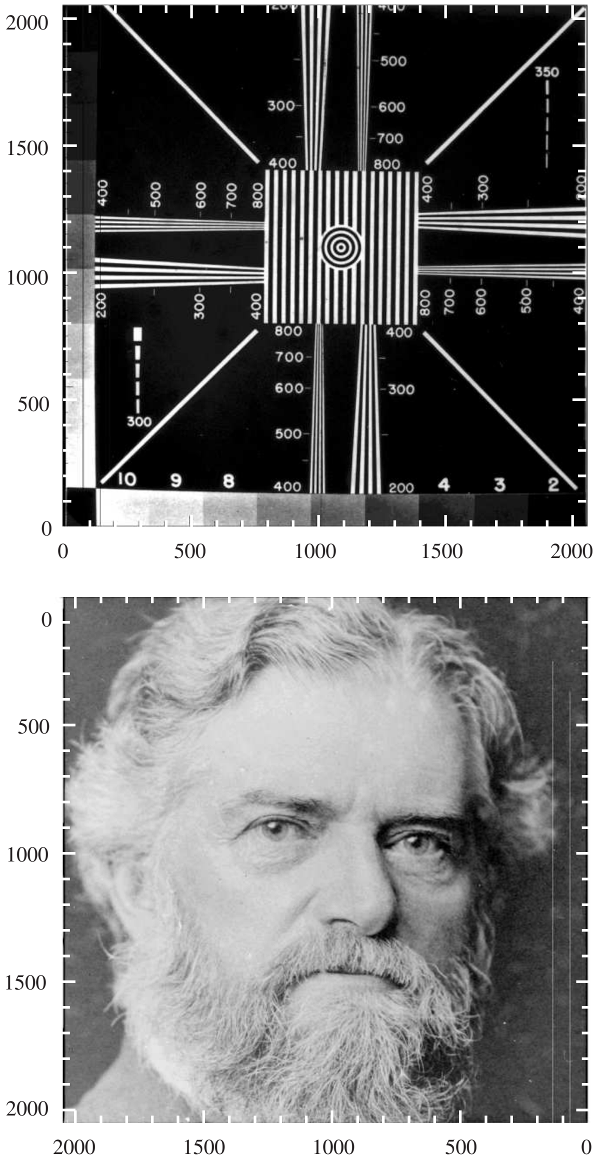

Figure 6: Test pattern images taken with the 2048 $\times$ 2048 CCD. The CCD was front illuminated.

4. Conclusions

Several important milestones in the fully depleted CCD development have been achieved. Scientific quality charge transfer efficiency has been demonstrated on a 2048 $\times$ 2048 CCD, as well as acceptable cosmetic quality. Noise, dark current and full well have been measured and are adequate for most science applications. The results presented are for front-illuminated CCD's, and it remains to demonstrate scientific quality performance on back-illuminated devices. Nonetheless, the front-illuminated device has much better quantum efficiency at near-infrared wavelengths than existing CCD's, and back-illuminated devices are expected to have excellent quantum efficiency.

Acknowledgments

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