Active Pixel Sensors: Are CCD's Dinosaurs?

Eric R. Fossum

Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, California 91109 USA

ABSTRACT

Charge-coupled devices (CCD's) are presently the technology of choice. for most imaging applications. in the 23 years since their invention in 1970, they have evolved to a sophisticated level of performance. However, as with all technologies, we can be certain that they will be supplanted someday. in this paper, the Active Pixel Sensor (AI'S) technology is explored as a possible successor to the CCD.

An active pixel is defined as a detector array technology that has al least one active transistor within the pixel unit cell. The AJ'S eliminates the need for nearly perfect charge transfer -- -the Achilles' heel of CCDs. This perfect charge transfer makes CCD's radiation "soft," difficult to use under low light conditions, difficult to manufacture in large array sins, difficult to integrate with on-chip electronics, difficult to use at low temperatures, difficult to use at high frame rates, and di fficult to manufacture in non-silicon materials that extend wavelength response. With the active pixel, the signal is driven from the pixel over metallic wires rather than being physically transported in the semiconductor.

This paper makes a case for the development of APS technology. The state of the art is reviewed and the application of A1'S technology to future space-based scientific sensor systems is addressed.

1. INTRODUCTION

The charge-coupled device (CCD), while presently the imager technology of choice in scientific applications, is a dinosaur doomed to extinction. The likely successor to CCD technology is the Active Pixel Sensor (APS) technology, just emerging in the most advanced imager laboratories in Japan for application to high-definition television (HDTV) and electronic still cameras. While APS technology is still in its infancy, it is easy to extrapolate to the demise of CCDs. The AI'S technology preserves all the desirable features of CCDs, yet circumvents the major weaknesses of CCD technology.

The Achilles' heel of CCD technology is fundamental to its operation -- -the need for the perfect transfer of charge across macroscopic distances through a semiconductor. Although CCDs have become a technology of choice for present-day implementation of imaging and spectroscopic instruments due to their high sensitivity, high quantum efficiency, and large format, it is well-know that they are a particularly difficult technology to master. The need for near-pc]fect charge transfer efficiency makes CCDs (1) radiation "soft," (2.) difficult to reproducibly manufacture in large array sizes, (3) incompatible with the on-chip electronics integration requirements of miniature instruments, (4) difficult to extend the spectral responsivity range through the use of alternative materials, and (5) limited in their readout rate. A new imaging sensor technology that preserves the positive attributes of the CCD yet eliminates the need for charge transfer could quickly eclipse the CCD.

Continued advancement in microlithography feature size reduction for the production of semiconductor circuits such as DRAMs and microprocessors since the invention of the CCD in 1970 enables the consideration of a new image sensor technology, called the Active Pixel Sensor (APS). In the new APS concept, one or more active transistors are integrated into the pixel of an imaging detector array, and buffer the photosignal as well as drive the readout lines. At any instant, only one row is active, so that power dissipation in the APS is less than that of the CCD. The physical fill-factor of the APS can be approximately 50% or higher, and the use of on-chip microlenses or binary optics can increase the effective fill-factor to over 80%. Sensitivity, read noise, and dynamic range are similar to the CCD. Thus, the APS preserves the high performance of the CCD but eliminates the need for charge transfer.

The APS concept represents a significant revolution in scientific image acquisition. Since CCDs are used ubiquitously in imaging and spectroscopic instruments, the benefits of a technology not susceptible to the shortcomings of CCDs described above can be immense. This technology can enable a large step in the miniaturization of instrument systems by allowing a high degree of electronics integration on the focal-plane. Since the AT'S technology allows ranciom-access (window-interest) capability, new guidance and navigation sensors can be envisioned.

This paper explores APS technology. The limitations of CCDs due to the requirement for nearly perfect charge transfer are discussed. Related technologies to APS such as photodiode arrays, cbarg,c-injection devices, and hybrid infrared focal-plane arrays are also discussed. The APS concept is then introduced. Both lateral and vertical configurations are described. The advantages of AI'S technology is summarized, The state of the art of APS technology development is then addressed. CMD, BCMD, SIT, and other device structures are reviewed. Finally, applications of AT'S technology to projected NASA mission needs are described.

2. BACKGROUND

2.1 What's wrong with CCDs

The charge-coupled device (CCD), an electronic analog, shift register, was invented in 1970. In the intervening 23 years, the CCD has become the primary technology used in scientific image sensors. The details of CCD technology are complex, even for students of semiconductor device physics. It is not possible to provide a complete description of CCD operation in this paper, but the interested reader is referred to texts such as that by Yang[1] or Tompsett[2]. The virtues of the CCD include its high sensitivity, high fill-factor, and large formats. The high sensitivity arises from a high net quantum efficiency of the order of 40%, the high fidelity of reading out the CCD, and the low noise output amplifier. Typical output amplifier noise is of the order of S electrons r.m.s. due to the low capacitance of the output sensing node. The high fill-factor of a CCD pixel (80%-100%) is due to the fact that the MOS photodetector is also used for the readout of the signal. The large format Of CCDs (typically' 1024x1024, and as high as 4096x4096[3]) has been enabled by the concurrent drive of the semiconductor memory business to improve silicon wafer quality and fabrication yield,

Even as the scientific CCD has become the baseline detector technology for visible imaging and spectrometer systems, its weaknesses have also gained in importance and driven the development of alternative imaging technologies, with the high performance CCD as a benchmark

The Achilles' heel of CCDs is fundamental to the CCD operating principle -- the need for nearly perfect charge transfer. The CCD relies on the transfer of charge (usually electrons) from under one MOS electrode to the next through sequencing of voltages 011 the electrodes. The electrons are transported through the bulk silicon material macroscopic distances (e.g., centimeters) before they reach the output sense node. A typical CCD has three electrodes per pixel, so that in a 1024 x 1024 imager, the electrons may be shifted, 011 the average, several thousand times. The ratio of electrons successfully transferred to number left behind per electrode is the charge transfer efficiency (CTE). The CTE needs to be as close as possible to perfect to enable scientifically acceptable performance of the CCD. If the CTE is given by η, the net fraction of signal transferred after n transfers is simply η^n, As shown in the table below, the CTE must be very high.

Table 1. CCD Fidelity vs. CTE

ARRAY SIZE	CTE	FRACTION AT OUTPUT
1024x IO24	0.999	0.1?8
	0.9999	0.815
	0.99999	0.980
2048x2048	0.99999	0.960
4096x4096	0.99999	0.921
8192X8192	0.99999	0.849

Typical scientific CCDs have a CTE of 0.99999and a representative number of electrons in a scientific CCD signal packet is J,000. For a CTE of 0,99999, this means only one electron can bc lost every 100 transfers! Since. a single broken bond in the silicon crystal can (and usually will) capture a signal electron, the need for perfect silicon crystal quality is the major weakness of the CCD.

The need for }ml-feel transfer efficiency has a great impact on the viability of CCDs for future space missions. The five major issues are (1) the radiation softness of CCDs, (2) a difficulty to achieve large array sizes, (3) an incompatibility of CCDs with the requirements for instrument miniaturization, (4) difficulty in increasing the spectral responsivity range of CCDs, and (5) difficulty in increasing the readout rate of CCDs. These issues arc described below.

Radiation softness

CCDs suffer from both ionizing and displacement damage. ionizing, damage affects the oxide, and is not considered critical since processes that harden the oxide against ionization damage arc well known. On the other hand, *displacement damage caused by high energy particles and photons is deadly to CCDs.* Particularly damaging arc protons in the few hundred keV range. A single 250 keV proton causes an average of J O silicon lattice displacements[4], though higher and lower energy protons can be less damaging. If all radiation consisted of 250 keV protons, then 1 krad corresponds to a fluence of approximately J 25,000 protons/cm^2, or for a 1024x IO24 CCD with 20 micron pixels, approximately 5 electron traps per pixel. Fortunately, only a fraction of the (post-shielding) protons fall in this maximum damage regime, so that the actual dose tolerance of a 1024X1O24 CCD is about 10 krads. For future orbiter missions around Jupiter and Saturn, the. use of CCD technology is tenuous at best. Certain car(h-observing orbits can also result in high dose rates. Future spacecraft with nuclear propulsion systems arc expected to generate high radiation dose rate environment.s. It should be noted that the radiation tolerance of a CCD gels worse as the sensor format gets larger since more transfers arc required to deliver the signal electrons to the output amplifier.

Difficulty to achieve large array.sizes

Since the net transfer efficiency goes exponentially with number of transfers (η^{m}), it is obvious that as CCD array sizes grow larger, the requirement on transfer efficiency becomes more stringent. To compensate, readout rate must be decreased, but scientific CCDs are already slow to read out (50 kpixcls/see, or ?0 seconds per frame for a 102 LJxIO?4 CCD). '1 he radiation dose tolerance decreases with increased array size as described above. *The manufacturing yield decreases as the array* size *grows, particularly since CCDs are highly vulnerable to single point defects that can block an entire column.* This is why only one or two 4096x4096 CCD ICs have actually been demonstrated, and they had numerous defects. The drive power requirement for CCDs also grows with array size since CCDs arc capacitive in nature, and the entire CCD must be driven to achieve the output of a single pixel.

Incompatibility with miniature instrument requirements

Instrument miniaturization will require highly integrated, low-power sensor electronics. This will, in turn, require on-chip timing and driver electronics, as well as cm-chip signal chains and perhaps analog-to-digital conversion for the image sensor. The CCD device structure is not easily integrable with CMOS. Furthermore, CCDs typically require high and varied voltages, also incompatible with low-power CMOS electronics. Operating on-chip devices with high voltages can cause emission of infrared radiation that is detected by the imager, contaminating the image. While it is possible that first-generation miniature instruments may utilize CCDs with off-chip electronics, the future of smart miniature imaging and spectrometry instruments will requite a more tractable technology.

Extension of spectral range

Future astrophysics and planetary instruments will benefit from large, monolithic detector arrays that extend the nominal 0.4 - 1.0 micron spectral range of CCDs. Increasing the spectral responsivity range of CCDs requires the utilization of materials other than silicon, and/or the removal of structures integral to CCD operation. Blue, ultraviolet and soft x-ray response requires the eliminat ion of overlying electrodes that absorb higher energy photons. Backside illumination has been used on the ground with some success but the long term stability of backside illuminated CCD structures for UV

response has prevented *their* widespread usc in space instruments (an exception is the WF/PC instrument in HST and it required significant modification to apply a last minute, expensive, (albeit successful) Rube GoldbcrS-like remedy). Low-QE, low-MTF, down-converting phosphors (lumogen) deposited on the front-side of CCDs will be used on WF/PC 11. Pinned photodiode inter-line transfer CCDs have been developed by Kodak[5] and used withsome success to overcome these problems. Infrared response of silicon CCDs requires integration of infrared absorbing materials such as platinum silicide[6] m SiGe junctions[7,8]. These devices suffer from very low QE and incomplete reset resulting, in large kTC noise. Large format scientific CCDs in non-silicon materials (e.g., GaAs, InGaAs, Ge, diamond) arc unlikely to be achieved due to the relative immaturity of these materials compared to silicon, Non-CCD structures will be required to achieve monolithic, large format, scientific performance.

1 .imited readout rate

For many present and future applications, the readout rate of scient ifrc CCDs (50 kpixcls/see) is neatly too slow for practical USC. Examples include star trackers and fine guidance sensors, astrophysics and material analysis instruments requiring photon position and energy information (energy is proportional to the number of photoelectrons), and imaging systems supporting microgravity materials processing experiments on Space Station Freedom. Three to five orders of magnitude improvement in detector an ay readout rate is required, While some high speed, large format CCDs arc being developed for 1 HDTV (1900x1120 at 50 Mpixels/s), the performance of these CCDs is inferior to the competing APS t echnology, and not suitable for most scientific applications. This is because charge transfer efficiency degrades rapidly with increasing transfer rate.

Other well-knowl problems stemming from charge-transfer in CCDs includes low temperature performance degradation due to the onset of earl-icr freeze-out (e.g. an on-focal plane SIRTF fine guidance sensor operat i ng at 4K could not use a CCD, or theN41'1$ Lincoln Laboratory infrared 11 I P-CCD pet formance limited by low temperature CCD CTE[8]), and spur ious charge generation in virtual phase CCDs.

in essence then, nearly all the problems with CCDs stem from the need to efficiently transfer electrons through macroscopic distances of semiconductors. If the need to transfer the signal can be eliminated, detector array performance can be significantly be enhanced.

2.2 Related image Sensor Technologies

Photodiode Arrays

Imaging photodiode arrays predate CCDs by a fcw years[9]. Pixels contain a p-n junction, an integrating capacitor (often the p-n junction itself) and MOS selection transistors. The photodiodes on a single row arc typically bussed together on an output line with a column selection transistor connecting a single photodiode at a time to the bus. The photodiode array (the *reticon*) was one of the first solid-slate imaging devices and had large advantages over its vacuum tube predecessors. Compared to the CCD, however, the photodiode array was more complex since selection transistors had to be fabricated within each pixel, and some on-chip multiplexer circuits had to be fabricated as WC]]. Later, the noise of the photodiode a rray also became a limitation to its performance Compared to the CCD since the photodiode readout bus capacitance results in an increase in noise level. Correlated double-sampling, (CDS)[10] cannot be readily employed with a photodiode array without external memory.

Recently, a photodiode array configured for random accessibility with on-chip CMOS circuitry was reported[11]. This 80x80 prototype array was designed for random accessibility and included an in-pixel source-follo~vcr to minimize bus capacitance effects (making it an active pixel sensor as described below.) The pixel size using 3 μm CMOS design rules was 144 μm x 144 μm with a fill-factor of 6%. An estimated input referred noise level of approximately 2S0 electrons r.m.s. was reported. This noise was dominated by $(kTC)^{1/2}$ processes inherent in photodiode arrays, The architecture also is susceptible to significant tjxc.d-pattern noise and I/f noise since CDS cannot be readily applied.

Charge Injection Devices

The charge injection device (CID) was invented in the early 1 970's, a few years after the invention of the CCD[12]. The CID, unlike the CCD, requires only a single, intra-pixel charge transfer. The charge is shifted under a floating sense gate and the induced voltage change is the output signal. '1'bus, CIDs are immune to the deleterious effects of imperfect charge transfer and have been used in high radiation environments. CIDs also feature random accessibility of the pixels, high fill-factor, and good blue/U V response. Unfortunately, the CID, like the photodiode and MOS imager, suffers from high bus capacitance since the sense gates of all pixels on a given row are tied in parallel. in a recent paper, a high performance 512x51 2 CID imager was reported to have a sinp,lc-read input-referred noise level of 220 electrons r.m.s.[13]. The CID, however, can be operated in non-destructive readout mode so that multiple reads of the same signal can be per formed and averaged together. Multiple sampling results in a nearly $(1/N)^{1/2}$ reduction in read-noise level where N is the number of reads so that the input-referred read-noise level after 100 reads is reported to be 26 electrons r.m. s. The drawback of' multiple reads is an N-fold increase in readout time and a need to reduce dark current[14].

Hybrid IR FPAs

1 lybr id infrared focal-plane arrays typically consist of a detector array chip bump-bonded to a silicon readout multiplexer[15,16]. Each detector pixel has an associated unit ccl] in the multiplexer that contains an integrating capacitor, selection transistors, and usually some preamplifier of varying sophistication. For example, a capacitive transimpedance amplifier (CTIA) can be integrated within the unit ccl] to maintain constant bias on the detector and reduce low RoA effects. The separation of detector and unit cell electronics allows for separate optimization of each, and enables detector pixels with nearly 1000/' fill factor, Read noise is typically in the 30-S0 electron r.m. s. range, though multiple sampling can help reduce the noise level.[17] The major difficulty associated with hybrid IR FPA technology is the manufacturability of the hybrid. A second difficulty is that when the detector and readout multiplexer are made of differing materials, stress is induce.d by the difference in thermal expansion coefficients when the hybrid assembly is cooled. The str ess can lead to reliability concerns regarding the structure's integrity.

3. ACTIVE PIXEL SENSOR CONCEPT

The active pixel sensor (APS) technology preserves the desirable attributes of CCDs such as high sensitivity, high signal fidelit y anti large arr ay formats. The recent invention of the on-chip microlense or binary optics allows the nominal 50% fill-factor of the APS to approach to 80-90% fill factor of the CCD. The APS approach dots not require charge-transfer across macroscopic distances and thus eliminates the five negat ive major issues associated with CCD detector arrays descr ibed above.

An active pixel sensor (APS) is defined as a sensor with one or more active transistors located within each pixel, The in-pixel active transistors can provide both gain and buffering functions. Twenty years ago, an active pixel sensor with a "practical _pixel size-wias not possible due to the state-of-tl)c-alt of microlithography in the 'early 1 970's, The technological push of the semiconductor industry has driven microlithography to the sub-micron regime, and 1,25 micron CMOS is practically an industry standard. It is in the shadow of this progress that the fundamental advantage CCDs had over any other imaging technology has been eclipsed. CCDs in the 1970's were attract ive because only three electr odes were required per pixel to make them operate. A 30 micron pixel was thus possible. However, pixel size is determined more by scientific imaging opt ics in the 1990's than by microlithograp hy constraints. 'J'bus, there is a new window of opportunity to take advantage of the advances in microlithography as it continues its inevitable evolution driven by the digital microelectronics industry.

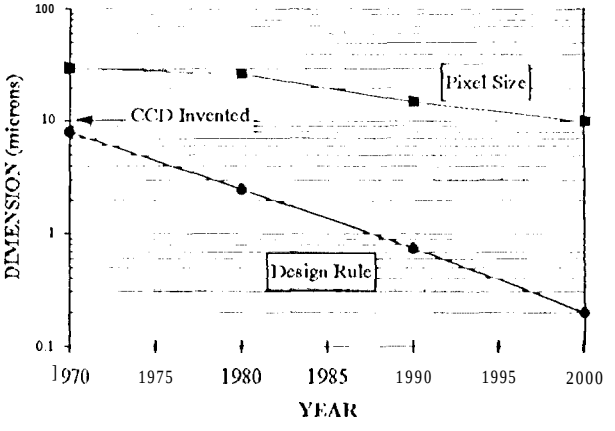

Fig. 1. 1 Evolut ion of photolithograph ic feature size vs. pixel size.

3.1 Lateral APS

A lateral APS structure is defined as onc that has part of the pixel area is used for photodetection and signal storage, and the other part is used for the active transistor. The advantage of this approach, compared to a vertically integrated APS, is that the fabrication process is simpler, and is highly compatible with state-of-the-arl CMOS and CCD device processes. A simple example of a lateral APS device compatible with CMOS is shown below in Fig. 2.

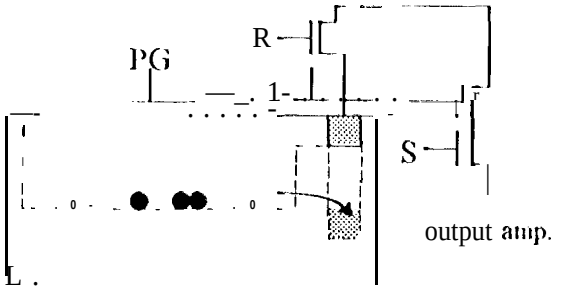

Fig. 2. Schematic ofa simple, CMOS-compatible active pixel.

in this device, charge is integrated under the photogate PG. Prior to readout, the output floating diffusion node is reset using the in-pixel reset transistor R. For readout, in-pixel selection transistor S is selected, connecting the. in-pixel source.-follo~\'cr to a column bus line. To reduce noise, the voltage of the floating diffusion node can be sensed and later used for CDS. The photosignal is then transferred from PG to into the floating diffusion node. This simple intra-pixel transfer is similar to that required for CID operation, However, unlike the CID, the capacitance represented by the floating diffusion node is very small, like that found in a CCD output amplifier, so that the charge to voltage conversion can be of the order of 10 μV/electron. Since this structure allows CDS, kTC and I/f noise can be suppressed. CDS also removes threshold voltage fixed - patteIn noise, A sample layout of this simple AI'S pixel is shown below in Fig. 3.

When implemented in commercially available 0.8 μm CMOS, the pixel size shown is 16 μm x 16 μm with a fill factor of over 50°/0. With a microlens placed over the cell (as illustrated in Fig. 3), one might anticipate a fill factor increase to over 80°/0. The spectral response of the ccl] shown will be approximately that of a standard double.-poly CCD image sensor. The noise level anticipated for this device is similar to that obtained for CCDs (3-5 electrons r.m.s.) if a buried-channc] CMOS process is used,

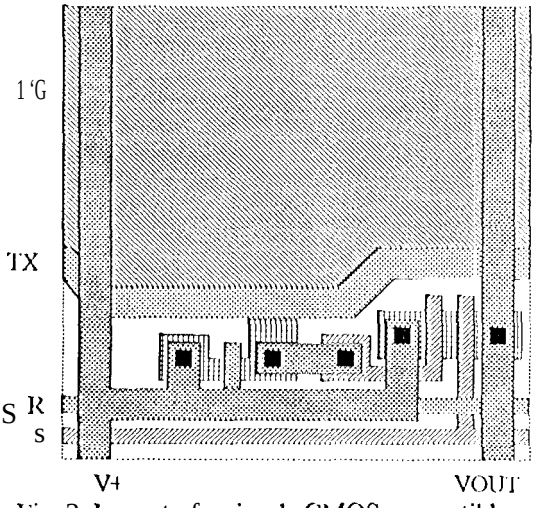

Fig. 3. Layout of a simple CMOS-compatible APS pixel.

3.2 Vertical APS

A vertical AI'S structure increases fill-factor (or reduces pixel sire) by storing the signal charge under the output transistor. Both field-effect vertical AI'S structures (CMD, FGA, BCMD) and bipolar (BASIS) AT'S structures have been developed, as described below. in the field-effect structure, the signal charge acts as a backgate bias on a lateral MOS (or JFET) transistor at the surface. In the bipolar structure, the signal charge changes the base-emitter bias of a bipolar transistor. The vertical configuration trades plfill-view complexity for vertical structure complexity.

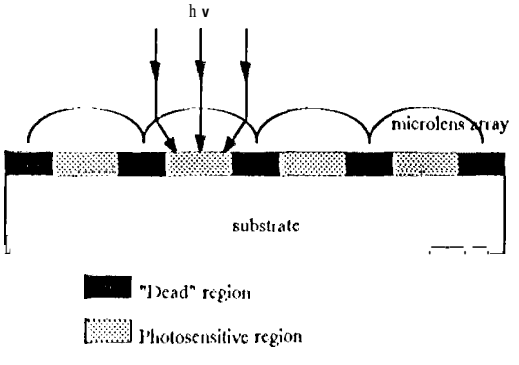

Fig. 3. Schematic illustration of on-chip microlens array to increase effective fill-factor.

3.3 Advantages of the APS

Since APS technology requires intra-pixel transfer, at most, the consequences of CCD charge transfer arc ameliorated. 'l'bus, APS

imagers can be expected to by radiation hard, operate well at lower temperatures, be fabricated in large array sizes, and be more compatible with advanced materials. It is noted that the readout of A1'S can involve either lateral transistors or vertical transistors. Vertical output has the advantage of requiring onc less surface contact and enables smaller pixels. However, it also implies a common (substrate) connection 10 all output amplifiers and thus may restrict imager architecture.

4. STATE-OF-THE-ART

In the past few years, several innovative APS technologies have been proposed and explored. Most of these act ivit ics arc centered in Japan for the development of HDTV video cameras and electronic still cameras. Mosl of the actual fabrication activities of Texas Instruments takes place in Japan as well. 'J'here arc no activities known to the author in the United Stales or Eur opc at this time. in the APS area except for some recent work at JPL.

4.1, lkmblc-gate floating surface transistor (Toshiba)

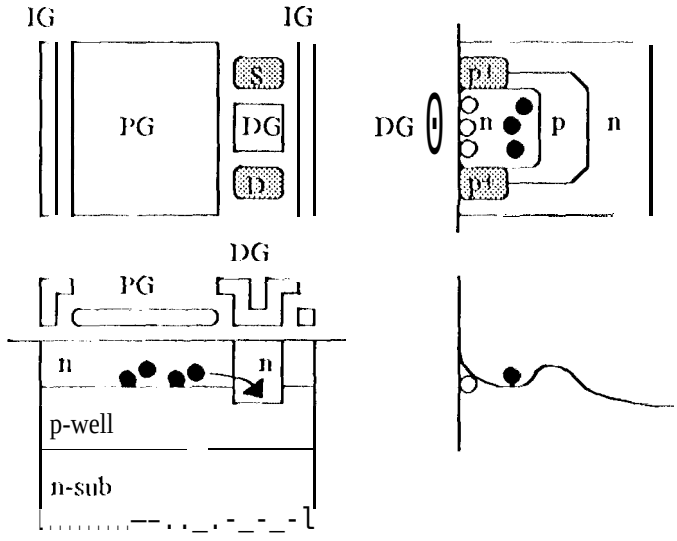

Fig. 5. Schematic illustration of Toshiba floating-surface transistor. Upper left is plan view. Upper right is a cat through output transistor. Lower right is potential in transistor. Lower left is lateral cut through plan view.

A lateral APS technology has been under development by Toshiba[18]. Termed the "double-g,atc floating surface transistor," it utilizes a readout transistor evolved from the low noise CCD output amp] ifier proposed by Brewer[19] and refined by Toshiba[20,21]. Shown schematically in Fig. S, the pixel consists of a buried-channel MOS photogate (PG) region that integrates and stores optically-gener ated electrons. The output amplifier is a surface p-channel MOSFET. The electron signal charge is transferred under the conductive p-channel to an n-doped confinement region (DG). The electrons arc confined vertically by a p-well between the stot age area and the n-substr ate. The electr cm signal charge acts as a back gate on the p-MOSFET. Readout of the Toshiba sensor is accomplished a row at a time using a charge-dcmain "line potential modulation" technique that provides charge gain and reduces the readout bandwidth requirements on individual in-pixel transistors, A sensitivity of 200 μV/e- and a charge gain of 1,100 was reported. Readout noise was reported to be 880 holes corresponding to an input-referred noise of 0.8 electrons r.m.s. The readout is non-destructive and, in principle, multiple reads could be performed to reduce white noise. The most serious problem currently facing this technology is dark fixed pattern noise (FPN) due to detection transistor potential variations, The 10 %FPN may, in principle, be reduced by reading the output amplifier twice, once following charge transfer, and once following charge ejection. The difference signal might reduce FPN and the expense of signal readout time.

4.2. Charge Modulation Device (CMD) (Olympus)

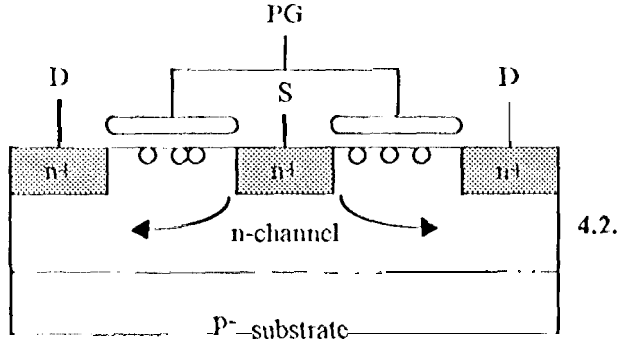

Fig. 5. Schematic illustration of Olympus CMD pixel.

The charge modulation device (CMD) imager has been under development by Olympus for several years[22,23,24,25]. It is a vertical APS and involves no charge transfer. The optical ly-generated-hole signal charge is integrated at the MOS surface. A buried n-channel MOSFET in a concentric ring configuration surrounds the collection region. The pixel size has been reduced to 7.3 μm x 7.6 μm. The presence of the surface hole charge modulates the buried n-channel MOSFET current when the transistor is selected for readout. The current is sensed by a transimpedance amplifier and converted to a voltage. The convulsion gain

was recently reported as 250 pA/hole. Dark current was 4 fA/pixel or of the order of 10 nA/cm^2, possibly reflective of the unaccumulated Si-SiO_2 surface. The shot noise of the high dark current has significant impact on total input-referred noise. Input-referred noise is estimated to be 400 holes r.m.s., but can be reduced by suppressing dark current through cooling. Fixed pattern noise is also high, corresponding to approximately 1,360 holes r.m s. and is attributed to geometric variations. Other noise sources in the output amplifier (e.g. I/f) and FPN, in principle, could be suppressed by resampling the output immediately following readout and reset,

4.3. Bulk Charge Modulation Device (Texas Instruments)

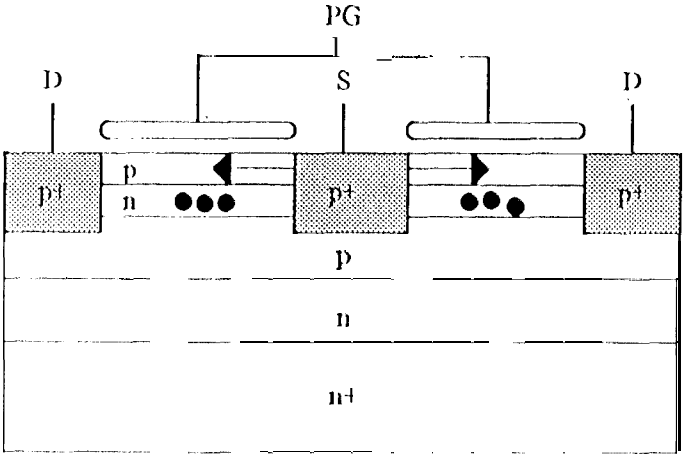

Fig. 6. Schematic illustration Texas Instruments' BCMD pixel.

The bulk charge modulated device (1 3CMD) has evolved from an initial JFET floating-gate array (FGA) sensor at Texas Instruments[26]. The JFET, while allowing high blue response, has some problems related to reset. The BCMD is an improved photosite structure and is similar in concept the CMD device described above, but is more complex and has higher performance[27]. The BCMD consists of a buried p-channel readout transistor that is backgated by signal electrons in an n-type confinement region below the readout transistor. The confinement region i s fully depleted by a vertical reset operation that damps any signal electrons over a deeper p-type barrier into the n+ subst rate, Optically generated electrons arc collected and integrated in the confinement region. The vertical APS with its complex vertical layer structure has the advantage that a low-noise buried p-channel MOSFET is used for readout. Also, surface generated dark current is collected by the FET source and drain and repelled from the confinement region. However, experimental dark current was anomalously high (1.5 nA/cm^2). The readout is voltage mode where the potential of the confinement region is translated into a source-follower output "voltage. Conversion was reported to be 15 μV/e- with a 15 electron r.m.s. input referred noise level likely dominated by dark current shot noise. Readout is row-at-a-time into a bank of storage capacitors later scanned for serial output. The image sensor was configured as a hexagonally-packed array with on-chip color filters.

4.4. Ilasc-Stored Image Sensor (BASIS) (Canon)

The base-stored image sensor (BASIS) has been under development by Canon[28,29,30]. This vertical bipolar transistor-based device consists of a p-type base layer sandwiched between an n+ emitter and a n+ collector (substrate). The base is reset to a voltage level using a clamp transistor chain and followed by capacitively coupling of the base-emitter junction into forward bias for a short period of' time. Since the base is not fully depleted, its reset voltage is susceptible to kTC noise. Opt ically generated holes flow to the p-type base where they arc integrated. During readout, the final base voltage is readout using the bipolar transistor in an emitter-follower mode onto a capacitor at the end of the column line. The cell is then reset and the reset level is sampled and stored on a second capacitor. The output signal is the di fference in voltage on these two capacitors. While this operation does not reduce kTC noise, it does suppress FPN to a very low level.

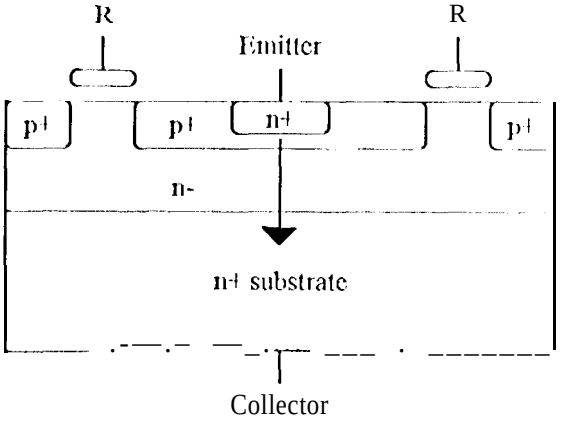

Fig. 7. Bipolar image sensor (BASI S) developed by Canon.

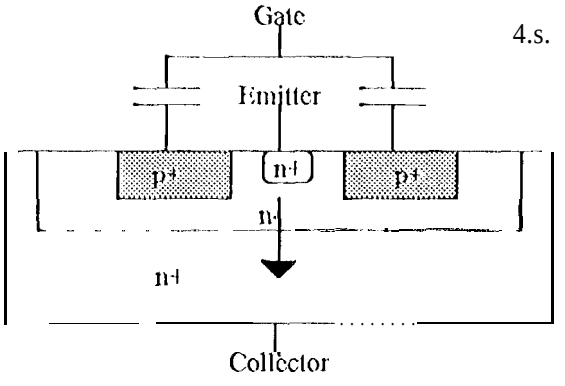

Fig. 8. Olympus S] 'I' pixel.

4.s. **Static induction** Transistor **(SIT) (Olympus)**

in addition 10 the CMD device described above, Olympus has also been developing, a static induction transistor (S1'1') image sc]mr-[31,32]. The S1'1' utilizes vertical electron current flow between the surface and substrate. Unlike diffusion transport in the base of a bipolar transistor, the electron current is controlled by a surrounding p I field-effect gate that electrostatically controls the barrier to vertical current flow. The floating p I gate is reset by forward biasing, the p I-n junction. Since the gate is not fully depleted, kTC noise is introduced in its met operation and the device is also susceptible to image lag. Image lag is significant without bias light. After reset, optically generated holes flow to the gate and change its potential. During readout, the gate is capacitively coupled to a read line and is bootstrapped to a less negative potential, thereby turning on the SIT. The S1'1' readout is in source-foltower voltage mode, row-at-a-time, onto holding capacitors. The voltage in the holding capacitors is then scanned for serial readout. The S1'1' image sensor readout is non-destructive, thereby allowing, in principle, multiple reads to reduce white noise-[33]. A reset pate could also be added to improve lag, but at the expense of pixel size.

4.6. JPL Activity

J]'], is developing a simple, CMOS-compatible, lateral AI'S to further explore the AI'S concept, The design of the CMOS APS is described in an accompanying paper[34] and is summarized here. The pixel integrates signal electrons under a MOS photogate. For readout, charge is shifted laterally to under a floating sense gate, in a fashion similar to CIDs. The floating gate voltage is buffered by an in-pixel source-follower and driven on a column line. Charge can be shifted back and forth to allow a multiple samples and reduction in I/f and white noise. By measuring the magnitude of the resultant a.c. signal, kTC noise and threshold-voltage non-uniformity-induced FPN is suppressed. The signal is fed to a X--A A/D converter located at the bottom of each column, The tall, thin A/D layout is cased by the Σ-Δ architecture that permits column-to-column non-uniformity Or components. The Σ- Δ architecture trades component precision for oversampling. The pixel design also includes a reset transistor for periodic resetting of the floating gate (e.g. every frame) and a lateral anti-blooming structure. Designed as *50* µm x *50* µm pixel with 25°A fill-faclor using an inexpensive, commercially available 2 pm CMOS process, the pixel size can be scaled to 20 µm x 20 µm by using state-of-lhc-al-t 0.8 µm CMOS processes.

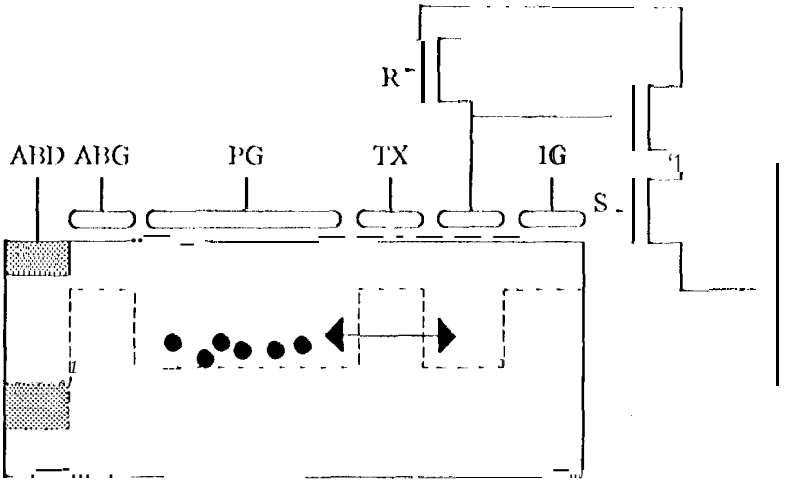

Fig. 9. JPL CMOS-compatible lateral APS.

4.7. Summary

A summary of the AI'S technologies is presented below in '1'able 2. Surveying the present technologies, it appears that lateral approaches permit low noise performance suitable for scientific applications. For consumer electronic still cameras, it is unclear which technology may emerge as a prefer red approach. HDTV requires very high pixel rates so that vertical out put approaches leading to higher current drive capability may be prefer cd,

Table 2. Summary of APS technologies.

	DGESPT	CMD	BCMD	BASIS	SIT	CMOS APS
Developer	Toshiba	Olympus	Texas Instr.	Canon	Olympus	JPL/Caltech
APS Type	Lateral	Vertical	Vertical	Vertical	Lateral	Lateral
Output	Lateral	Lateral	Lateral	Vertical	Vertical	Lateral
Pixel Size (μm)	13 x 13	7.3 x 7.6	10 x 10*	13.5 x 13.5	17 x 13.5	50 x 50
Sensitivity	200 μV/e-	250 pA/e-	15.4 μV/e-	3.5 μV/e-	0.6 μV/e-	~NIC-
Input-Referred Noise	0.8 e- rms	400 e- rms	15 e- rms	60 e- rms	69 e- rms	5 e- rms
Dynamic Range	75 dB	45 dB	72 dB	76 dB	86.5 dB	60 dB
Fixed Pattern Noise (p-p)	10 %	5 %	2 %	0.03 %	1.1 %	< 1 %
Anti-blooming	vertical	vertical	vertical	none*	none*	lateral
Lag	0	0	0	<0.1 %	70940"	0
Comments	FPN may be reducible by read/reset/re-sample	Noise dominated by dark current. Improved by cooling,	*Hexagonal layout	*Can be reduced using clippling operation.	*SIT turns on	Projected performance. Uses 2 μm CMOS design rules.

5. FUTURE DIRECTIONS

5.1. Camera-on-a-chip

There is an impetus within NASA to reduce overall mission cost. Reduction of spacecraft mass will permit the use of less expensive launch vehicles. 3'bus, there is a strong drive to develop miniature instruments that reduce mass and volume. State of the art scientific imaging systems for space-borne remote sensing instruments use CCD imagers. Presently, the power and mass of imaging subsytems arc dominated by electronics and optics, However, CCDs arc not amenable to integrating high density CMOS electronics on-chip. The APS technology being pursued by J} 'I. will ultimately lead to the realization of a scientific "camera-on-a-chip." This camera-on-a-chip will have a full digital interface. Exposure control and readout window of interest will be downloaded into the sensor. The sensor will generate all internal timing and control logic from an external clock. The sensor will output digital image data thus avoiding the need for off-chip signal chains and A/D converters and simplifying packaging and interface requirements. The incorporation of on-chip image compression processing is also possible in future imaging systems.

S.2. High speed imaging

It is believed that AT'S sensors will allow higher speed operation of image sensors than their CCD counterparts. While exposure time is ultimately limited by input photon flux and quantum efficiency (including fill factor and microlenses), the readout of the sensor typically limits high speed operation. The APS concept can be more readily extended to high speed material systems such as GaAs compared to CCD technology, since high charge transfer efficiency is no longer required, The realization of high performance image sensor architectures in materials such as GaAs should permit readout rates (per readout channel) in the range of 1-10 billion pixels/sec. I'bus, it may be possible conceive of large area image sensors operating in the multi-mega-frame per second regime.

S.3. **Extended** spectral **range**

The quest for extended spectral responsivity range in large area monolithic image sensors (e.g. UV or SWIR) has typically led to a need to develop either an amorphous material overlayer technology[35,36,37], or use internal photoemission barriers[6,8] in CCDs. Coupling the amorphous material overlayer technology with an APS readout, or implementing an APS readout in a material such as InGaAs[38] can lead to simpler, higher performance technologies.

5.4. Application **to** guidance and navigation

Guidance and navigation sensors on spacecraft presently use CCD technology. Pixel sizes in the range of ?.5 μm arc typically employed. The non-destructive readout nature of most APS technologies can be used to increase integration times for stats of interest. Window readout may simplify system electronics design. The improved radiation hardness of AI'S over the CCD is another added advantage in guidance and navigation sj'stems. The incorporation of on-chip drive and signal processing electronics can also simplify system design, reduce mass, power and volume requirements, and improve system reliability, These advantages will be discussed in a later paper[39].

5.s, Application 10 **low** light **level** sensors

1 arge CCD pixels, typically used in low light level image sensor to increase effective optical aperture, are detrimental to the transfer of charge and result in slow readout or poor readout fidelity, especially at video rates. The AT'S technology is more or less insensitive to pixel size, and yet provides high sensitivity and operation at video rates, For example, the Toshiba AI'S sensor has sub-electron read noise and high dynamic range, and is suitable for implementation as a large pixel device. The JPL CMOS AI'S is a second example of the applicability of this technology to low light level imaging. It is possible that with further improvement in read noise, APS technology may supplant microchannel plate technology in night vision goggles. The solid-state APS technology offers lower cost, simpler power suppl its, and compatibility with fut urc heads-up display technology for combat soldiers.

6. CONCI ,US1ONS

This paper has presented a discussion of the active pixel sensor (APS) technology. The problems with state-of-tllc-ar[clmt~c-coupled device (CCD) technology have been identified. It is noted that time delay and integration (TDI) sensors may continue to utilize CCDs since charge-domaill TDI dots not introduce additional noise. The APS concept was introduced and the state-of-the-art in AI'S imagers was reviewed. Future applications of APS technology were suggested. AT'S technology development is still in its infancy. However, it shows great promise for preserving the high performance of the CCD while ameliorating the undesirable effects associated with the CCD need for pet feet charge transfer. It appears likely that scientific instruments may begin to utilize APS technology by the turn of the century to increase array sizes, increase readout rate, reduce noise and reduce radiation effects.

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