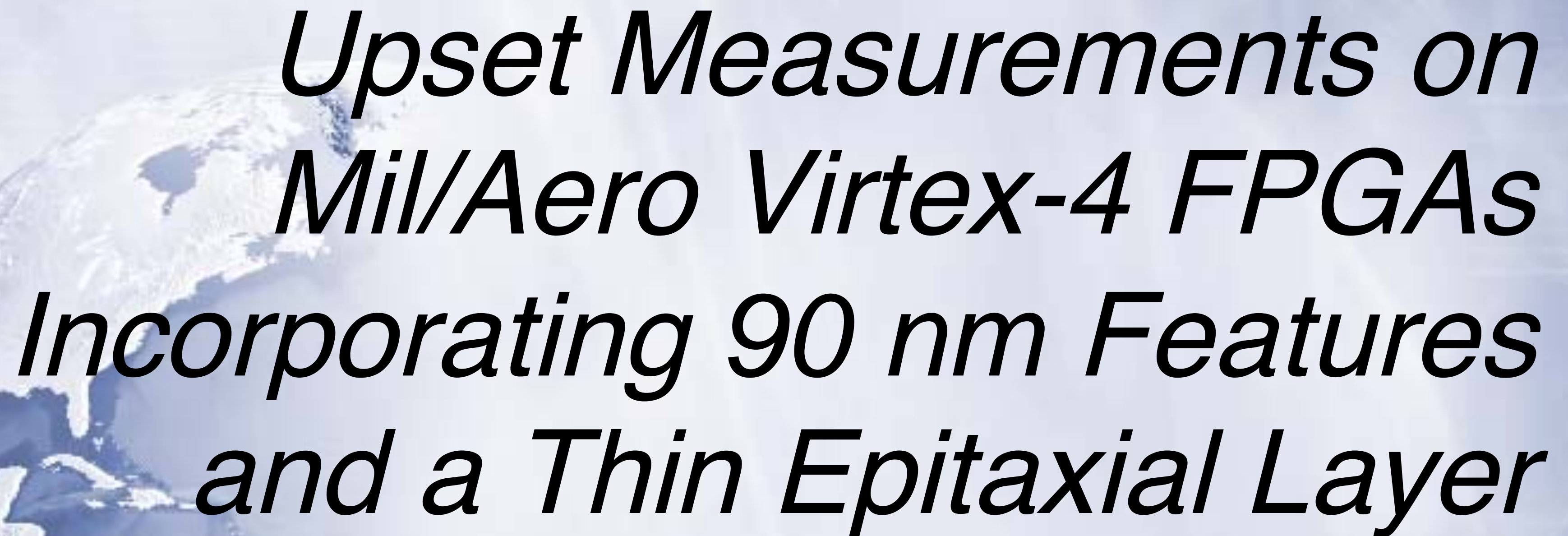

Upset Measurements on Mil/Aero Virtex-4 FPGAs Incorporating 90 nm Features and a Thin Epitaxial Layer

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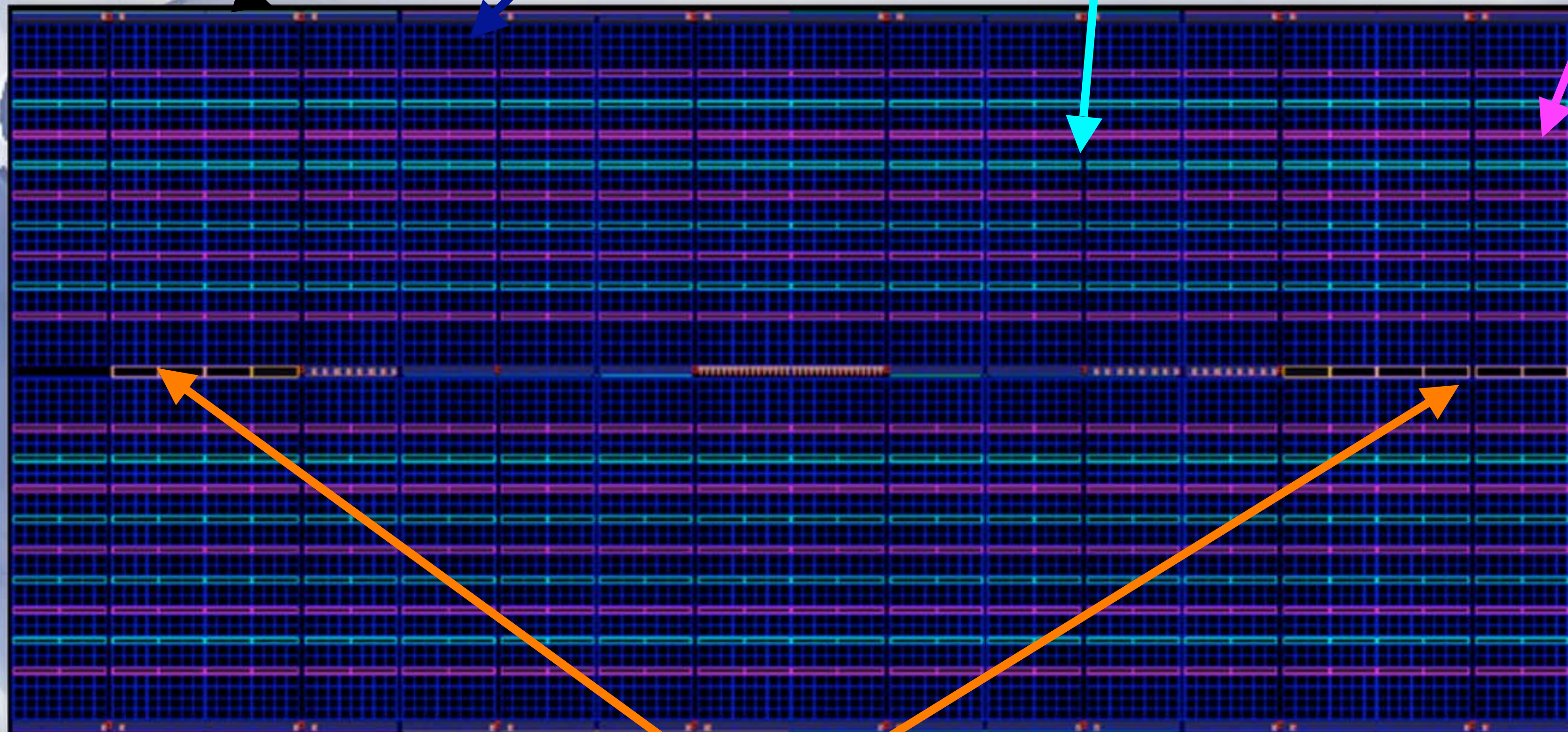
We present static results for the family of thin-epitaxial Xilinx Virtex-4 FPGAs, and make comparisons to previous results obtained for theVirtex, Virtex-II, and Virtex-II Pro. The data presented was acquired through a consortium based effort, with the common goal of providing the space community with data and mitigation methods for the use of Xilinx FPGAs in space.

- Device Description
- Test Objectives
- Test Methodologies and Results
- Scaling Trends
- High Current Investigation and Mitigation
- Conclusions

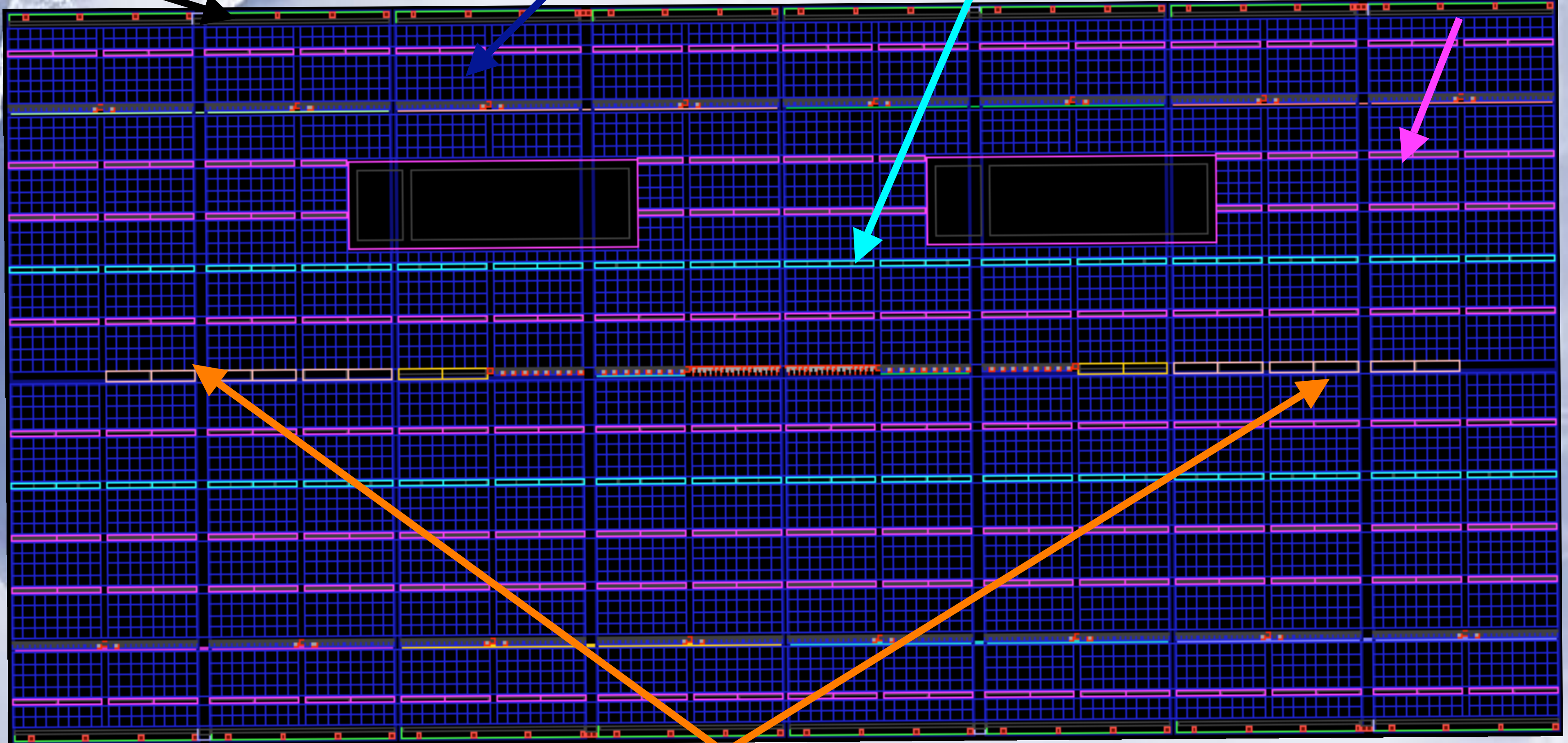
Virtex-4 SX55 Features



SX55 Configuration bits: 15964416

SX55 BRAM bits: 6738432

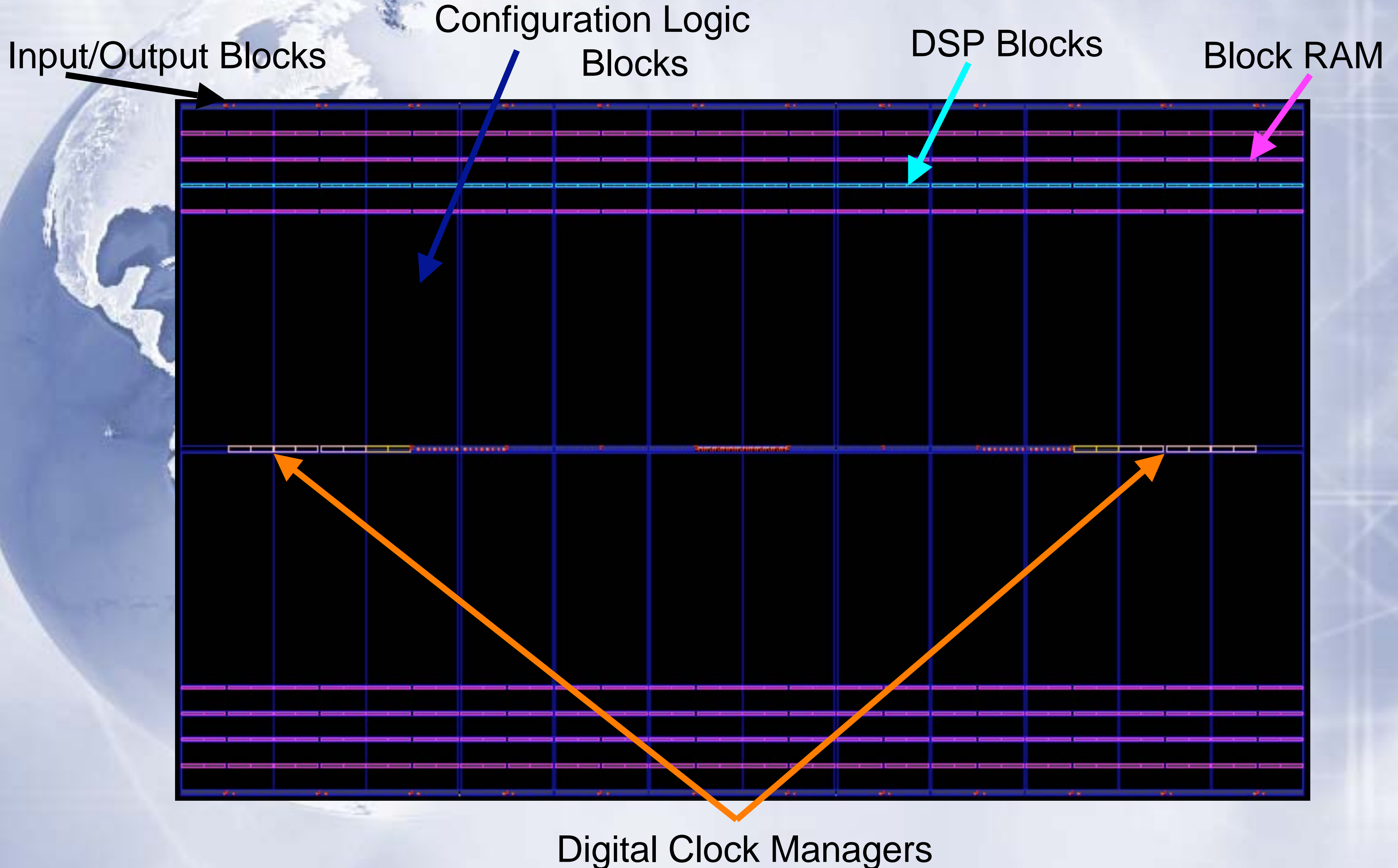
Virtex-4 FX60 Features



FX60 Configuration bits: 15565568

FX60 BRAM bits: 5394944

Virtex-4 LX200 Features

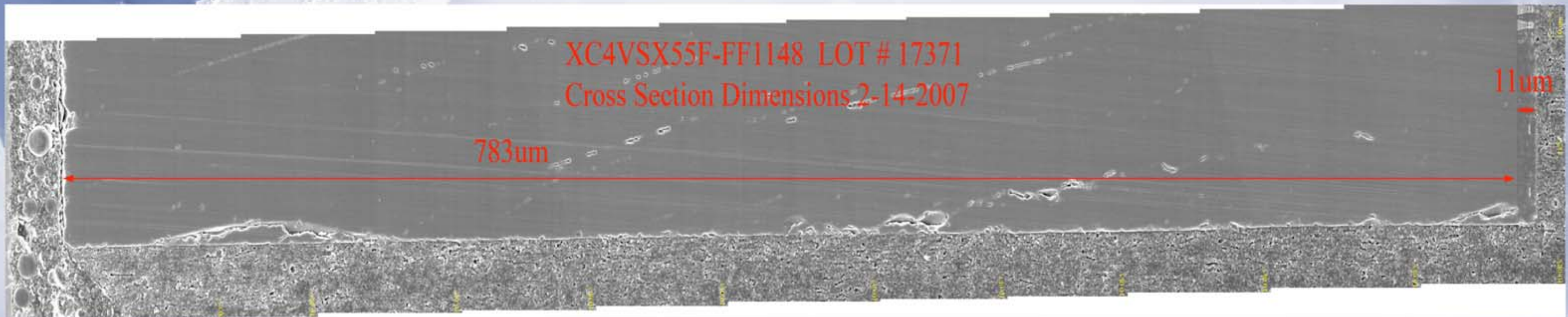


LX200 Configuration bits: 44240640

LX200 BRAM bits: 7084800

Device Summary

- XQR4VSX55-FF1148, XQR4VFX60-FF1148, XQR4LX200-FF1513
  - 90nm CMOS Process, 1.2V core voltage
  - Flip Chip Geometry
    - Requires Device Thinning (From ~780 microns down to ~100 microns silicon)



  - Thin Epitaxial Substrate Layer (2 microns)

Test Objectives

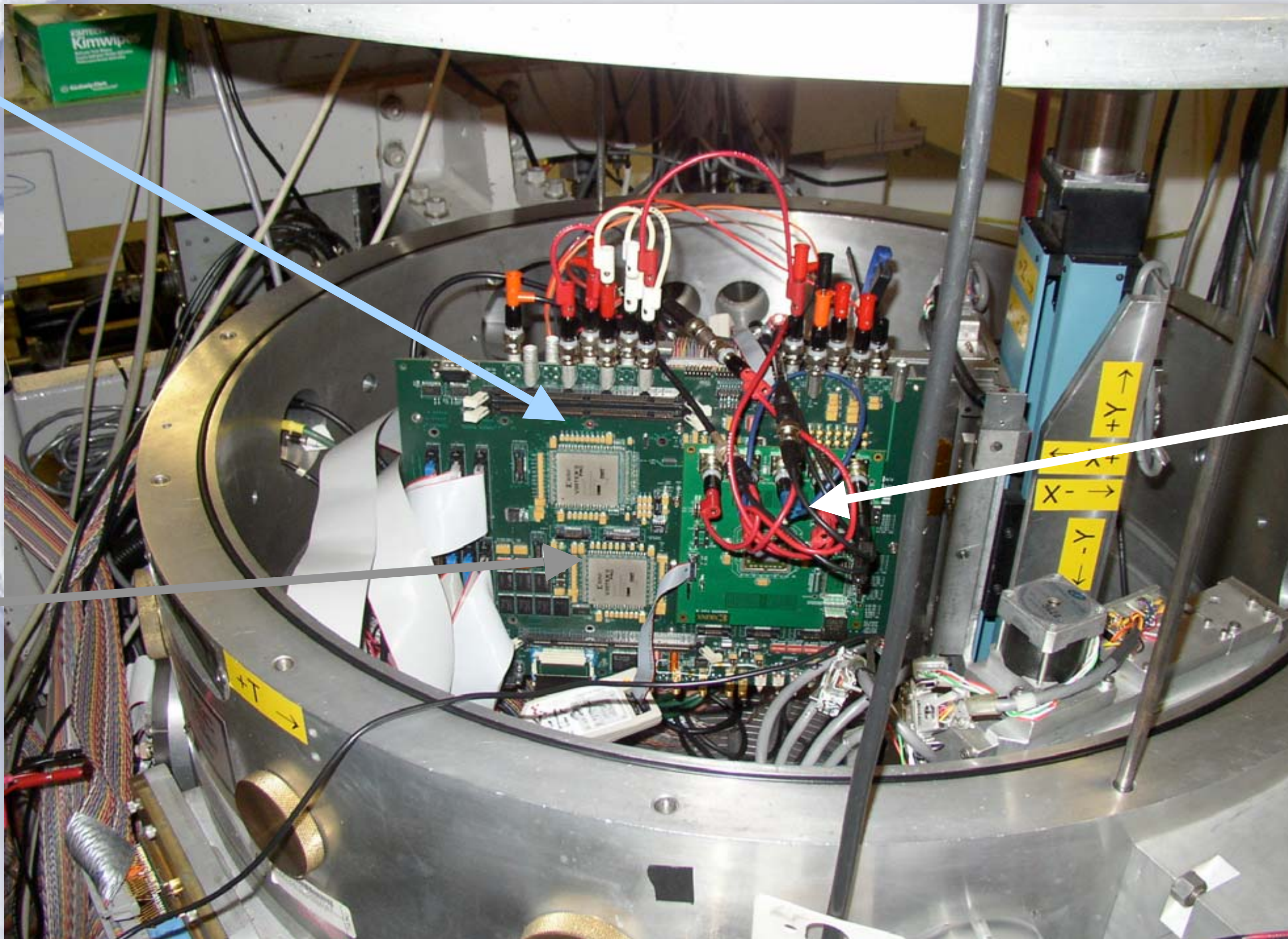
- Complete Full Static Characterization (Static Cross Section as a function of LET/Energy)
  - Single Event Functional Interrupt (SEFI)
  - Latchup (High Temperature and LET)
  - Configuration Memory
  - Block RAM (BRAM)
  - User Flip-Flops
  - Half-Latches (Weak Keeper Circuits)

Test Setup

Functional Monitor

DUT Daughter Card

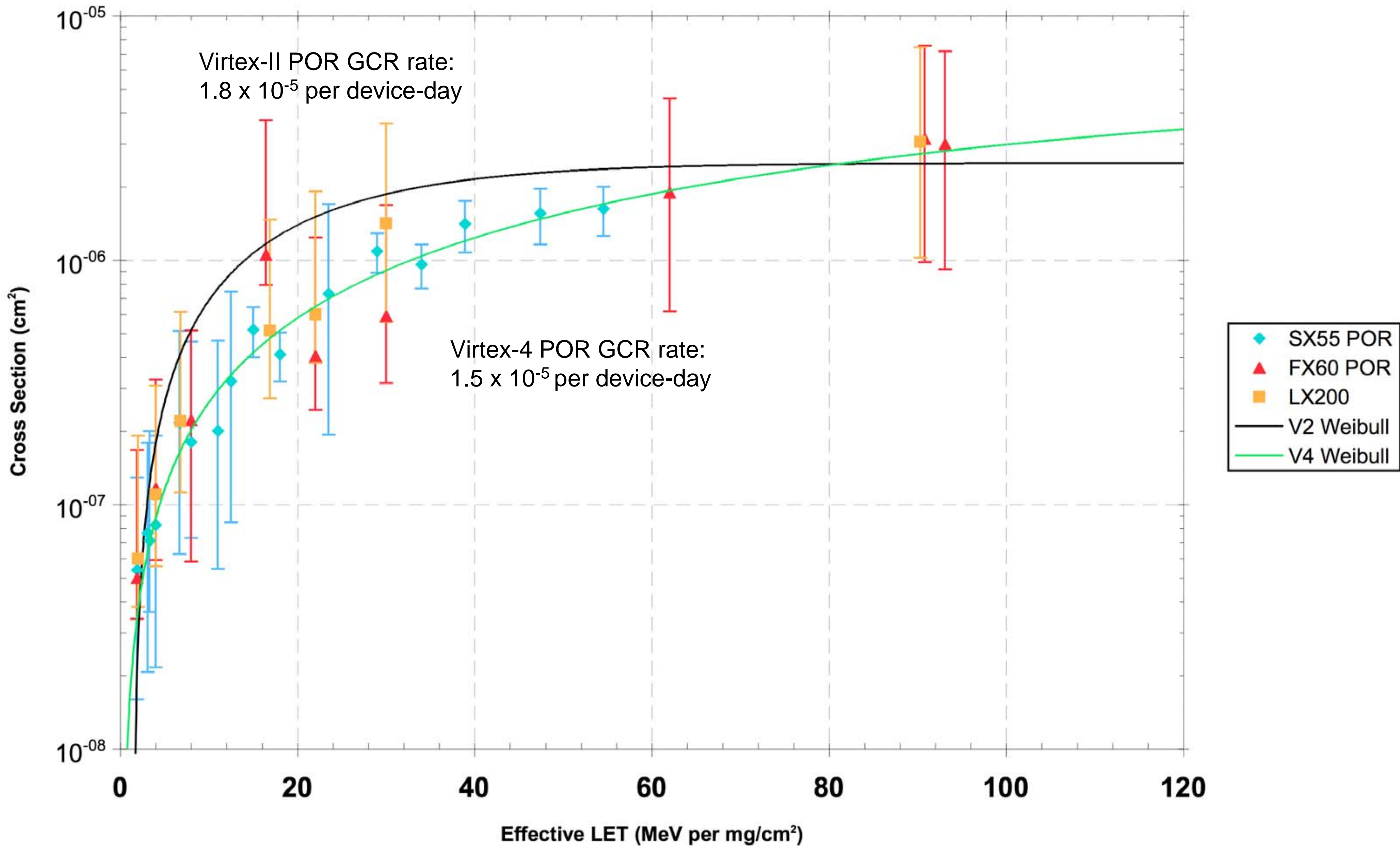
Configuration Manager



SEFI Test Design and Methodology

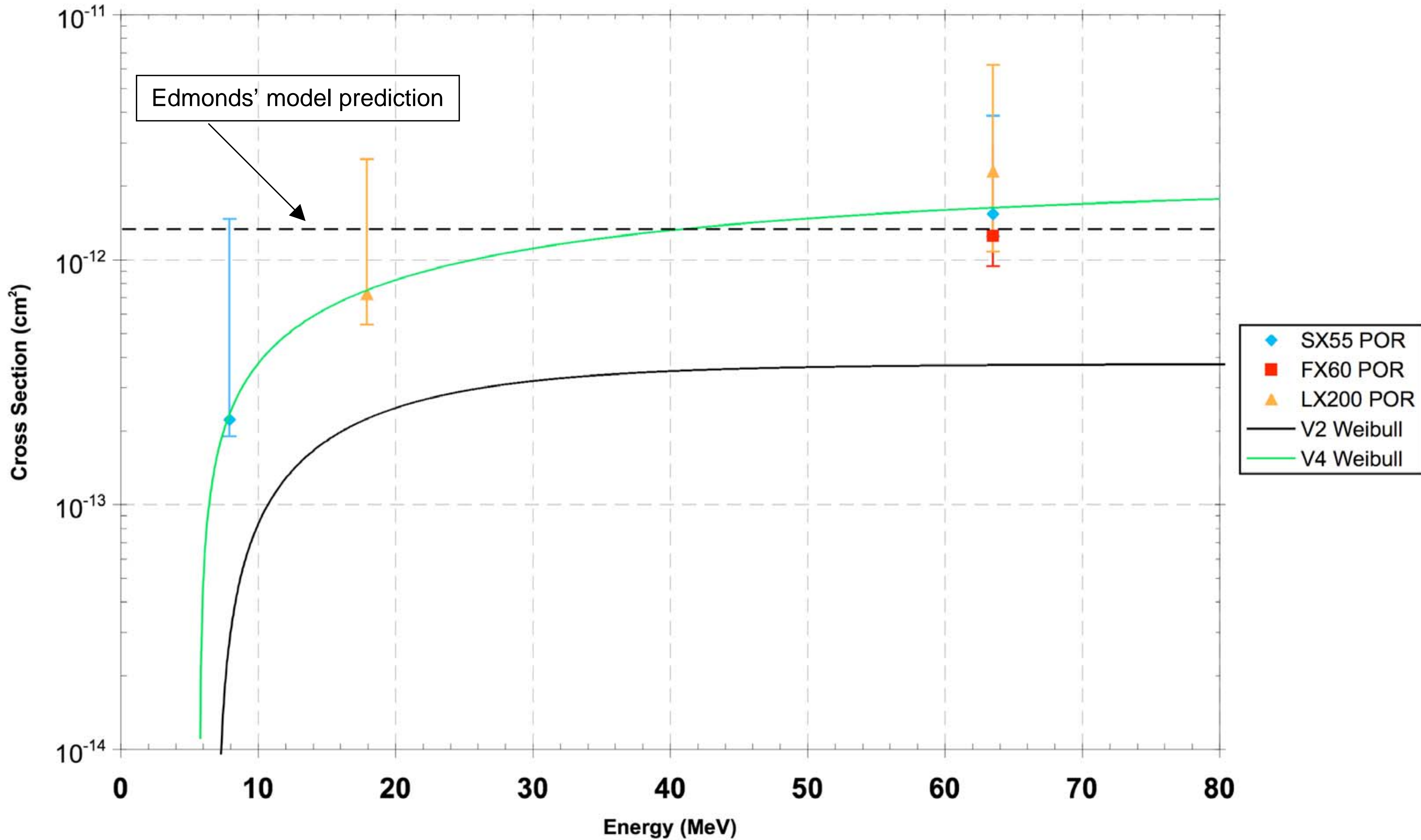
- DUT design is nearly irrelevant (for most SEFIs)
  - Usually try to use a functional design that requires a lot of flux (e.g. half latch test)
  - Try to use an application that uses several I/O's and I/O's from different banks
  - Monitor/control device status pins (done, init, prog, etc.)
  - SEFI's have a low cross section, therefore requiring high amounts of fluence for good statistics
  - Four SEFIs defined for the Virtex-4: POR, SMAP, FAR, and Global Signal

- POR-Power-On-Reset SEFI
  - Accomplishes the same thing as a POR
  - It is not know if it comes from POR circuitry or something else in the configuration logic
  - Detected if DONE goes low, if all configuration logic is reset, or if all configuration control registers are reset to a preconfigured state



All Virtex-II data can be found in [1]

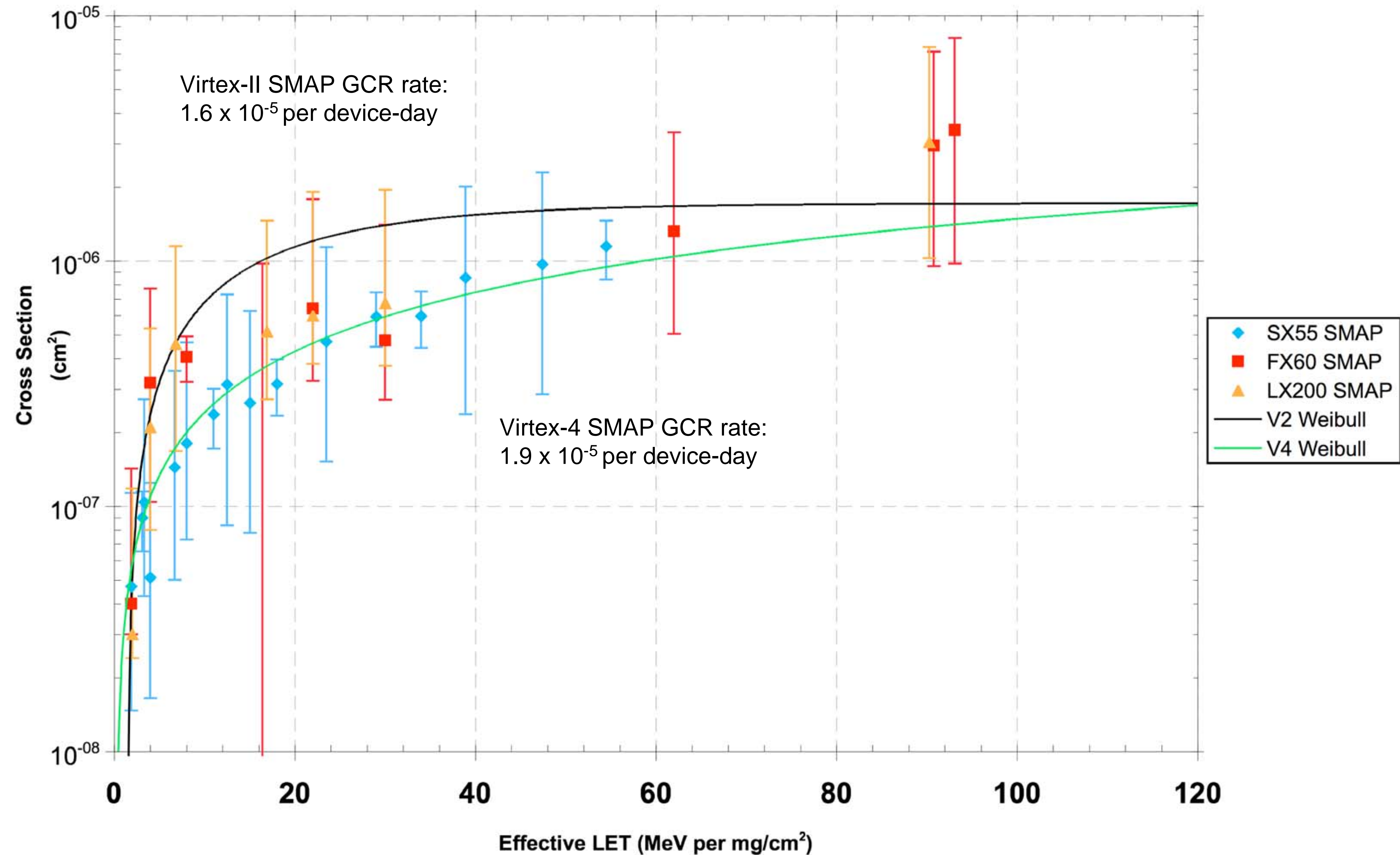
All rates calculated at Adams GCR solar minimum, with nominal 100 mils shielding



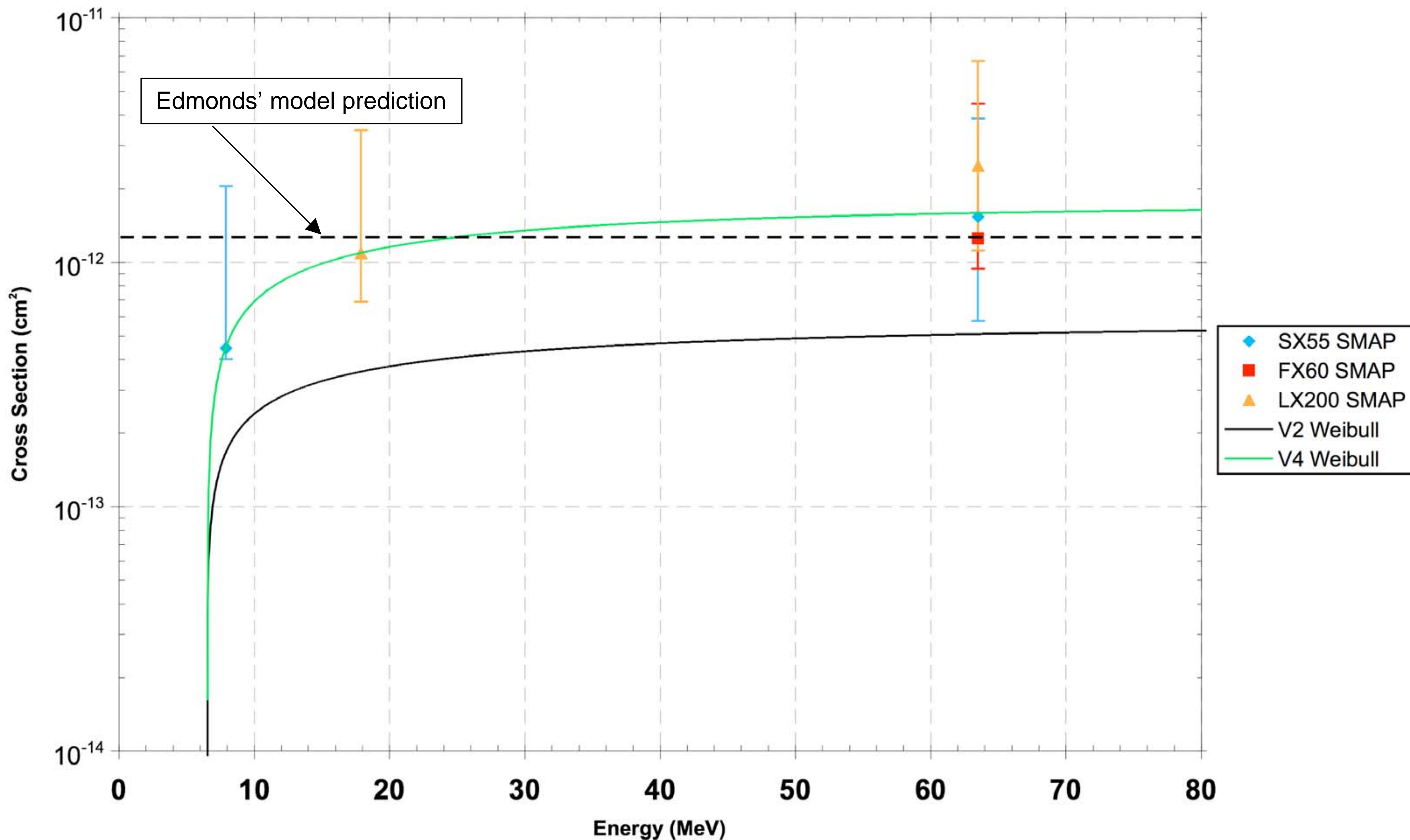
The dashed line represents model predictions of proton results taken from heavy ion data [2]

SEFI Definintions—SMAP

- SelectMAP SEFI
  - Configuration is controlled through this port
  - Disabling the SMAP port will cause lots of upsets to accumulate
  - Detected by an inability to read/write to configuration memory or control registers, nonsensical configuration data, etc.



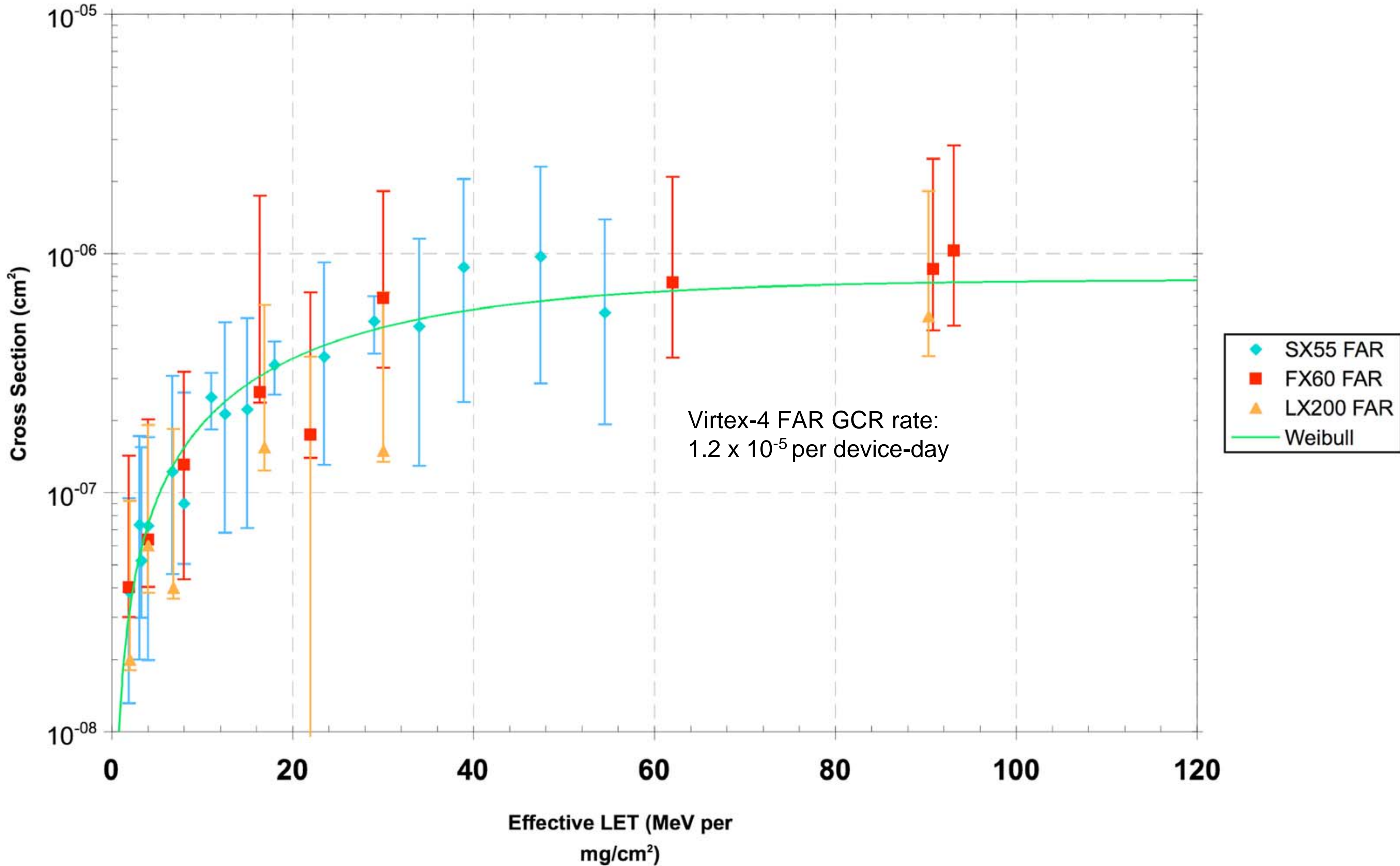
All rates calculated at Adams GCR solar minimum, with nominal 100 mils shielding



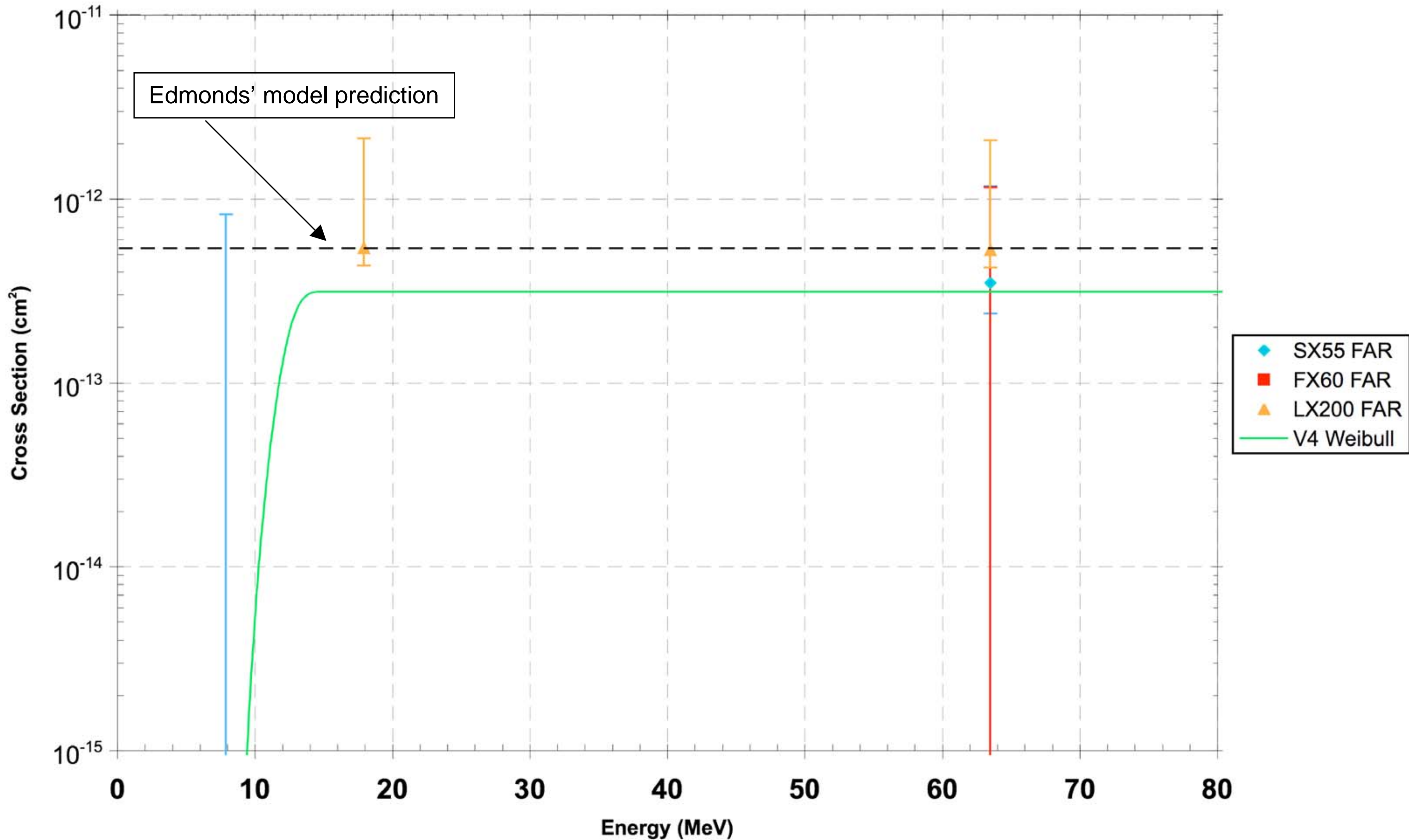
The dashed line represents model predictions of proton results taken from heavy ion data [2]

SEFI Definintions—FAR

- FAR SEFI
  - An upset to the FAR control logic
  - A set of dummy read/writes are used to detect a FAR SEFI
  - Recovered by pulsing PROG and reconfiguring the device



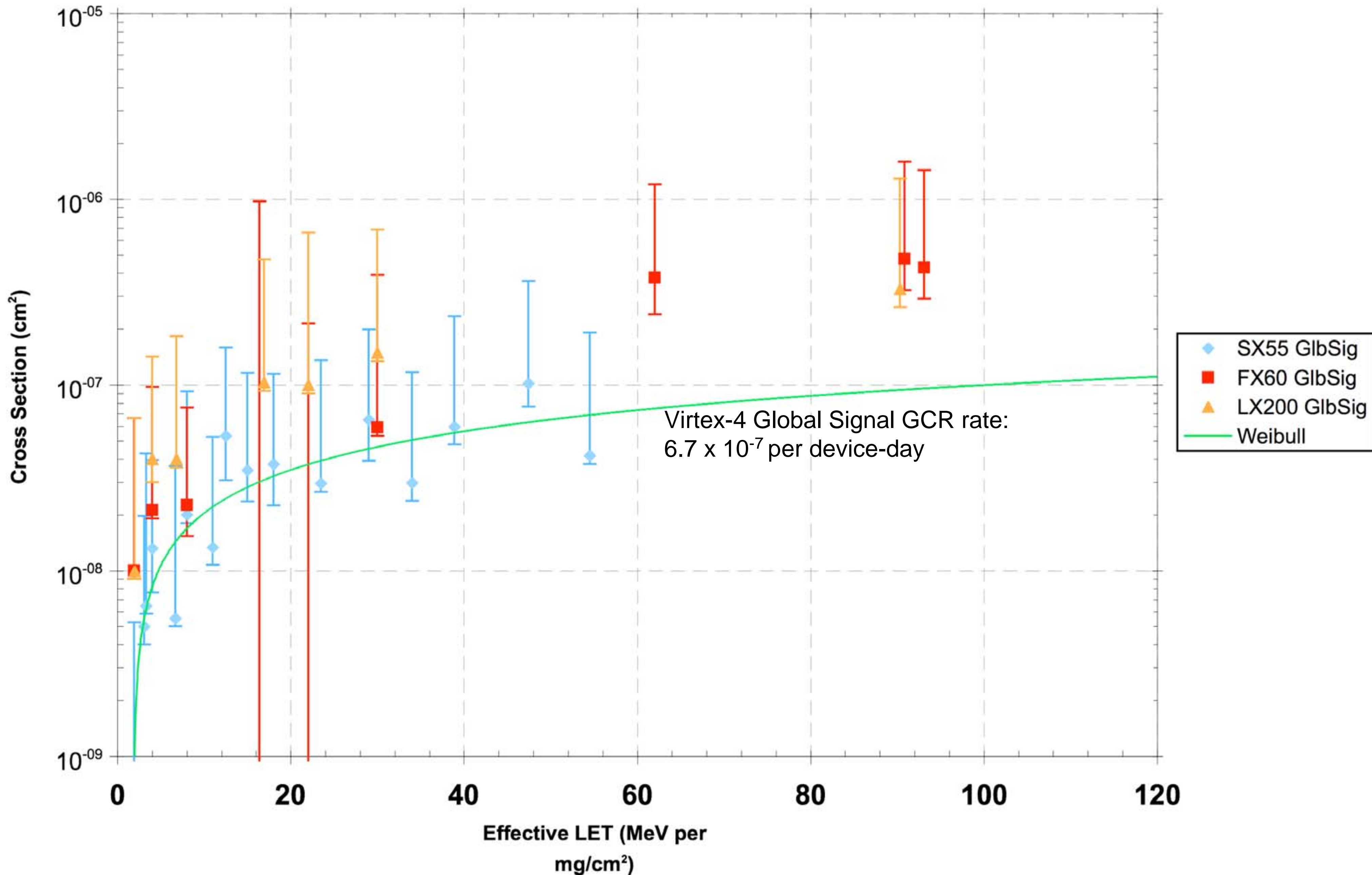
All rates calculated at Adams GCR solar minimum, with nominal 100 mils shielding



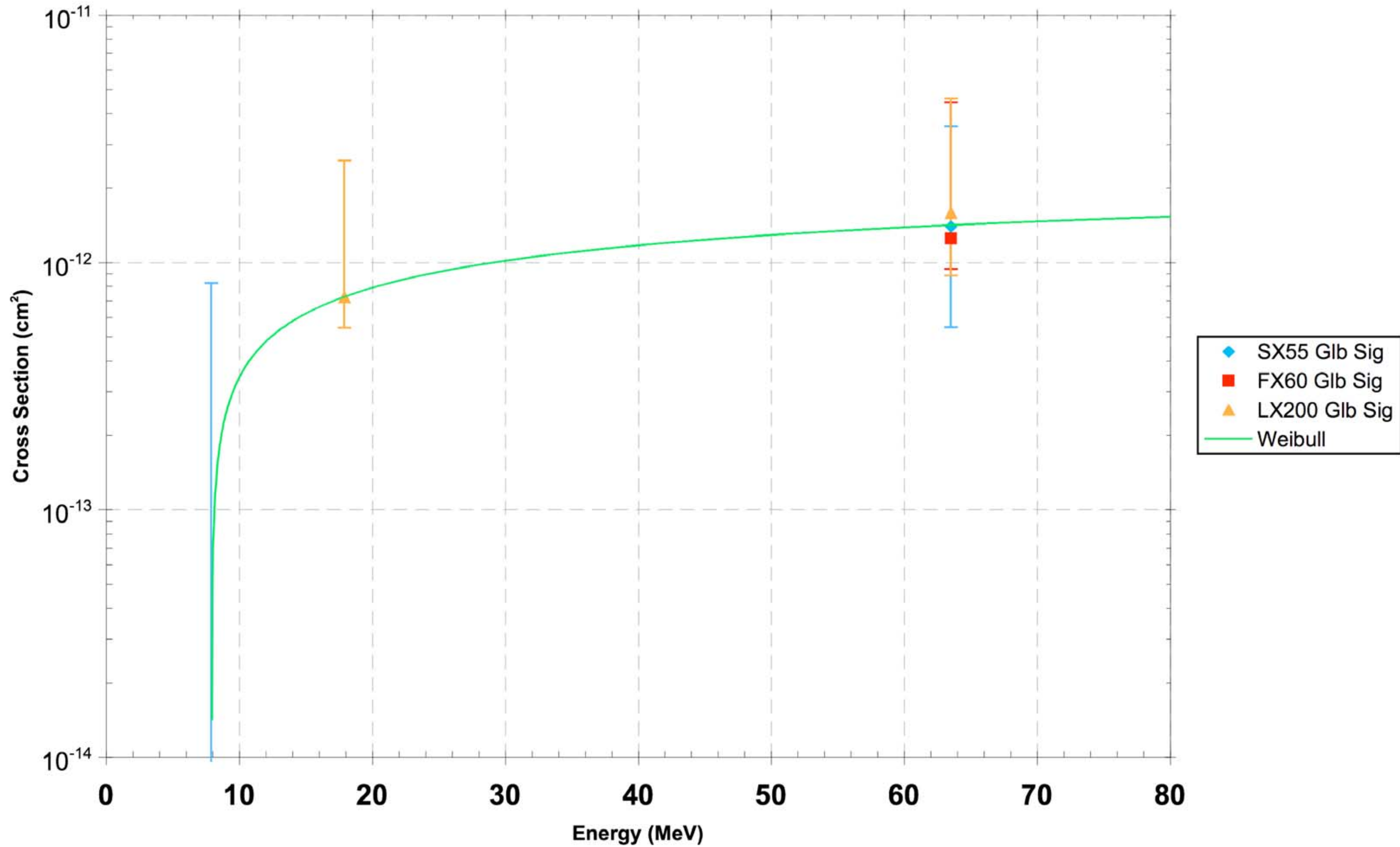
The dashed line represents model predictions of proton results taken from heavy ion data [2]

SEFI Definintions—Global Signal

- Global Signal SEFI
  - Detected if there is an upset to the control or status register
  - Recovered by pulsing PROG and reconfiguring the device



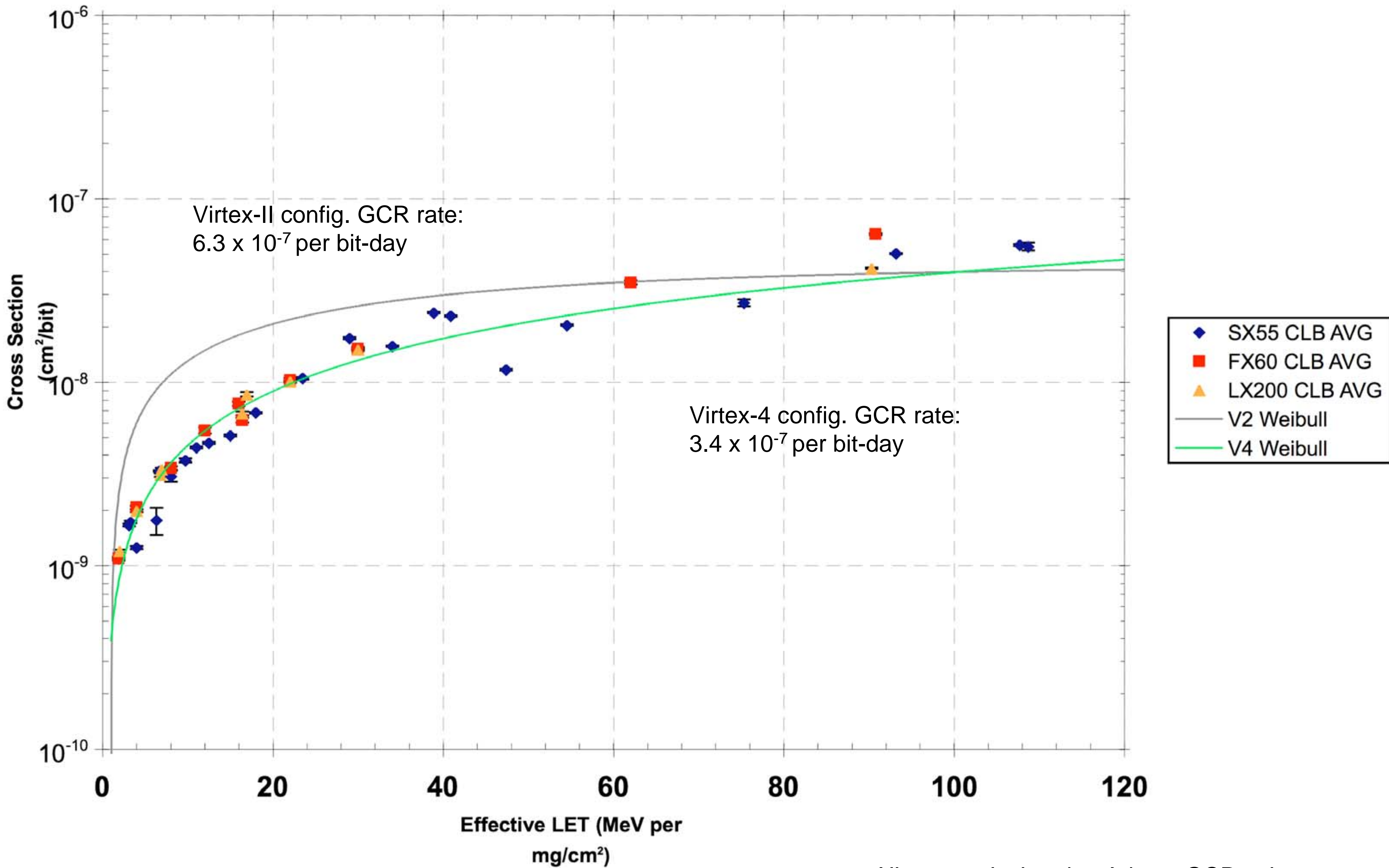
All rates calculated at Adams GCR solar minimum, with nominal 100 mils shielding



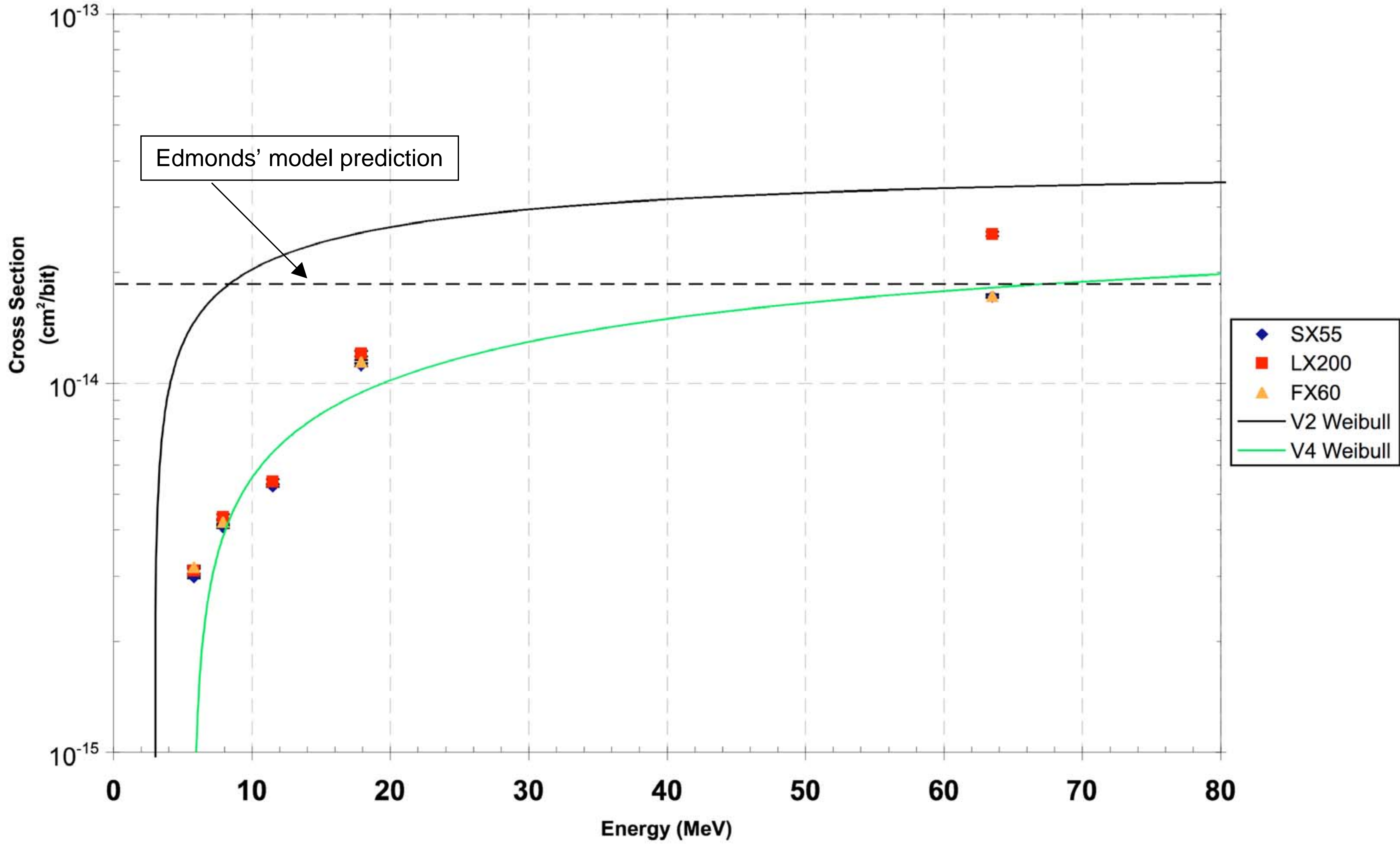
Xilinx Virtex-4 Proton Average Global Signal SEFI Cross Section
Cross Section (cm²)
Energy (MeV)
10-11
10-12
10-13
10-14
0
10
20
30
40
50
60
70
80
SX55 Glb Sig
FX60 Glb Sig
LX200 Glb Sig
Weibull

CLB and BRAM Design and Methodology

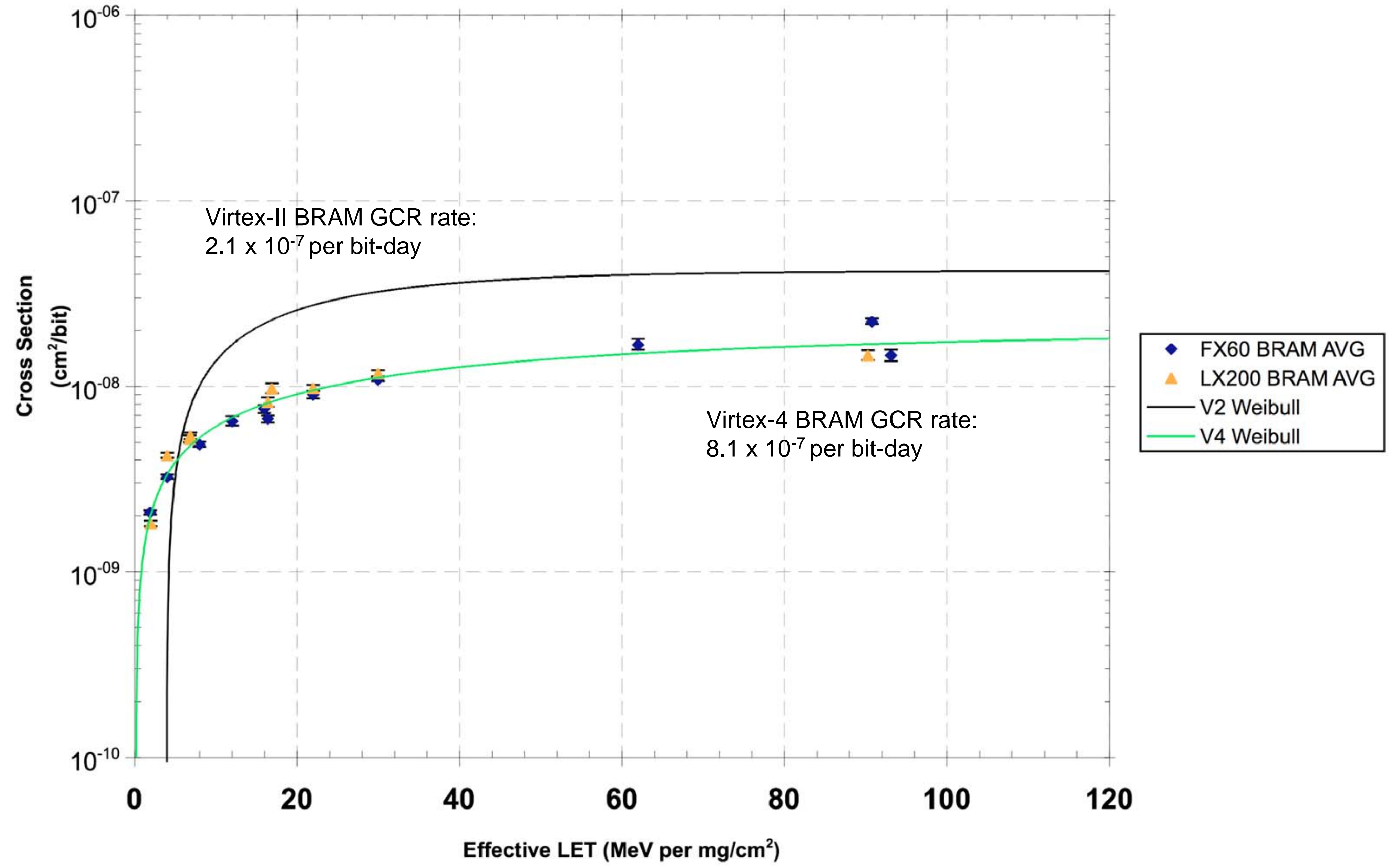
- Three Methodologies:
  - Low flux, low fluence with an iMPACT device readback after irradiation
  - Low flux, low fluence with a configuration readback after or during irradiation
  - Low flux, low fluence with readback and scrubbing during irradiation
- BRAMs tested with fill patterns of both '0' and '1'



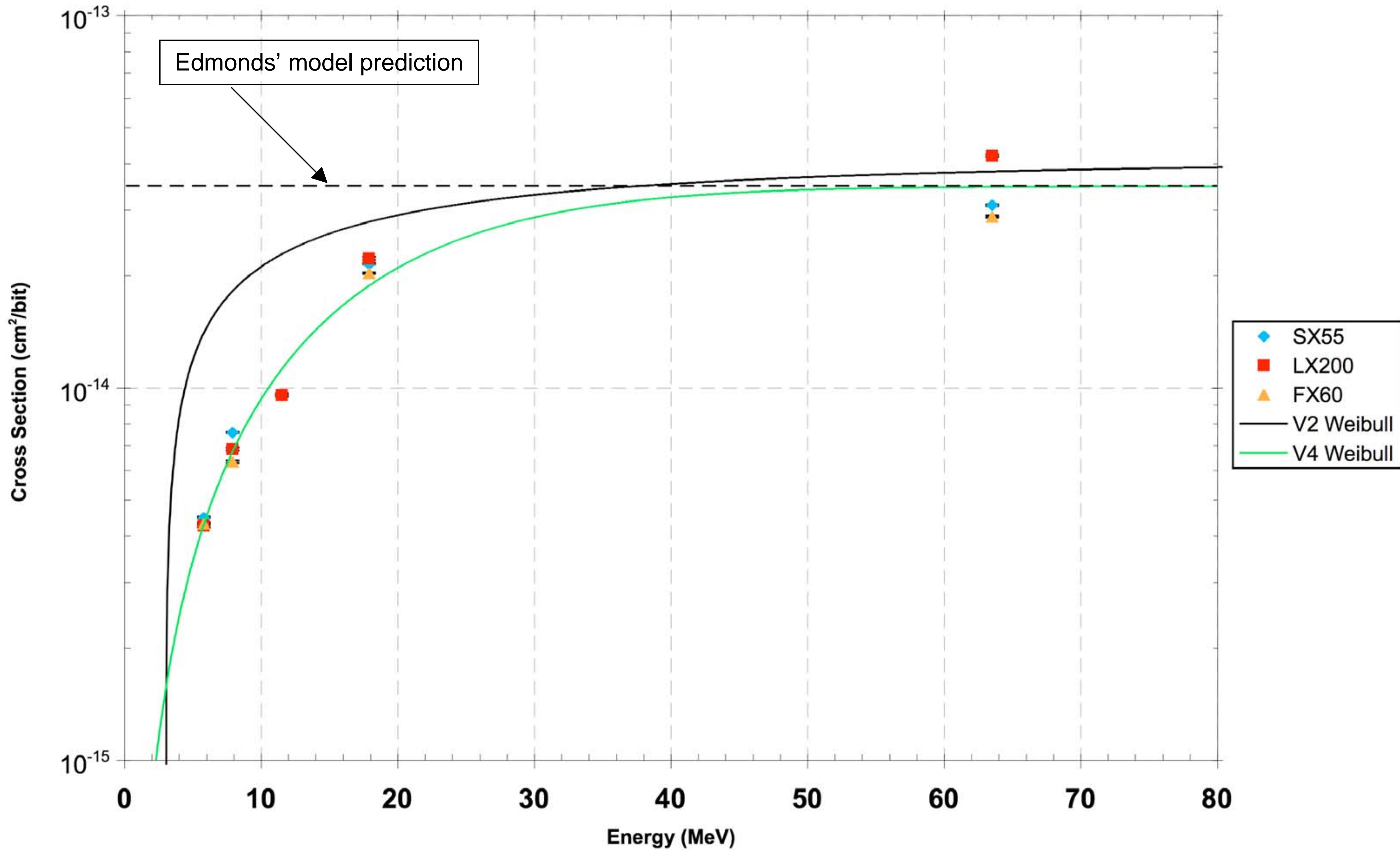
All rates calculated at Adams GCR solar minimum, with nominal 100 mils shielding



The dashed line represents model predictions of proton results taken from heavy ion data [2]



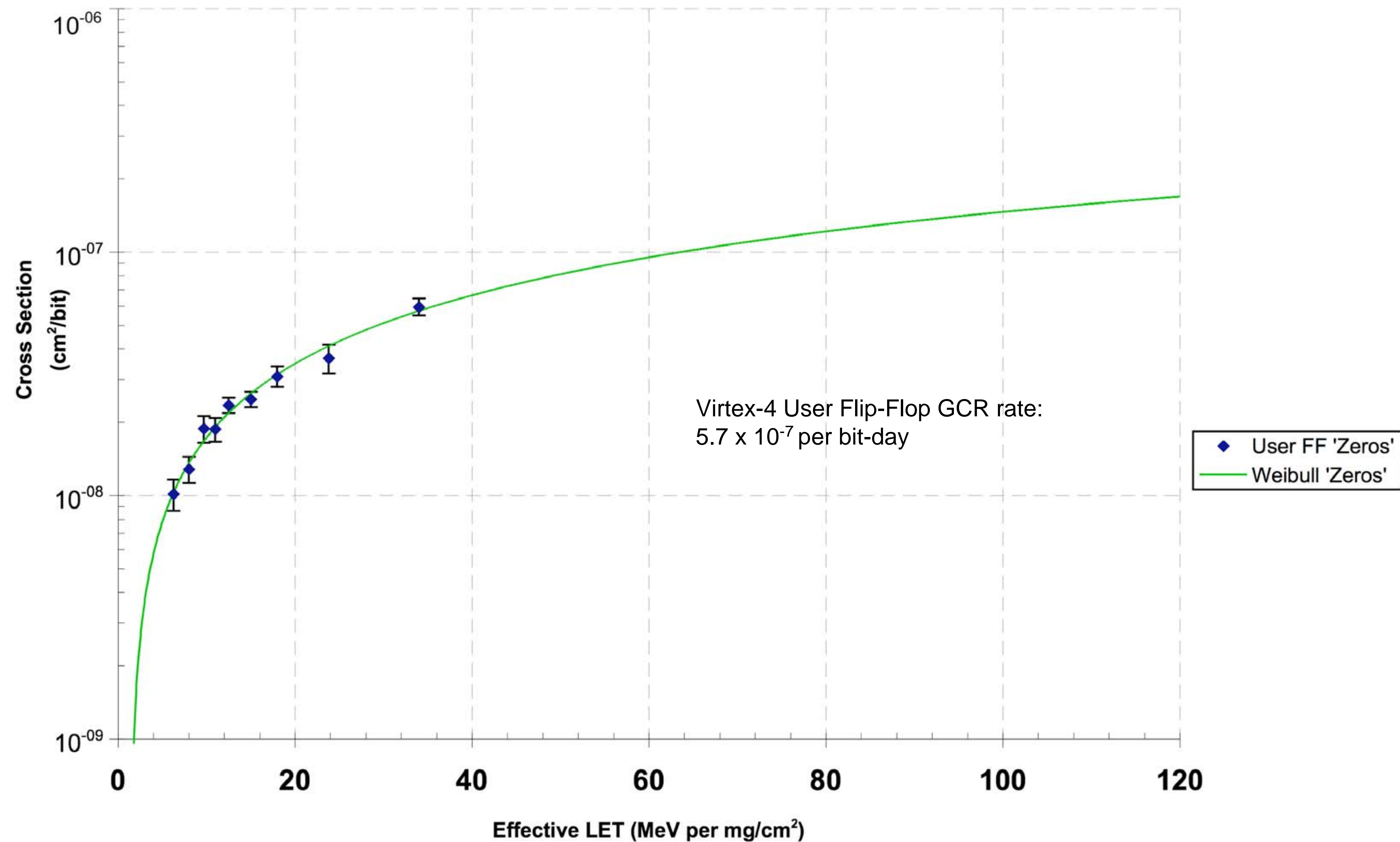
All rates calculated at Adams GCR solar minimum, with nominal 100 mils shielding



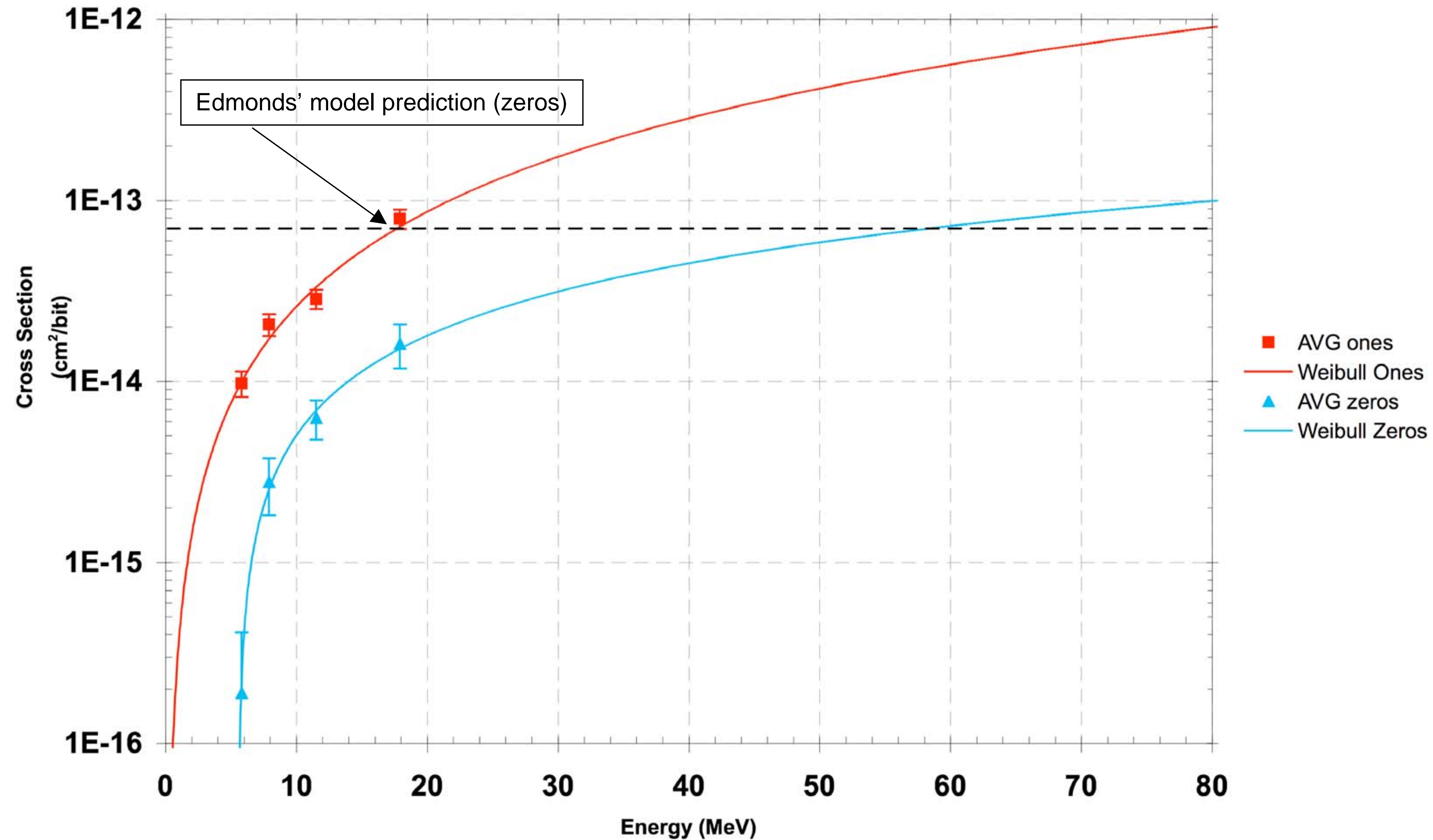
The dashed line represents model predictions of proton results taken from heavy ion data [2]

User Flip-Flop Design and Methodology

- 33 shift register chains of 1024 flip-flops each were implemented in the DUT
  - The user could select the pattern to be shifted in ('0', '1', or checkerboard)
- Device was irradiated statically at low fluxes
- Errors were clocked out and counted after irradiation
- The DUT configuration was scrubbed while being irradiated.

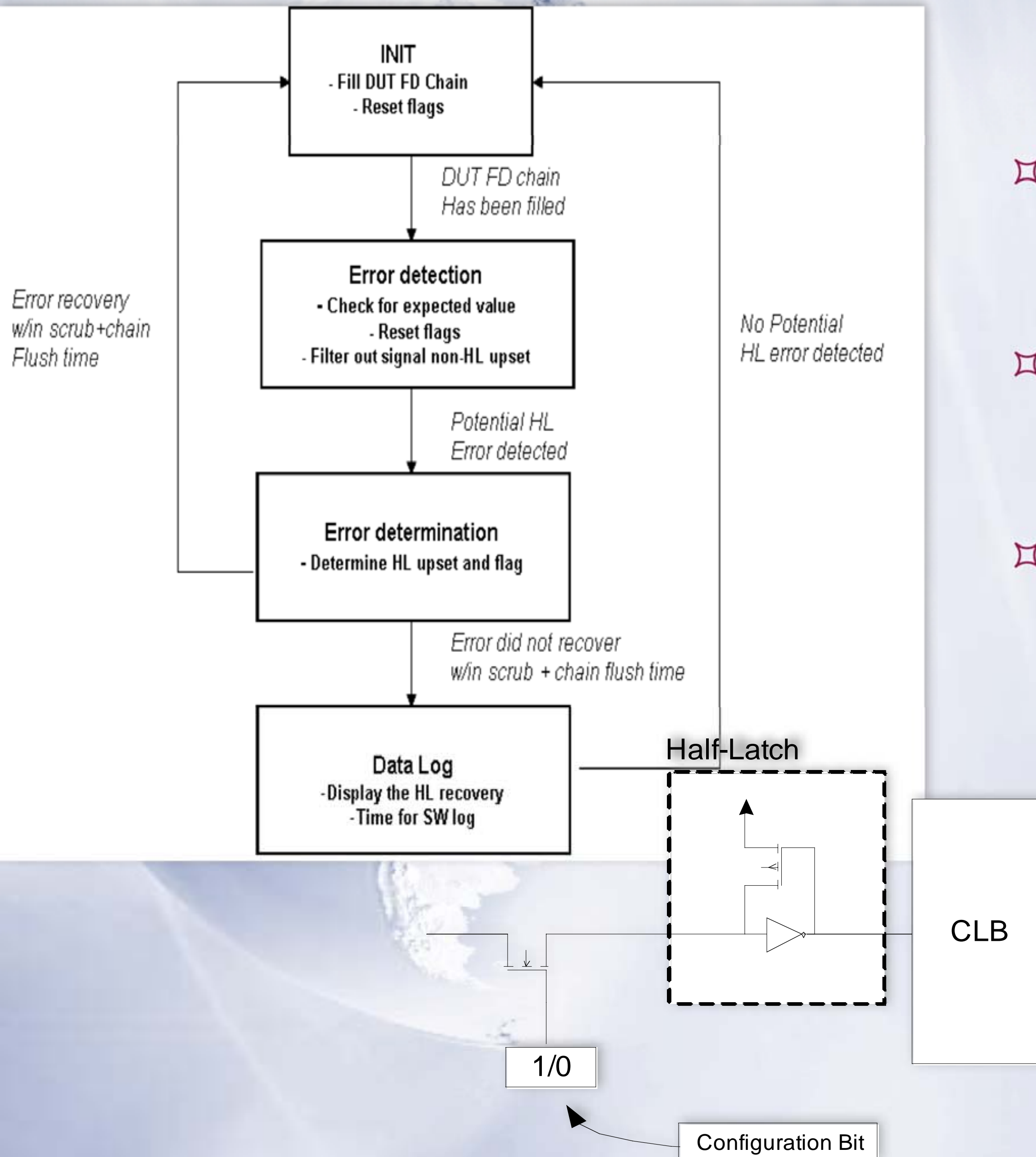


All rates calculated at Adams GCR solar minimum, with nominal 100 mils shielding



The dashed line represents model predictions of proton results taken from heavy ion data [2]

Half-Latch Design and Methodology



- Design consists of 32 independent long shift register chains that utilize as much of the device's Flip-Flops as possible.
- Each FD has at least 2 half latches at its CE (clock enable) and RST (reset) ports. The clock rate to the shift register chains is at 32 KHz.
- To detect half latch upsets, 32 independent monitoring state machines exist on a monitoring device running at 32 KHz. Each functional monitoring will provide its corresponding DUT shift register chain with input and verifying the output data.

Half-Latch Results

- History of Half-Latch testing
  - Virtex II—Very low cross-section of half latches that didn't recover
  - Virtex-II Pro—No stuck half latches, but some that took several seconds to recover
  - Virtex-4—No long recovering or stuck half latches
- Conclusion: Half-Latch upsets have improved over technology scaling

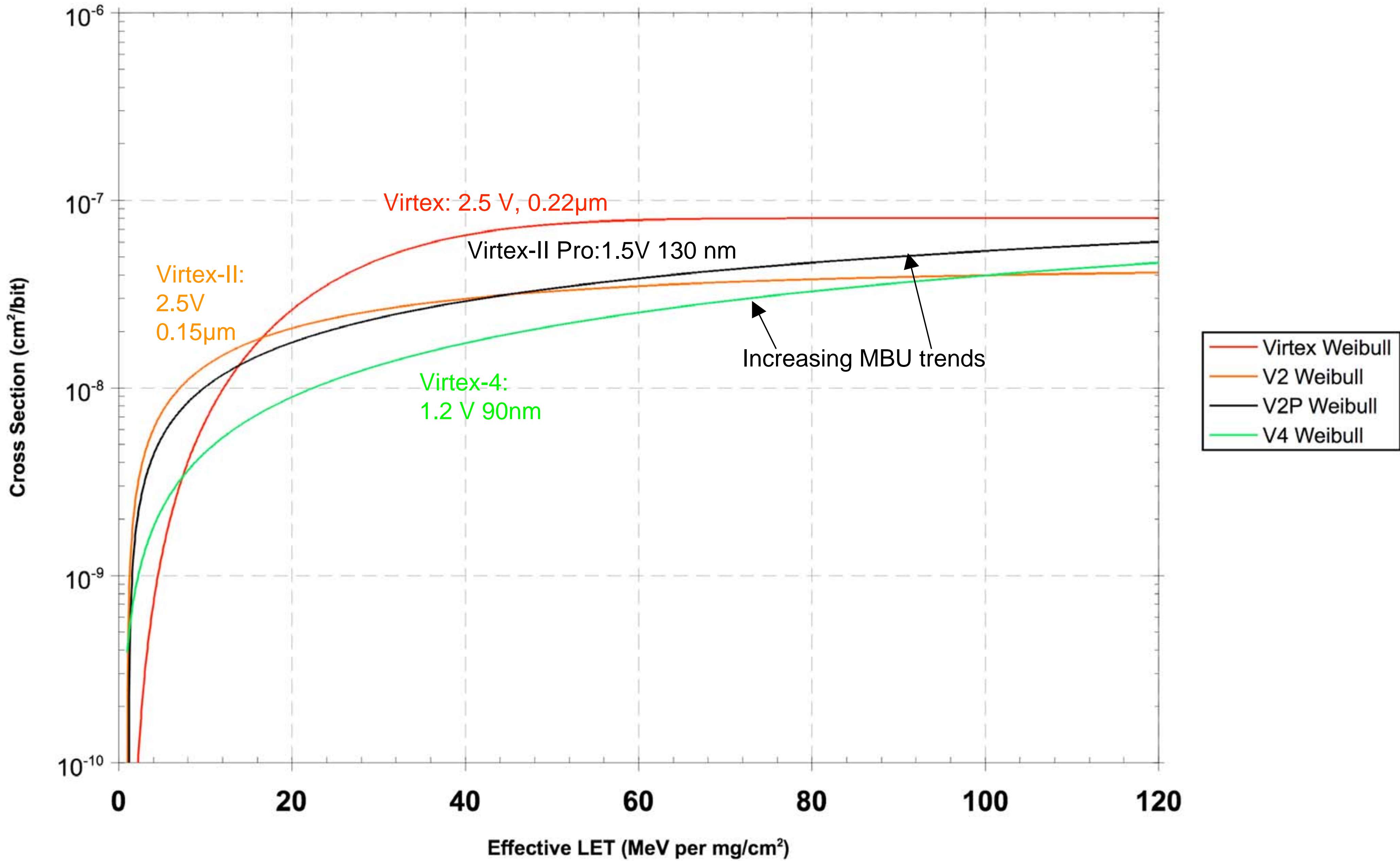
Single Event Latchup testing…

- Latchup was tested in vacuum up to an effective LET of 109 MeV per mg/cm^2 (SX55) and 90 MeV per mg/cm^2 for the LX200 and FX60.
- All parts were heated to 120° C
- The DUTs were biased to Voltage Spec. Max
- A minimum total fluence of $1X10^7$ $ions/cm^2$ was subjected to each DUT
- No latchup was observed
- No high current phenomenon (as observed in the V-II Pro) was observed during latchup runs
- A total of 5 parts were tested: 3 SX55, 2 FX60 and 1 LX200.

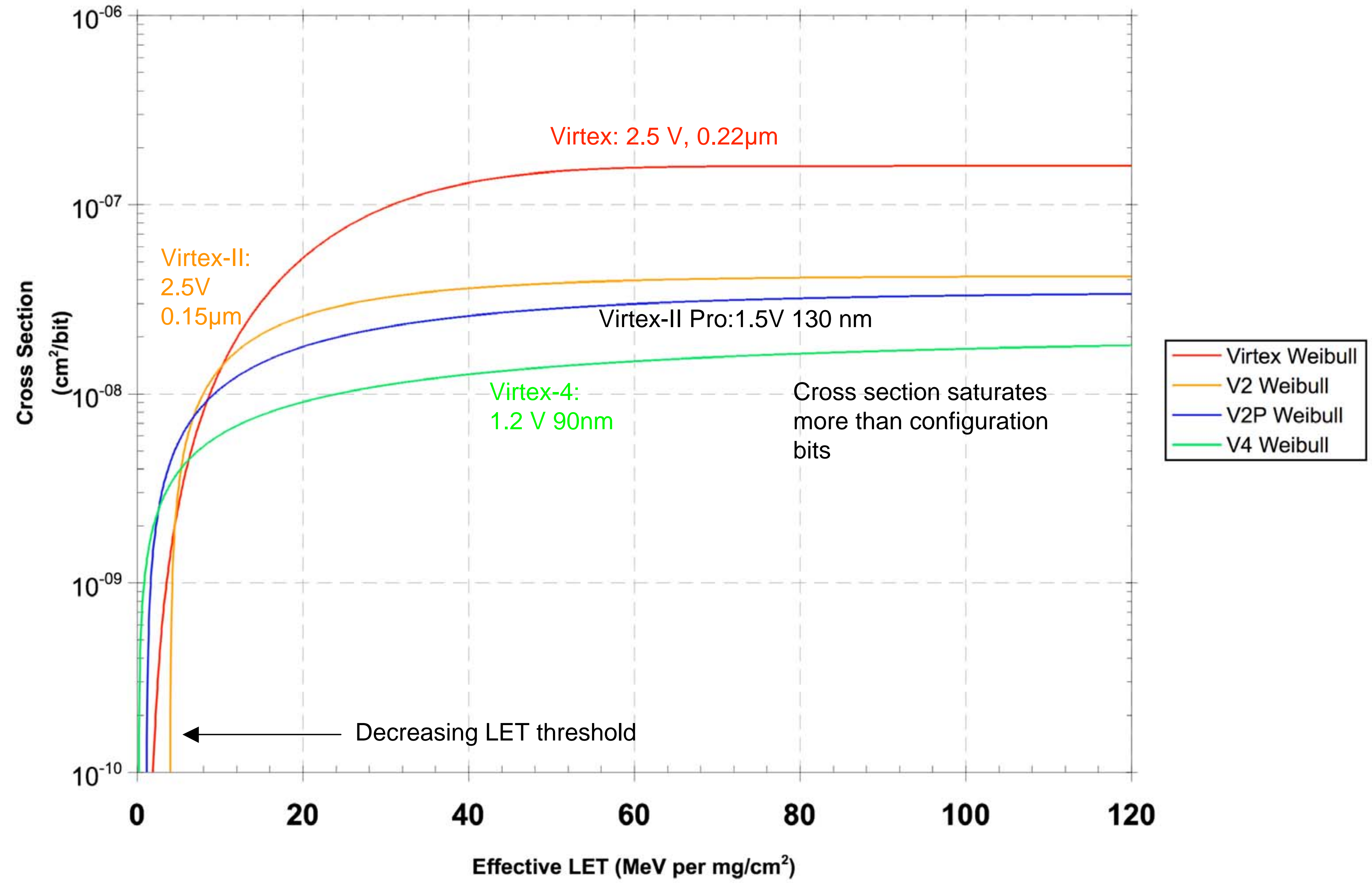
- A high current mode was observed during SEFI testing during March 2007
- Event had a very low cross-section (an order of magnitude less then SEFIs)
- Not SEL
- Focused investigation into the scrubbing algorithm

High Current Investigation Results

- Proved that the scrubbing algorithm caused the high current seen in beam testing
- Developed a new, frame-based scrubbing algorithm and beam tested the new design
- Now recommend frame based scrubbing and readback/scrub approach (no blind scrubbing)



Virtex data was taken from [3]


Xilinx Virtex Family Heavy Ion SEU BRAM Cross Section
Cross Section (cm²/bit)
Effective LET (MeV per mg/cm²)
10-06
10-07
10-08
10-09
10-10
0
20
40
60
80
100
120
Virtex: 2.5 V, 0.22μm
Virtex-II:
2.5V
0.15μm
Virtex-II Pro:1.5V 130 nm
Virtex-4:
1.2 V 90nm
Cross section saturates
more than configuration
bits
Decreasing LET threshold
Virtex Weibull
V2 Weibull
V2P Weibull
V4 Weibull

- Overall per bit fabric performance has improved over last two generations (although scaling has allowed for more bits)
- No high current at high temperature phenomenon as seen in V-II Pro
- No SEL observed
- SEFI rates approximately the same, but no Power Cycle SEFI
- Partial Reconfiguration based high current has changed the recommended scrubbing methodology

References

- [1] G. M. Swift et. al. "Xilinx Single Event Effects 1st Consortium Report: Virtex-II Static SEU Characterization," January 2004. Available: http://parts/docs/swift/virtex2_0104.pdf
- [2] L. D. Edmonds, "Proton SEU Cross Sections Derived from Heavy Ion Test Data," IEEE Trans. Nucl. Sci., vol 47, no. 5, 2000.
- [3] E. Fuller, et al. "Radiation Testing Update, SEU Mitigation, and Availability Analysis of the Virtex FPGA for Space Reconfigurable Computing." Available: http://www.xilinx.com/support/documentation/data_sheets/ds003-1.pdf