

3-D Simulation of Heavy-Ion Induced Charge Collection in SiGe HBTs on SOI

Muthubalan Varadharajaperumal, Guofu Niu, John D. Cressler, Robert A. Reed, and Paul W. Marshall

Abstract— This paper presents the 3-D simulation of heavy-ion induced charge collection in SiGe HBTs on SOI. Charge collection is found to be independent of the thickness of n^+ buried layer, part of the silicon-on-insulator film, which directly relates to the collector resistance. The simulation results show that potential perturbation is confined within a thin region near the collector-base junction, due to the heavy doping of the n^+ layer. Comparisons with bulk SiGe HBTs show that the charges collected by the collector and substrate are much smaller in SOI than in bulk HBTs, primarily because of the removal of the collector-substrate pn junction. The charges collected by the emitter and base, however, are nearly identical in SOI and bulk HBTs, because the heavily doped n^+ buried layer decouples the potential perturbation and hence charge collection in the intrinsic emitter, base and collector from those in the collector-substrate junction. The load dependence of charge collection is also examined.

I. INTRODUCTION

High speed SiGe HBTs have demonstrated excellent hardness to both total dose and displacement radiation without intentional hardening, making them attractive for space applications. Single-event upset, however, is a potential problem, because of existence of the n^+ buried layer to p-substrate junction. As we will show below, the problem is particularly worse for heavy ions that penetrate deep into the substrate. A natural approach to SEU hardening is to remove the p-type substrate, thus eliminating the n^+ buried layer to p-substrate junction. In practice, this can be realized by fabricating the SiGe HBT on an SOI substrate, the feasibility of which has been demonstrated by various companies [1] [2] [3], primarily for reduction of parasitic capacitance and hence higher speed.

The purpose of this work is to investigate charge collection characteristics in SiGe HBTs on SOI using 3-D device simulation. We will examine the impact of the SOI thickness on charge collection, the impact of collector loading resistance, as well as the comparison of charge collection between bulk and SOI SiGe HBTs.

II. DEVICE STRUCTURE

The $0.5\ \mu\text{m}$ SiGe HBT structure from our previous work [4] is now simulated on an SOI substrate. The active $n^+/p/n$ emitter-base-collector layers are kept exactly the same for an apple-to-apple comparison. Fig. 1 shows the 3D view of the device, with the color indicating the doping level. Fig. 2 shows a 2-D cross

section obtained from a cut through the center of the 3-D structure. Doping concentration is indicated by color. The device has a p-substrate, $0.4\ \mu\text{m}$ thick buried oxide, an n^+ layer for reducing the collector resistance, a selectively implanted collector, a SiGe base and a polysilicon emitter. The active device is surrounded by trench isolation and buried oxide. The base contact is made through the heavily doped poly SiGe layer on top of the shallow trench. The highlight of the SOI technology is the absence of the collector-substrate junction, which played a major role in charge collection in the bulk device [4].

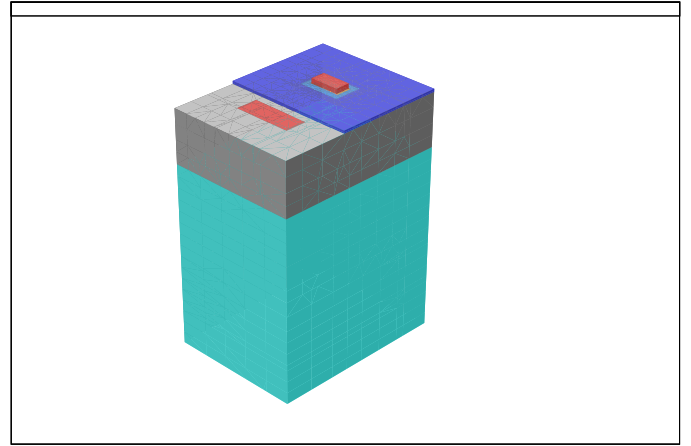


Fig. 1. 3-D view of the device. Color indicates the doping level.

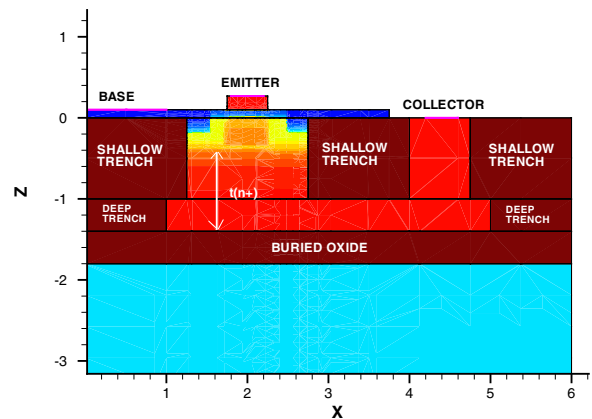


Fig. 2. 2-D cross section of the SOI SiGe HBT simulated.

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III. SEU DEVICE SIMULATION

The 3D structure of the HBT is constructed using MESH [5]. The electrical characteristics are simulated using DESSIS [6]. The doping and Ge profiles of the bulk SiGe HBT described in [4] are used. An 1 GeV Fe ion was used. SRIM simulation [7] showed an average LET of 12 MeV-cm²/mg which is equivalent to 0.1111 pC/ μ m charge deposition. The ion traverses the entire device. The charge track was generated over a period of 10 picoseconds using a gaussian waveform. The 1/e characteristic time scale is 2 picosecond and the 1/e characteristic radius is 0.1 μ m. The peak of the gaussian occurs at 2 picoseconds. The simulator does not support the variation of these constants with LET.

Fine gridding is placed around the charge track using a self-adaptive method described in [4]. As conservation of charge is not achieved by the default discretization scheme, a more accurate discretization scheme called the *Rectangular Box Integration* method is used [4]. The physics simulated includes doping dependant SRH recombination, Auger recombination, the phillips unified mobility model, velocity saturation and bandgap narrowing (BGN). The phillips unified mobility model models the mobility of the carriers accurately in HBTs and Auger recombination is used due to the heavy concentration of carriers generated by the heavy ion. All the terminals are grounded. Transient simulation was performed for five n⁺ layer thicknesses. Each transient simulation was performed until the current decays to zero. One transient simulation takes an average of 4 days on a dedicated Sun Blade 2000 workstation with 1.8 GB memory, provided convergence problem does not occur.

IV. CHARGE COLLECTION

A. Impact of n⁺ layer thickness

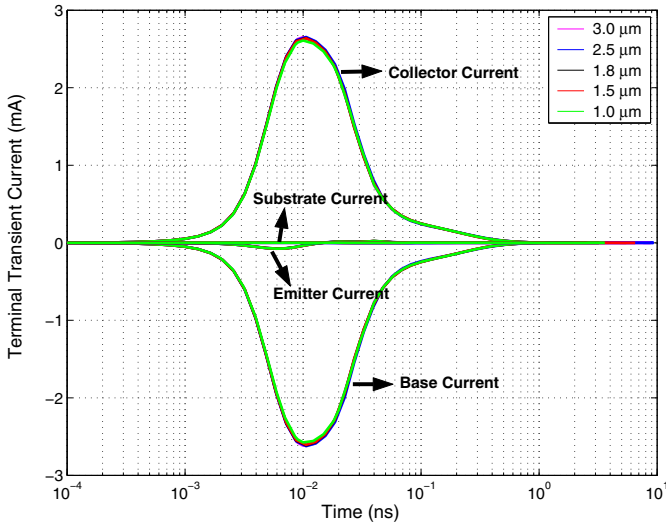


Fig. 3. Transient terminal currents for 5 different thicknesses of n⁺ layer.

Naively, one expects charge collection in SOI devices to be proportional to the thickness of the silicon on insulator layer. In an SOI SiGe HBT, the intrinsic n⁺/p/n layers corresponding to the emitter, base and collector set the minimum thickness of the silicon layer above the buried oxide. These layers are necessary to maintain basic transistor functionality. The only possible variable

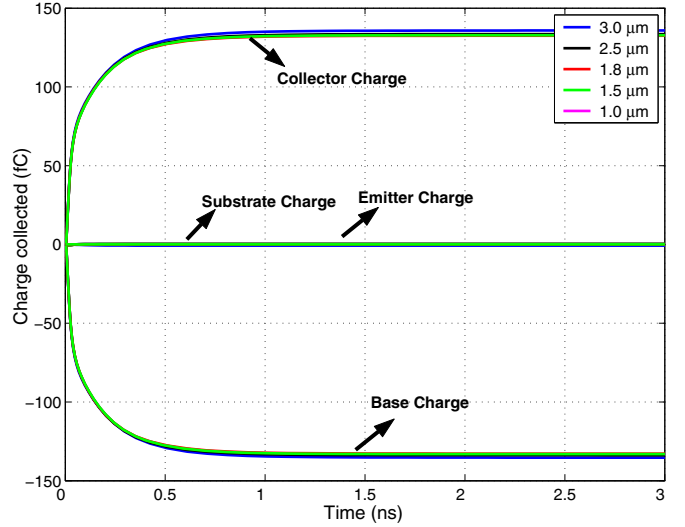


Fig. 4. Charges collected by the terminals for 5 different thicknesses of n⁺ layer.

TABLE I
CHARGE DEPOSITED AND COLLECTED FOR DIFFERENT N⁺ LAYER THICKNESSES.

n ⁺ thickness	Q _{collected} (fC)				Q _{deposited} (fC)
	Q _{coll}	Q _{base}	Q _{emit}	Q _{subs}	
1.0 μ m	133	-133.1	0.27	0.043	144.3
1.5 μ m	133	-133	0.25	0.044	203.68
1.8 μ m	133.4	-133.8	0.263	0.038	244.42
2.5 μ m	136	-135.5	0.32	-0.66	311.08
3.0 μ m	133.3	-133.5	0.272	-0.056	366.63

is the n⁺ buried layer thickness, as shown by t(n⁺) in Fig. 2. A thinner n⁺ buried layer, however, leads to increased collector resistance and increased saturation voltage, which are undesirable. If a smaller n⁺ thickness leads to significant reduction of charge collection, then a trade-off may be made between improving SEU immunity and reducing collector resistance.. Fortunately, this is not the case in SiGe HBTs, as we will show below.

Fig. 3 shows the terminal currents simulated for five n⁺ layer thicknesses. The ion strikes were performed at the center of the silicon island, surrounded by the trench isolation. Current entering the terminal is defined as positive. The terminal current transients are approximately the same for all of the n⁺ layer thicknesses simulated. As a result, the charges collected are independent of the n⁺ layer thickness, as shown in Fig. 4. Substrate and emitter currents are negligibly small at all thicknesses, as expected. The charges are obtained by integrating the terminal current over time.

Electron charge collection occurs primarily through the collector, while hole charge collection primarily occurs through the base. Charge collection through the substrate is negligible. Table I compares the charge deposited in the active volume above the buried oxide against the charges collected by various terminals. For the 1.0 μ m thick n⁺ layer HBT, an equal amount of 144.3 fC electron and hole charges are deposited in the Silicon-On-Insulator film. The charges collected by the collector and base, however, are 133 and -133.1 fC, respectively. Here a negative

charge indicates that positive charges flow out of the base terminal. The charge deposited increases from 144.3 fC for 1.0 μm thick n^+ layer to 366.3 fC for 3.0 μm thick n^+ layer. The charges collected by the collector and base, however, are approximately independent of the n^+ layer thickness. The emitter charge collection, is negligibly small compared to base and collector charge collections.

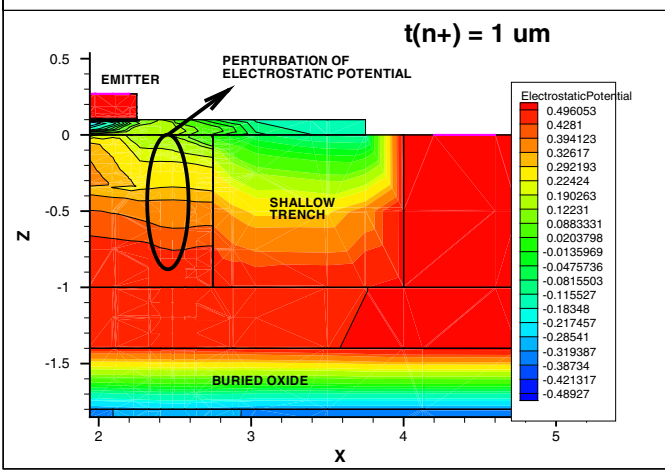


Fig. 5. Electrostatic potential contours at 9 ps, for $t(n^+) = 1 \mu\text{m}$.

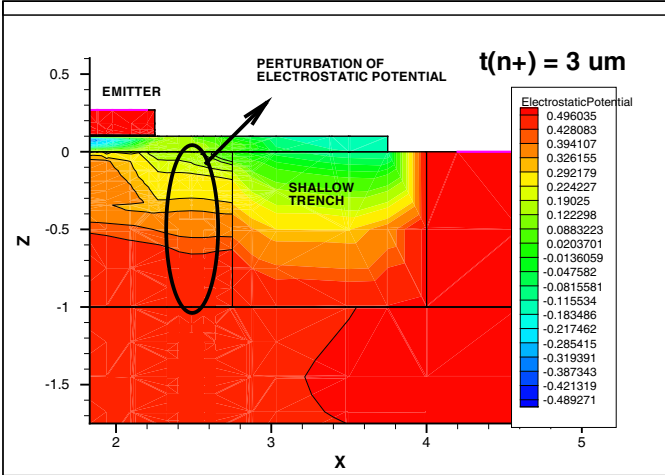


Fig. 6. Electrostatic potential contours at 9 ps, for $t(n^+) = 3 \mu\text{m}$.

The weak dependence of charge collection on n^+ layer thickness is attributed to the heavy doping of the n^+ layer. The passage of the ion causes an electrical field perturbation in the collector-base junction, or funneling of the potential distribution. Owing to the heavy doping of the n^+ layer, the funnel does not penetrate deep into the n^+ layer. As a result, charge collection occurs primarily above the n^+ layer, leading to the weak dependence of charge collection on n^+ layer thickness. Fig. 5 and Fig. 6 show the simulated electrostatic potential contours at 9 ps for the $t(n^+) = 1 \mu\text{m}$ and $t(n^+) = 3 \mu\text{m}$ devices, respectively. The top portions of the HBT are zoomed to better visualize the potential perturbation in the collector-base junction. The buried oxide cannot be seen in Fig. 6 because of the thickness of the n^+ buried layer. The pertur-

bation of potential for the $t(n^+) = 1 \mu\text{m}$ and $= 3 \mu\text{m}$ HBTs are approximately the same. In both cases, the perturbation is confined within 0.1 μm above and 0.8 μm below the collector-base junction interface. To a large extent, this potential perturbation determines the amount of charge collection through drift. The nearly identical perturbation of potential for two devices with different n^+ layer thickness is responsible for the independence of charge collection on the n^+ layer thickness.

Assuming that all of the charges deposited within the potential funnel are collected through drift, a first order estimation of the charge collected can be made by calculating the product of the LET and the length of the potential funnel [8]. In this case, the lengths of the potential funnels are 0.9 μm according to the simulated potential distributions (Fig. 5 and Fig. 6). With an LET of 0.1111 pC/ μm , the estimated amount of charge collection is 135.2 fC. This is quite close to the simulated numbers shown in Table I, which is from 133 to 136 fC for different n^+ thicknesses.

B. Load dependance

To examine the impact of load on charge collection, simulations are performed on the 1.0 μm thick n^+ layer structure using different loads. The collector terminal is loaded with a resistor (R_L) in parallel with a capacitor (C_L) of 1 pF. $R_L = 0, 1 \text{ k}\Omega$ and $2 \text{ k}\Omega$ are simulated.

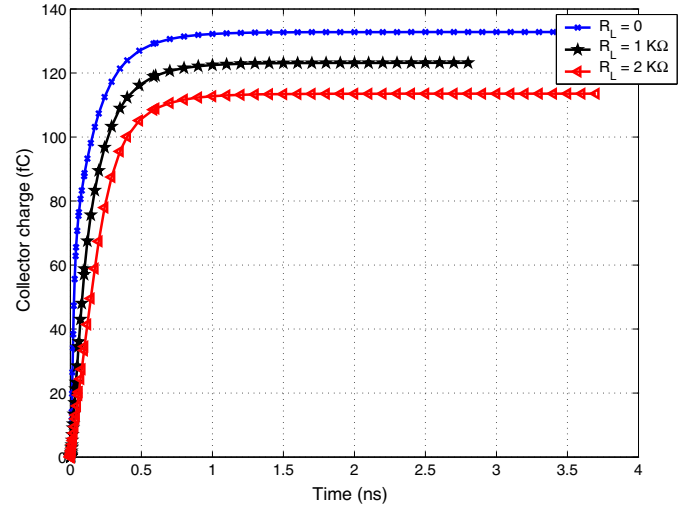


Fig. 7. Charges collected by collector terminal as a function of load resistor.

TABLE II
CHARGE COLLECTION FOR DIFFERENT LOADS ON COLLECTOR.

	$Q_{\text{collector}}$	Q_{base}	Q_{emitter}	$Q_{\text{substrate}}$
No Load	133 fC	-133 fC	0.27 fC	0.042 fC
1 k Ω Load	123 fC	-129 fC	5.8 fC	0.031 fC
2 k Ω Load	114 fC	-127 fC	13 fC	0.048 fC

Figs. 7 and 8 show the resulting charge collection for the collector and emitter, respectively. The charge collected by the collector decreases with increasing R_L . The charge collected by the emitter, however, increases with increasing R_L . This load dependence is similar to that in bulk SiGe HBTs [9]. The sum of the collector

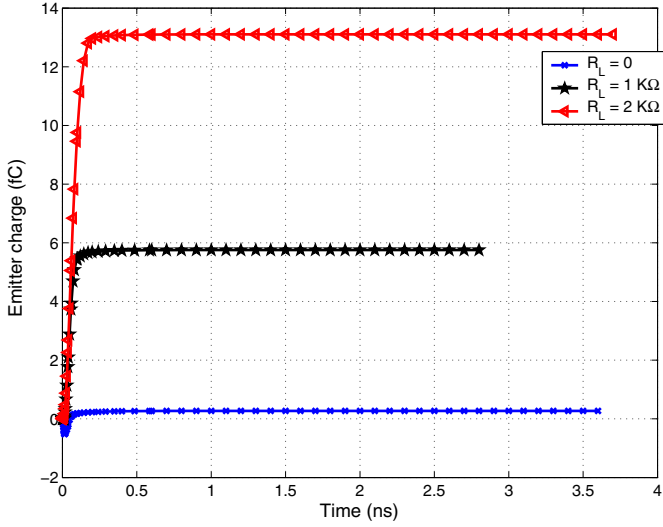


Fig. 8. Charges collected by emitter terminal as a function of load resistor.

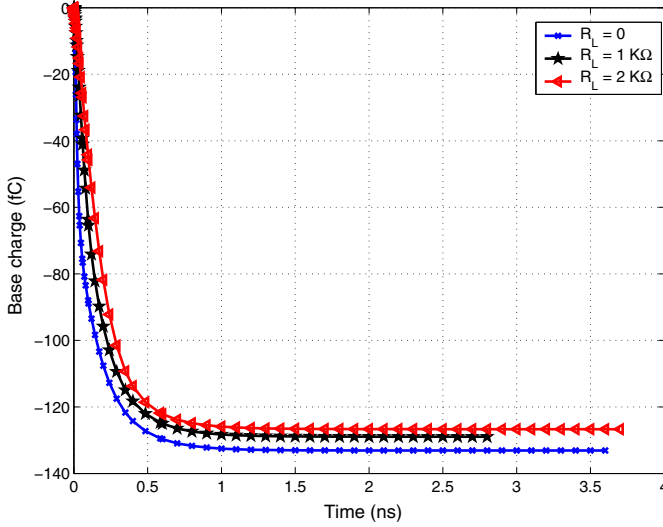


Fig. 9. Charges collected by base terminal as a function of load resistor.

and emitter charges decreases slightly with increasing R_L . The increase of R_L also increases the time of charge collection, as can be seen from Figs. 7 and 8. Figs. 9 show the resulting charge collection for the base. Table II summarizes the charges collected by the terminals for different R_L .

The electrons deposited can exit the device through the collector and emitter. An increase in the load on the collector directs more electrons towards the least resistive emitter. Hence the charge collected by emitter increases with increasing R_L . With increasing R_L , exit of charges from the device is more difficult, leading to a longer charge collection time and more carrier recombination. Increased recombination leads to a decrease of the total charge collection with increasing R_L .

V. COMPARISON WITH BULK HBT

A logical question is how the charge collection characteristics in SOI HBT compare to those in a bulk HBT. To answer this ques-

tion, we repeated the same simulation on the bulk counterpart of the SOI SiGe HBT discussed above. The substrate is grounded here, which represents the best case, as in circuits the substrate is always tied to the most negative potential, e.g. -5.2 V. In a bulk device, charge collection depends on the range of ion [9]. In this case, the range of the 1 GeV Fe ion is several hundred microns. In our simulation, only the first 25 μm of the bulk device is simulated due to simulator constraints. This is not exact, but should be sufficient for our purpose.

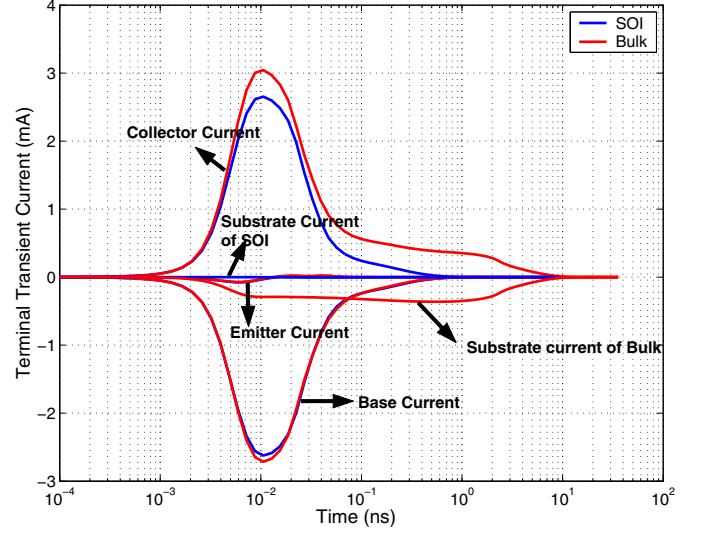


Fig. 10. Comparison of terminal transient currents between bulk and SOI devices.

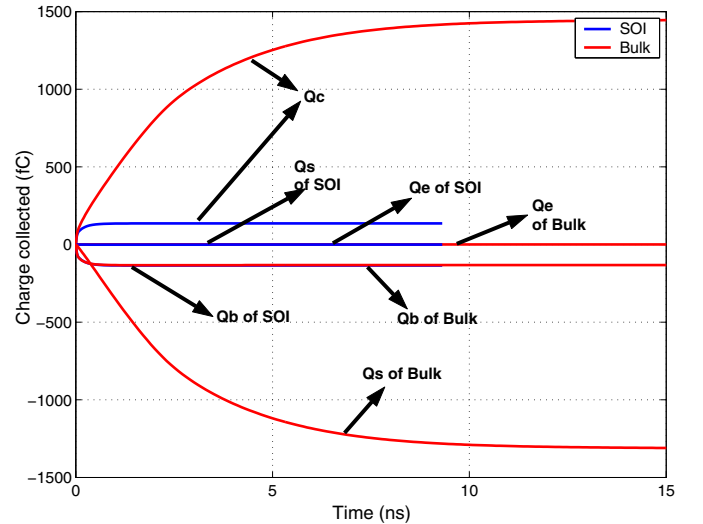


Fig. 11. Comparison of terminal charge collection between bulk and SOI devices.

A. Collector/substrate comparison

Fig. 10 shows the terminal currents for the bulk and SOI SiGe HBTs up to 10 ns. For the SOI HBT, the transient collector current decays to zero at 1 ns. For the bulk HBT, the collector current decays to zero at 9 ns. The substrate current is negligible in the SOI HBT at all times due to the absence of collector-substrate

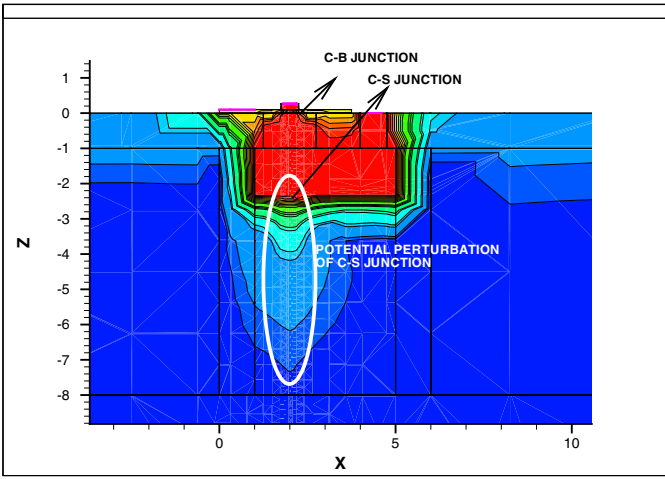


Fig. 12. Potential contours in the bulk structure at 7 ps.

junction. For the bulk HBT, the substrate current decays to zero at 9 ns.

Fig. 11 compares the bulk and SOI terminal charge collection characteristics up to 15 ns. The charge collection is complete in 0.8 ns in the SOI HBT while the charge collection is complete in 10 ns in the bulk HBT. The charge collected in the bulk HBT is 10 times the charge collected in the SOI HBT. For the SOI HBT, the substrate charge collection is negligible. For the bulk HBT, substrate charge collection is appreciable and comparable to the collector charge collection.

Fig. 12 shows the potential contours in the bulk HBT at 7 ps. The disturbance in the collector-substrate junction potential goes deep into the substrate which is why the collector charge collection is much higher in the bulk HBT than in the SOI HBT. The deep penetration of the potential perturbation into the substrate is primarily due to the light doping of the p-type substrate. For the same reason, charge collection takes a much longer time in the bulk HBT than in the SOI HBT. In bulk HBT, electrons are collected by the collector and holes are collected by the substrate, through the perturbation of the potential in the collector-substrate junction. On the contrary, in SOI HBT, the substrate collects negligible charge due to the removal of collector-substrate junction. If collector is the sensitive node, SOI HBTs offer significant advantage over bulk HBTs.

B. Base/emitter comparison

Interestingly, the base and emitter currents are virtually the same for the SOI and bulk SiGe HBTs. The base and emitter charge collection are about the same for the bulk and SOI SiGe HBTs. Base charge collection is complete within 0.8 ns in both bulk and SOI HBT and emitter charge collection is complete within 0.1 ns in both bulk and SOI HBT.

The reason for the similar base and emitter charge collection characteristics in the bulk and SOI HBTs is the decoupling of the charge collection in the active $n^+/p/n$ emitter-base-collector layers from the charge collection in the n^+ buried layer to p-substrate junction. Fig. 12 shows the potential perturbation in the collector-substrate junction and collector-base junction. The potential perturbation of the collector-base junction is confined

within $0.8 \mu\text{m}$ below the collector-base junction. An undisturbed n^+ buried layer is sandwiched between the collector-base junction and the collector-substrate junction. The potential perturbation in the collector-base junction is essentially decoupled from the potential perturbation in the collector-substrate junction. This decoupling is physically enabled by the heavy doping of the n^+ buried layer. The potential perturbation in the active $n^+/p/n$ emitter, base, and collector layers in the bulk and SOI HBTs are identical, as confirmed by the simulation details. As a result, the emitter and base charge collection characteristics are about the same in the bulk and SOI HBTs. If the base and emitter are the sensitive nodes of the circuit, SOI HBT offers no advantage over bulk HBT in terms of charge collection.

VI. CONCLUSION

We have presented 3-D simulation of heavy ion induced charge collection in SiGe HBTs on SOI. The charge collection is found to take place above the n^+ buried layer. As a result, thinning the n^+ buried layer does not help reducing the charge collection. The load dependence of the charge collection is found to be similar to that for bulk HBT. Comparison with bulk HBT shows that the emitter and base charge collection characteristics are similar in bulk and SOI HBTs, due to decoupling of the charge collection in the $n^+/p/n$ intrinsic device and the charge collection in the n^+/p collector to substrate junction. SiGe HBT on SOI is effective in reducing the collector charge collection, thanks to the removal of the n^+ buried layer to p-substrate junction, as well as the heavy doping of the n^+ buried layer.

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