BAE SYSTEMS

Reconfigurable, High Density, Gigahertz Speed Low Power Radiation Hardened FPGA Technology

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27- 29 November 2007

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BAE/Achronix RHFPGA Program

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- Background
- Introduction
  - Achronix Company
  - Achronix FPGA Overview
- BAE/Achronix Radiation Hardened Test Chip Data
- BAE/Achronix RHFPGA Program Overview
  - Product Features
  - Product Development Strategy
- Summary

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RHFPGA Roadmap

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Legacy ONO Antifuse Based RHFPGA

- 5V Legacy Product: ***Actel*** RH1020 and RH1280 FPGA's
- Production stopped in 2002; Build-out Inventory - exhausted
- Significant product demand continues
- Actions being taken: Re-install FPGA process into recently modernized foundry; Restart production.

Next Generation M2M Antifuse Based RHFPGA

- ***Actel*** RTAX FPGA's are being used in space missions
- Rad Hard (RHAX) FPGA's are better suited for certain missions
- Actions being taken: Migrate RTAX FPGA designs to RH foundry to build RHAX FPGA equivalents; Start flight-qualified production.

Reconfigurable Reprogrammable RHFPGA

- Critical need exists for re-configurable/ re-programmable, rad hard FPGA's
- Actions being taken: Develop & demonstrate Multi-million gate RHFPGA using ***Achronix*** fabric built on radiation hardened process/designs.

Background

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- Program History
  - Investigated Achronix Base Technology Starting in 2006
  - Test chips fabricated & successfully tested for SEU in 2007
  - BAE/Achronix Joint Development Program started under government funding in 2007

- Program Goal
  - Develop a SRAM based Multimillion Gate Reconfigurable Radiation Hardened FPGA based on Achronix architecture using BAE's Radiation Hardened Process Technology

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Introduction

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Achronix Company Overview

- Well funded, privately held fabless semiconductor company
- Founded in New York in 2004
- Headquarters moved to San Jose in 2006, retained New York R&D lab
- Working 90nm and 180nm prototype silicon
- Series of Patents protect key IP
- Partnerships with Major Fabs, IP and EDA vendors

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Achronix Commercial FPGAs

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- Standard SRAM-based FPGA fabric
- Embedded multipliers and memory blocks
- Pipelined implementation for high frequency operation (> 1 GHz)
- Pipelining is transparent to designers
  - Designers write standard VHDL/Verilog
- Industry-standard I/Os

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Achronix FPGA Architecture

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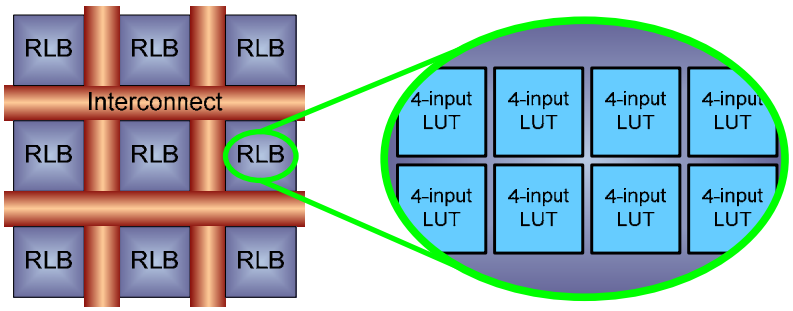
Familiar Silicon & Familiar Tools

Familiar Silicon

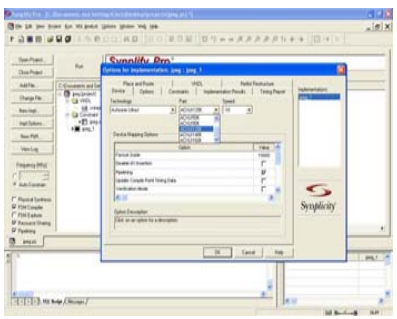
- Traditional 4-input LUT architecture
  - With GHz performance

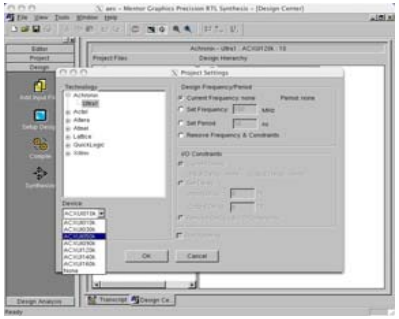


- SRAM-based reprogrammable FPGA
- Requires no knowledge of underlying technology

Familiar Tools

- SYNP Synplify-Pro and Mentor Precision Synthesis Flows





- Full compatibility with existing third party simulation, debug, and verification tools

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Achronix CAD Environment (ACE)

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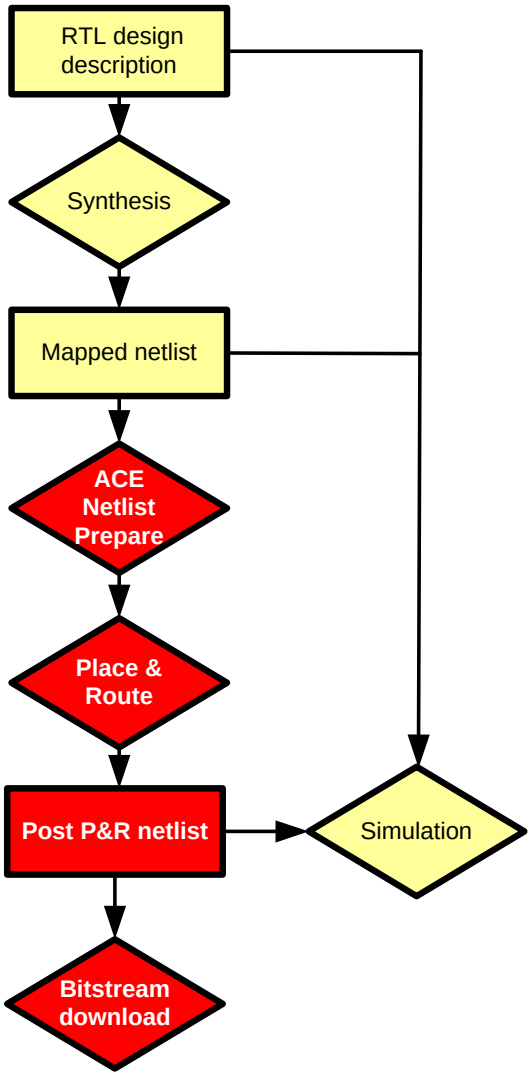

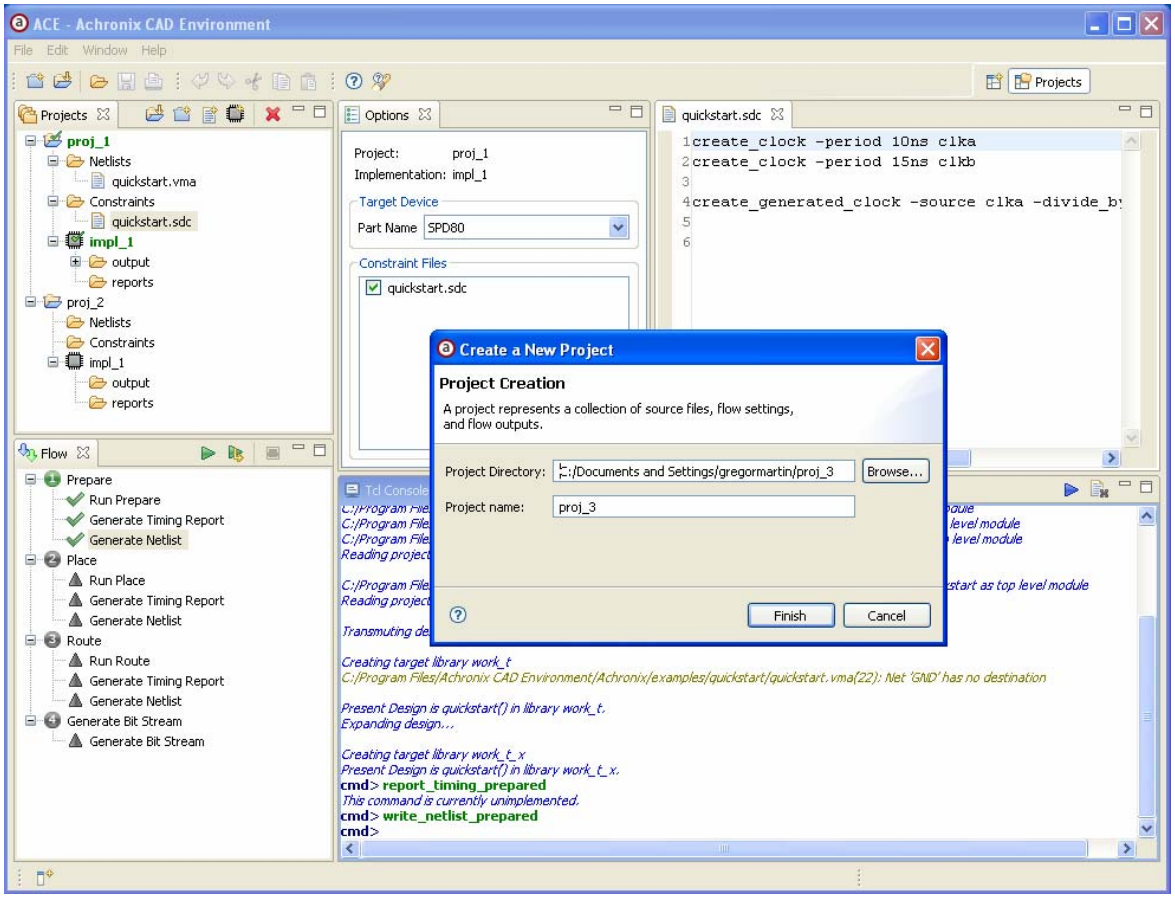

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Achronix FPGA History

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- 180 nm prototype (Sep 2005)
  - **674 MHz**
  - World's fastest CMOS FPGA by 2x
- 90 nm prototype (Apr 2006)
  - **1.93 GHz**
  - World's fastest CMOS FPGA by 5x

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Achronix 90nm FPGA Summary

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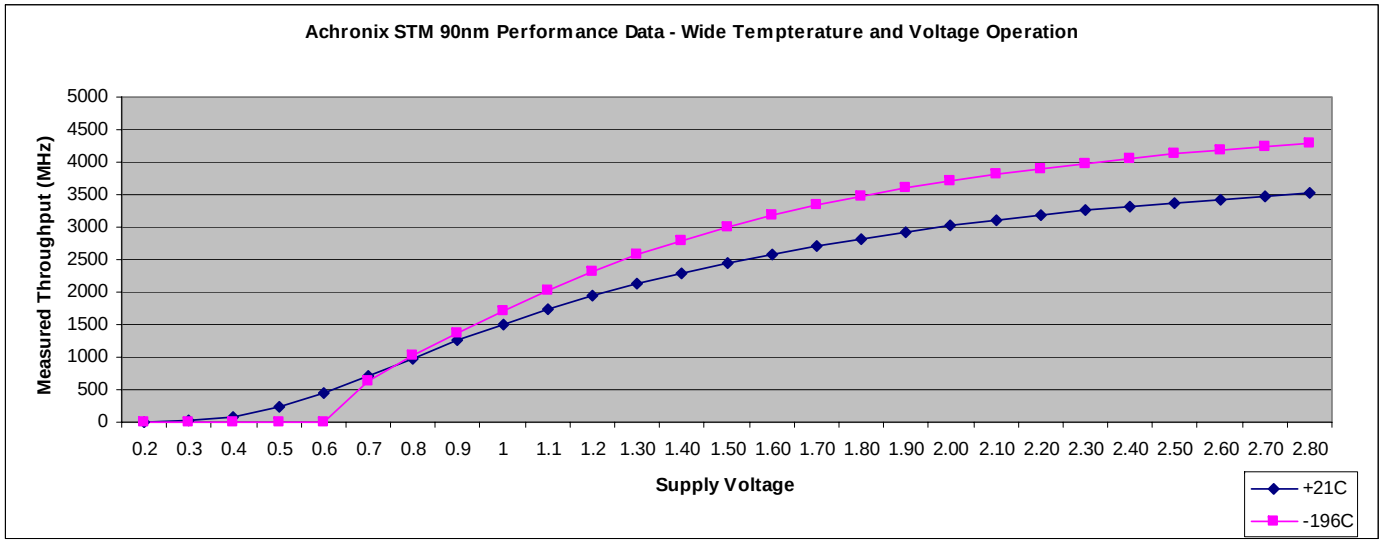

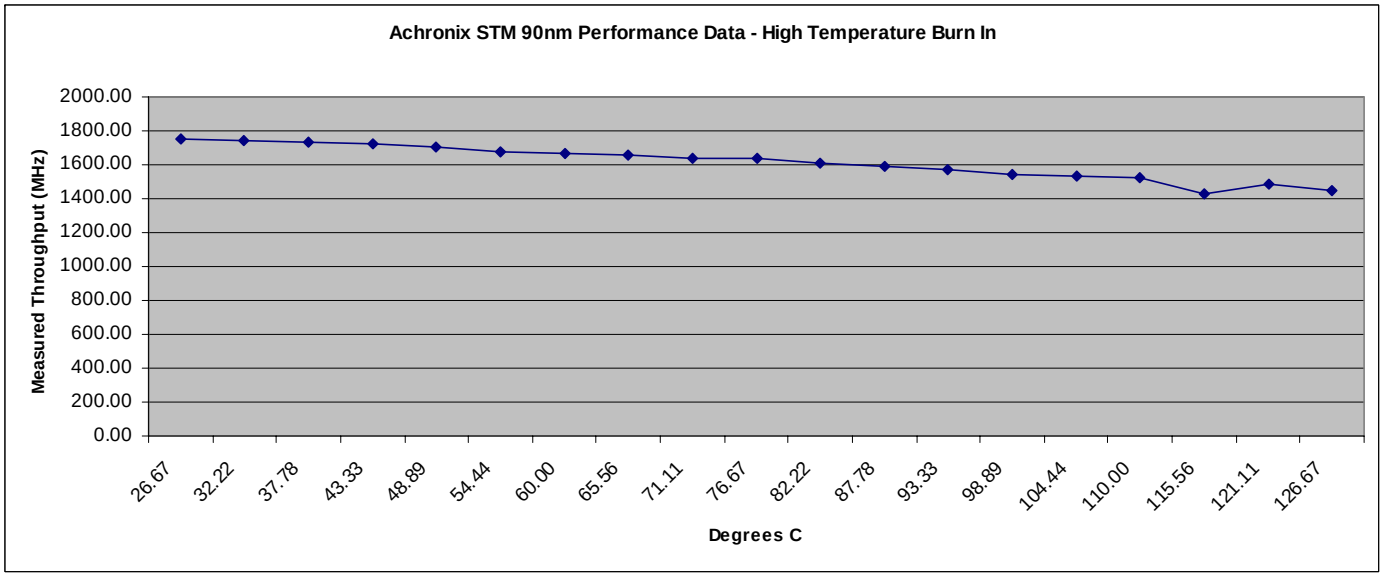

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SEU Mitigation

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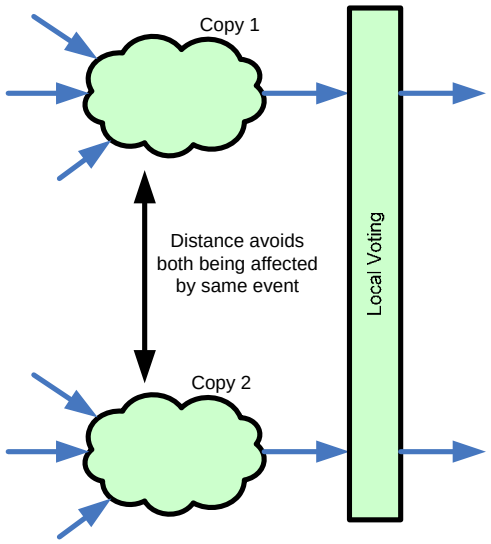
Achronix patented Redundancy Voting Circuits (RVC) SEU mitigation

- Redundancy Voting Circuits (RVC)
  - Two copies of all circuits implemented
  - Copies are non-adjacent avoiding the risk of a single upset affecting both
  - Every stage (combinatorial and state) has local voting mechanism



- Local voting waits until both copies agree
  - no SEU, no delay
  - If SEU on either, circuit resolves to the correct value after event energy dissipates

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BAE/Achronix RHFPGA Test Chip

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RHFPGA Test Site

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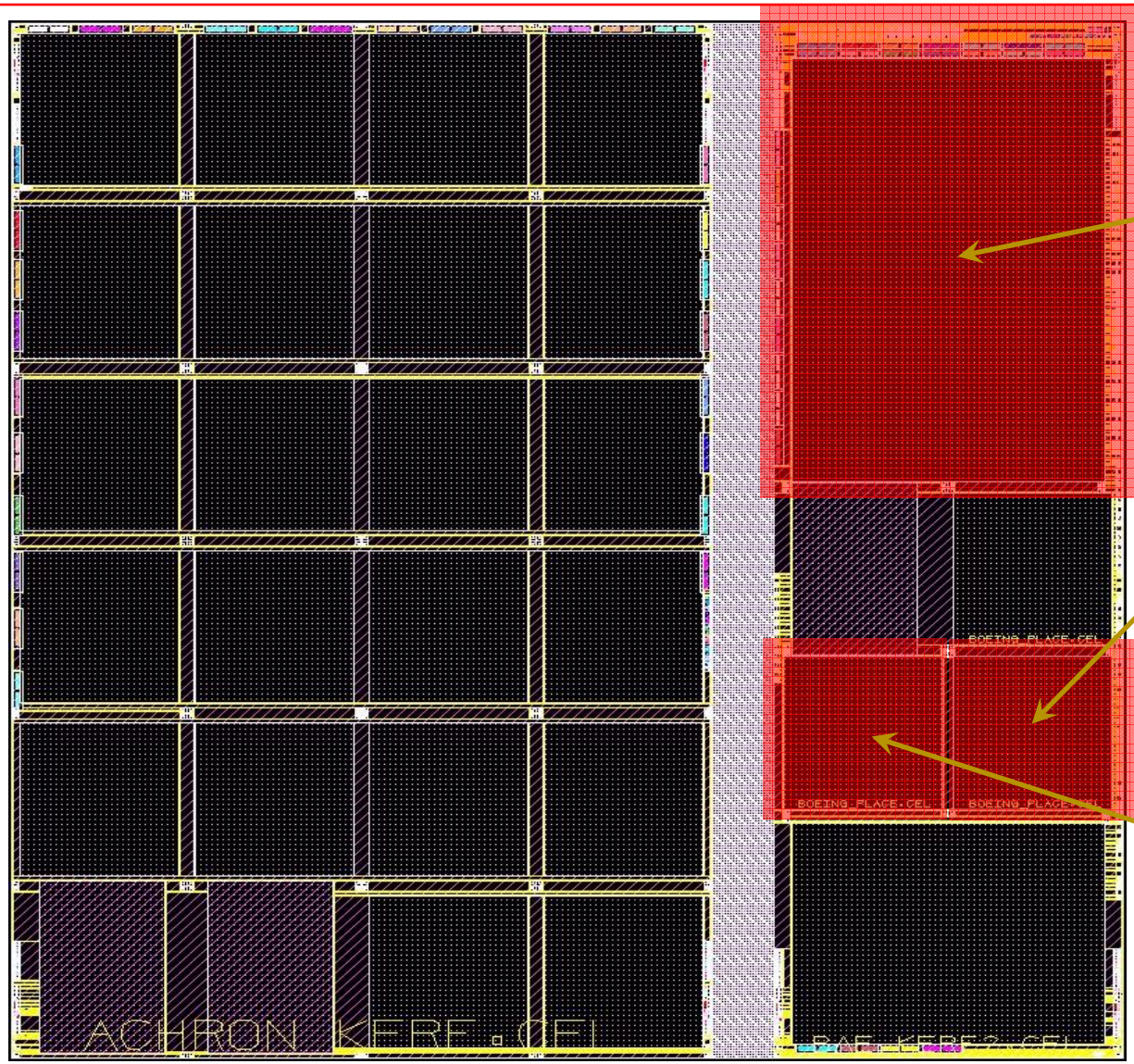

BAE-Achronix 54 mm^2 RADHARD FPGA

Low density design, 27K gate, 250 MHz, reconfigurable

BAE-Achronix 9 mm^2 RADHARD FPGA with BAE hard SRAM cells

Low density design, 4K gates, 250 MHz reconfigurable

BAE-Achronix 9 mm^2 RADHARD FPGA with Achronix hard SRAM cells

Low density design, 4K gates, 250 MHz reconfigurable

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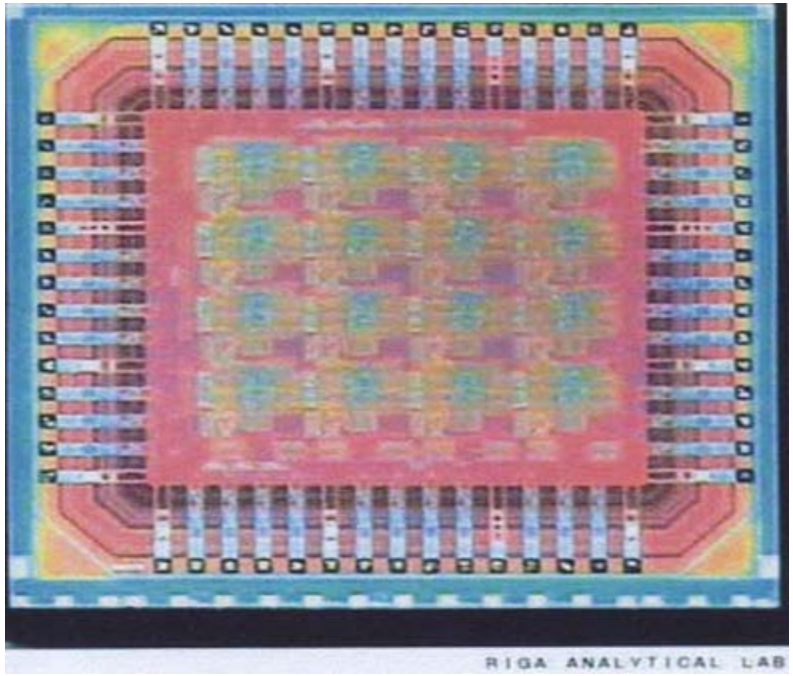
BAE-Achronix 3x3 RADHARD Testsite



BAE RADHARD FPGA Test Site Results

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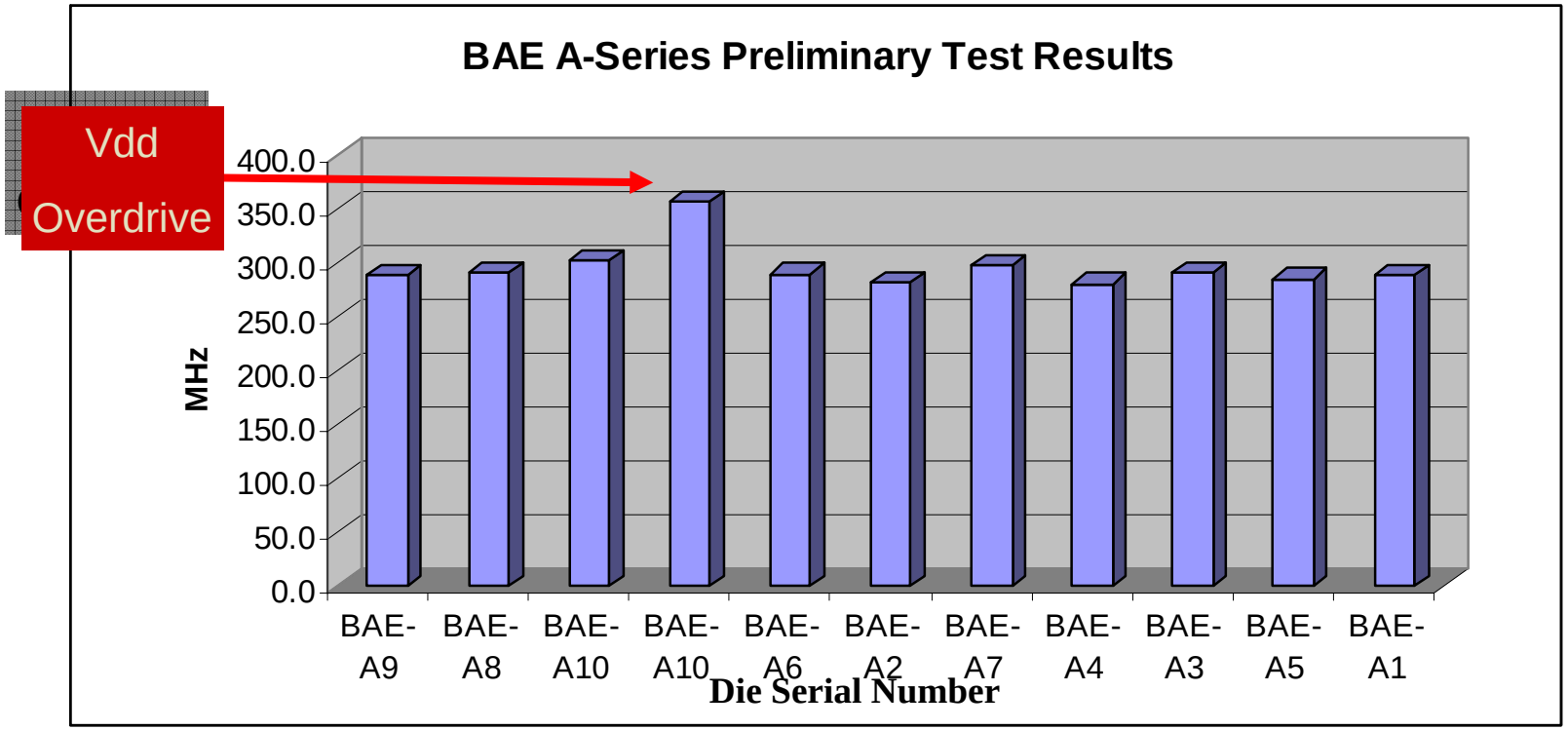

Design SPICE results predicted 275 MHZ – We averaged 289.3 MHz

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Test Site Performance and Power Summary

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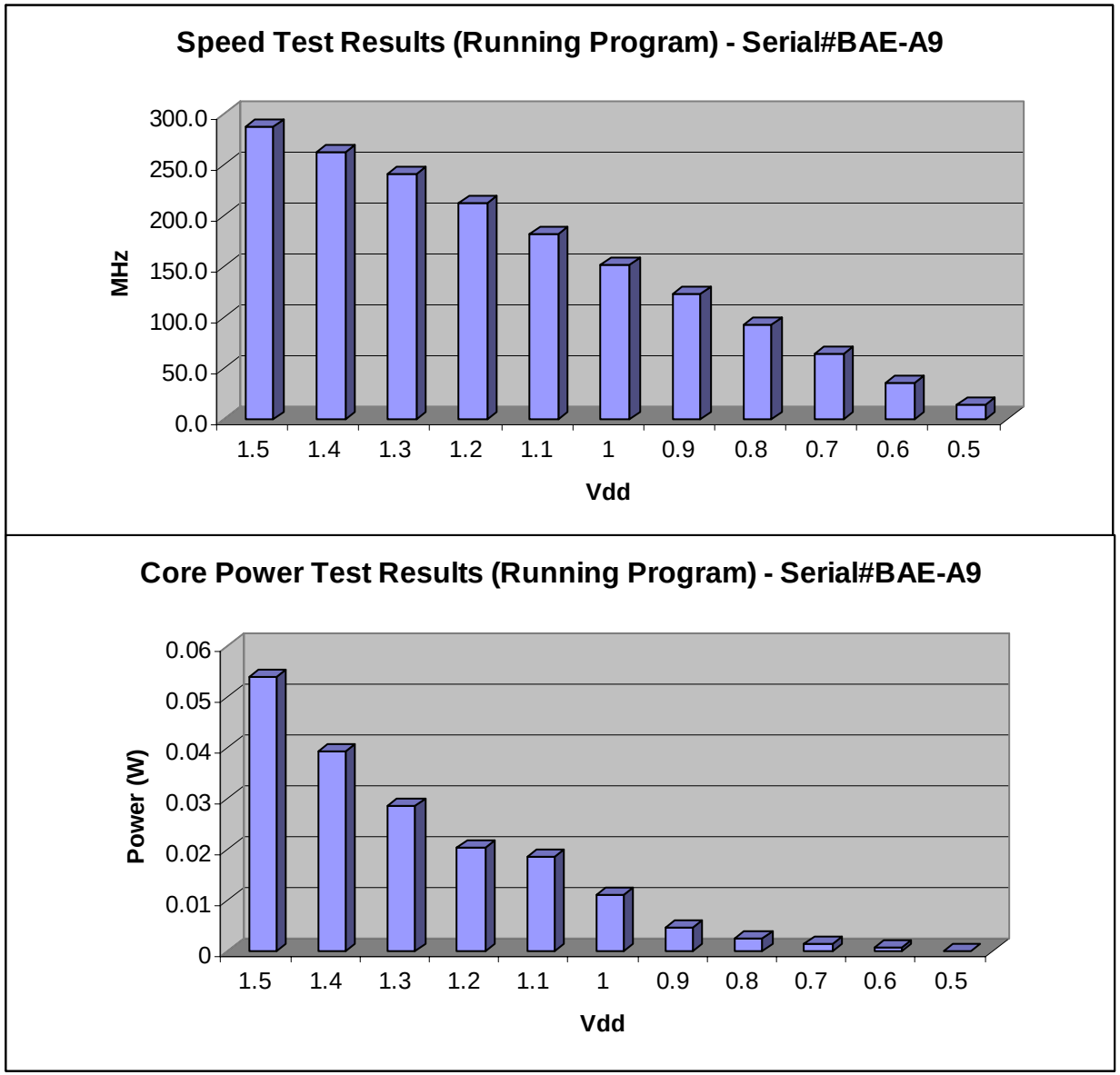

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Radiation Test Overview

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- The Test Chip contained a 4x4 array of FPGA Tiles implemented with RVC
- One dedicated tile had an 8 bit counter (implemented in RVC) on output acknowledge to observe the functioning of the various FPGA configurations at a reasonable frequency with standard I/O
- Five different FPGA patterns were utilized during testing running at different frequencies (37 MHz to 290MHz)

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SEU Test Summary

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- Testing completed at Texas A&M Cyclotron with Argon (0°), Krypton(0° and 45°), and Xenon (45°) did not cause any of the 5 patterns to lock-up or fail
- No observed SET or SEU events in SEE testing up to an effective LET threshold of 58 MeV-cm²/mg
- This testing validates that the Achronix Redundancy Voting Circuits (RVC) are achieving the intended goals

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BAE/Achronix RHFPGA Product

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RHFPGA Product Approach

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- RH15 Radiation Hardened Process
- RH15 RH SRAM
  - Configuration Memory
  - Block RAM (BRAM)
  - Registers
- Synchronous Frame
- ESD resistant Programmable I/Os
- PLL

BAE RH15 Radiation Hardened Technology

- FPGA Fabric
  - Reconfigurable Logic Blocks
  - Redundancy Voting Circuits
  - Block RAM Wrapper
  - Multipliers
  - Routing Resources
- Synchronous/Asynchronous Wrapper

Achronix FPGA Architecture

Reconfigurable Radiation Hardened FPGA

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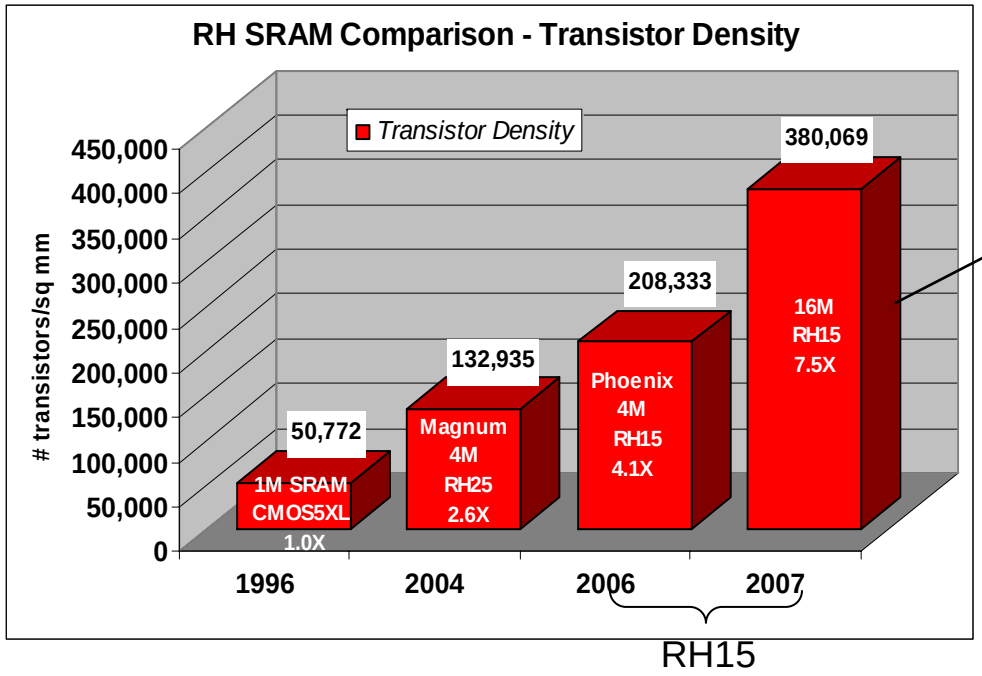
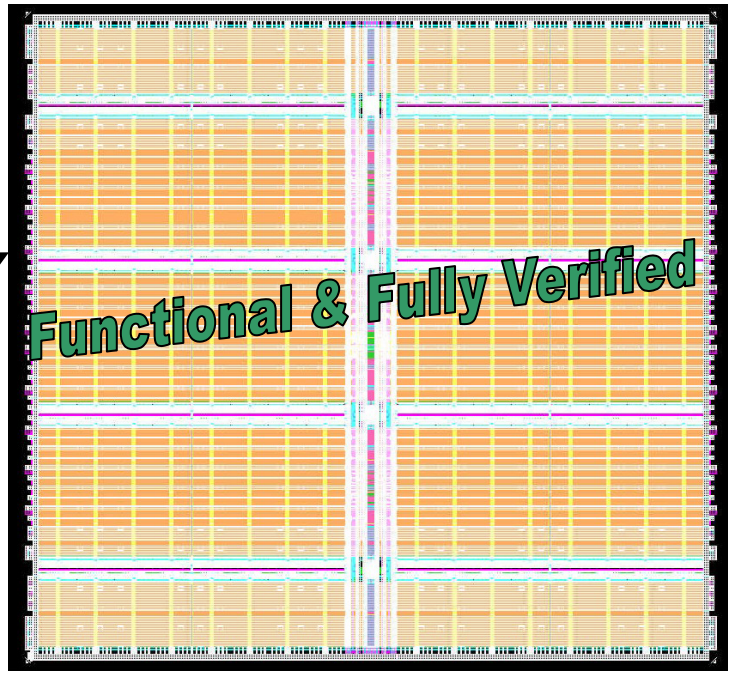
RH15 Density Capabilities





16M SRAM Chip Statistics

Transistors	113,070,511	Total ILCs	1,063,783,005
HVT NFETS	74,422,289	CA	298,967,451
HVT PFETS	38,645,756	CT	226,146,395
DGO NFETS	1,630	V1	212,067,749
DGO PFETS	836	V2	242,233,858
R2 Resistors	36,410,528	V3	82,209,612
Q2 Capacitors	18,205,264	V4	1,011,258
		V5	506,746
		V6	639,936

> 113 Million Transistors; > 1 Billion Inter-Level Connects; 176 meters of Resistor
16M SRAM is the highest density part built in Manassas

RH15 Performance Capabilities

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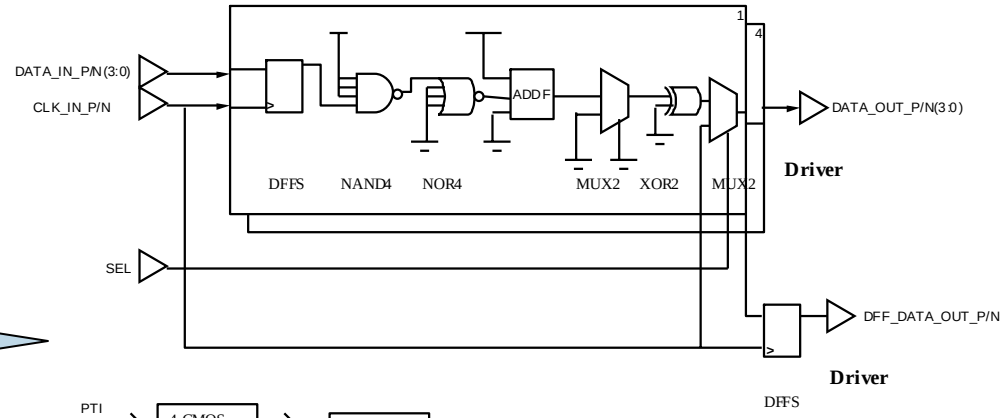
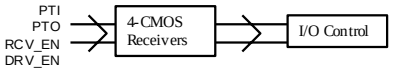
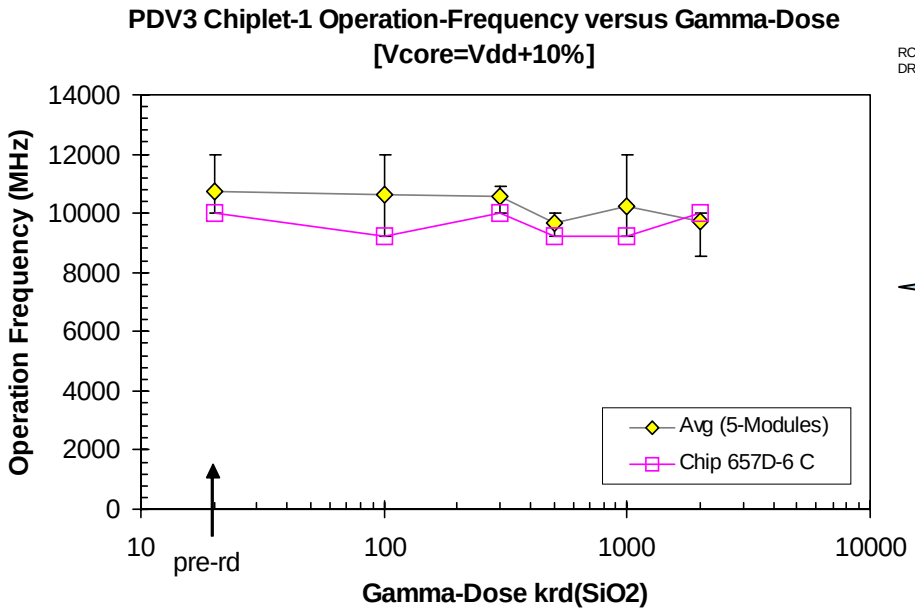
High Speed Circuit Testing
to measure on-chip gate delay.

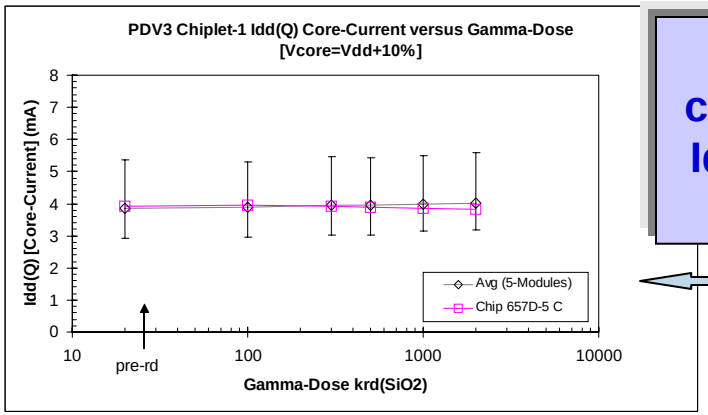
Logic Representation of High Speed Signal Paths







Results confirm >1GHz performance both pre- and post-irradiation (2 Mrd(SiO_2))



No change in Iddq with dose.

RHFPGA Features

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- Reconfigurable Radiation Hardened FPGA for military, aerospace and industrial applications
- Leverages standard RTL: Eliminates need for TMR design & tools
- High Performance FPGA (Up to 350 MHz)
- Total Dose Hardness through $1x10^{6}$ rad(Si)
- Single Event Error Rate of < $1x10^{-11}$ upsets/bit day
- Operating Temperature
  - -55°C to 125°C (Ambient)
  - Extendable to Extreme Temperatures
- Independently Configurable IO (PCI Compatible)
  - Low Voltage TTL/CMOS
  - LVDS
  - SSTL, HSTL
- Existing FPGA EDA Tool Support (Synplicity & Mentor)

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RHFPGA Product Development Strategy

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- Implement design using BAE Systems Radiation Hardened Process Technology Features
- On-chip memory structures
  - Replace Standard SRAM with BAE Systems RADHARD SRAM
- Circuit methodology
  - Use Achronix Redundancy Voting Circuit (RVC) and self-correction capability to actively correct upsets and transients
- Space apart critical nodes to reduce double-error probability

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ACX RHFPGA Program Overview

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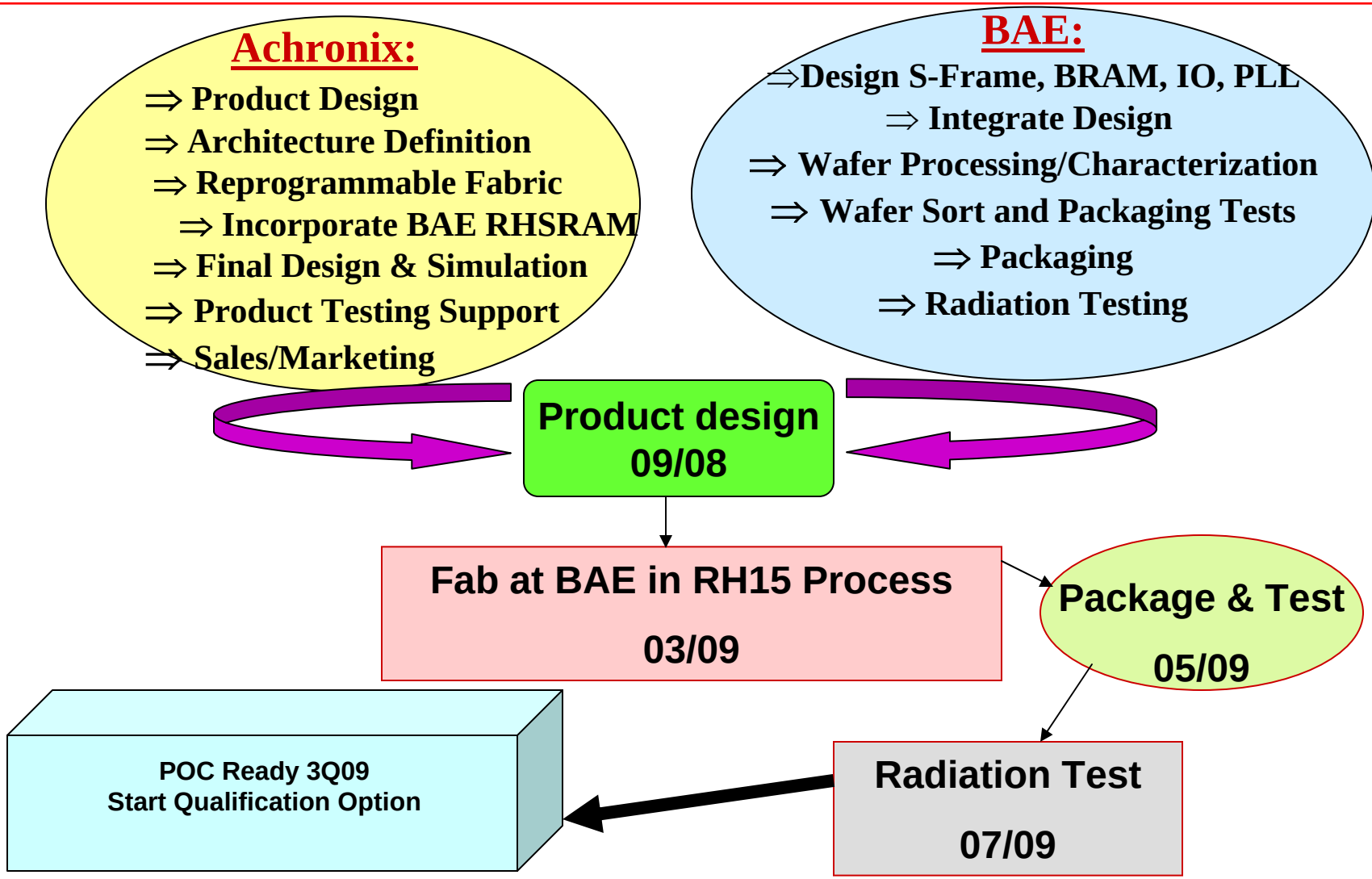

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RH15 CMOS Technology Features

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Key Features

Features:	RH15
Isolation	STI
Thin Oxide / DGO Devices	26 Å / 70 Å
Vdd Options	1.5 V / 1.8 V / 3.3 V
Metal Levels	7
Capacitors	Yes
Resistors	Yes
C4 / Wirebond	Y/Y

Radiation Hardness Assurance Levels

Environment	
Total Dose (rad(Si))	1M
SEU (errors/bit-day)	1E-11
SEL (MeV-cm2/mg)	120
Neutron Fluence (n/cm2)	1E13
Prompt Dose Upset (rad(Si)/s)	1E9
Prompt Dose Survival (rad(Si)/s)	1E12

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RH15 Performance Parameters Test Results

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Parameter	Goal	Threshold	Test Results	Status	Comments
Operating Voltage	1.5, 1.8 and 2.5V	1.5, 1.8 and 2.5V	1.5, 1.8 and 2.5V	Complete	*Goal level achieved.*
Operating Temp					
• Full Performance	0 - 80C	0 - 80C	0 - 80C	Complete	*Goal level achieved.*
• Functionality	-55 - 125C	-55 - 125C	-55 - 125C	Complete	
Operating Speed Worst Case and Post Radiation	1GHz	500Mhz	> 3GHz	Complete	*Goal level achieved.*
Total Ionizing Dose (rd(Si))	= 1M	= 500K	> 2M	Complete	*Goal level achieved.*
Single Event					
• Upset (errors/bit-day)	<1E-11	<1E-10	3.4E-11 S-ASIC, <<1E-12 SRAM	Complete	*Goal level achieved.*
• Latchup (MeV-cm2/mg)	>120	>100	>127	Complete	*Goal level achieved.*
Neutron Radiation (n/cm2)	>1E13	>1E12	>1E13	Complete	*Goal level achieved.*
Dose Rate (rd(Si)/s)					
• Upset	>1E10	>1E9	2.2E9	Complete	*Threshold level achieved.*
• Survivability	1E12	1E12	1E12	Complete	*Goal level achieved.*

RH15 KPP testing and verification successfully completed

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RHFPGA Package

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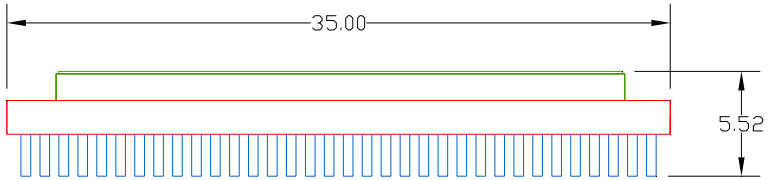
Base Package: (Developed for FG-HPSC (OGA)

- Ceramic Column Grid Array
  - Flip Chip Ceramic Column Grid Substrate (CCGA)
  - Hermetic Seam Weld Sealing
  - Substrate: 35 x 35mm
  - 34 x 34 Column Array
    - 1.0mm pitch
    - 1144 Total I/O
      - 840 signal
      - 304 Vdd and Gnd
  - Die site accommodates up to 20 mm Die



RHFPGA Package Plans:

- Package Modeling – 10/08 – 12/08
- Update Substrate Design & Verification – 12/08 – 2/09
- Package Availability – 4/09

Package to be Modified to Accommodate Programmable I/O Features

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Summary

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- Test Site
  - Electrical performance matches simulation (289 MHz)
  - Preliminary SEU Radiation testing performed by NASA
  - Data shows no SEU observed up to LET of 58 at 0° & 45° angles of incidence
- RHFPGA Program
  - Technical Goals of the Program Established
    - Build a multimillion reconfigurable RHFPGA using:
      - Achronix patented architecture
      - BAE's RADHARD process technology
  - Preliminary Product Requirements defined
  - Program Plan in place
- Design Activity underway
  - Defined Design Approach Methodology
  - Defined Specification details for BRAM, S-Frame, I/O, PLL.

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