Heavy Ion Testing of the BAE Chalcogenide Nonvolatile Memory Test Chip (CTCV)

Timothy Oldham[1], Hak Kim[2], and John Rodgers[3]
1. QSS Group, Inc., Seabrook, MD 20706
2. Jackson and Tull Chartered Engineers, Washington DC 20018
3. BAE Systems, Manassas VA 20110

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I. Introduction

The purpose of the test was to determine the SEE response of the BAE chalcogenide (phase change) nonvolatile memory. The samples were exposed to heavy ion beams at the Texas A&M University cyclotron.

II. Devices Tested

The test chips were engineering samples of the CTCV (chalcogenide technology characterization vehicle) test chip, fabricated on the BAE 0.5-micron line in the Spring 2002, shortly before the line was shut down for upgrading. The samples have four arrays of 64K cells, each. BAE has decided to concentrate on the cell designs in arrays B and D in future development, so we concentrated on those arrays in the test, too. The difference between the two arrays is in the sensing scheme—array B uses a single ended sense amp, and array D pairs two cells in a differential configuration. Therefore, array B has 64K bits, and array D has 32K bits. Two samples were tested, one for Array B, and one for array D. The nominal power supply was 3.3 V, but some shots were taken with the power removed, to test the non-volatility of the memory.

III. Test Facility

The cyclotron was tuned to 15 MeV/nucleon, and two ions (Au and Xe) were used. Most of the exposures used Au as the incident ion, because it had the highest LET available. Fluence was 10^7 particles/cm^2 in all exposures, and average flux varied from 4.27×10^4 to 2.38×10^5 particles/cm^2-s.

Ion	Energy (MeV)	LET(MeV/mg/cm^2)	Range (?m)
Xe	1176	55	92
Au (normal)	1695	89	91
Au (40?)	1695	116 (effective)	67 (effective)

IV. Test Methods

The NASA test system was built to be as similar as possible to the BAE test system. Hak Kim of NASA and Jon Maimon of Ovonyx/BAE consulted frequently, for that purpose. Patterns that could be written were all zeroes, all ones, and checkerboard. Tests were static, dynamic read, and dynamic write. In static tests a pattern was written, the sample was irradiated, and changes in the stored pattern (if any) were recorded. During dynamic read tests, a pattern was stored before the exposure, and read continuously during the exposure. During dynamic write tests, a pattern was alternately written, read, rewritten, read again, and so on during the exposure.

V. Results

There were no unambiguous static errors observed at any point in the testing. In the first set of static tests on Array B of the first sample, no static errors were observed, with Au ions normally incident (LET =89). On Array D of the second sample, no errors were observed at the highest LET (116), where one would most expect them. There were a number of intermittent problems with the test system during this test. Three of the sixteen bits in each word either did not work initially, or malfunctioned intermittently during the test, producing large numbers of errors even with the beam blocked. Results from those three bits have been deleted in this discussion. In other cases, noise apparently caused errors to be detected with the beam blocked. A few apparent static upsets were observed, but they were probably due to this noise. For Array D, for example, all the upsets were at lower LET than the tests with no upsets. Obviously, one would not expect the error rate to increase for less stressful test conditions. These results are roughly consistent with BAE results, where no upsets were observed under any condition, with testing up to LET = 98.

In previous testing, BAE had reported two kinds of errors in dynamic read testing [1], that is, two different kinds of SET. First, with zeroes (the high resistance/low current state) written, a current transient could cause the system to sense high current (a one). Subsequent read cycles would read correctly, indicating that the contents of the cell were not changed. They called these events false reads, and false reads of ones (that is, zeroes read as ones) were strongly preferred. Second, they observed one case of a false write, where the cell contents were changed, during a read. A one was rewritten to a zero, in that case. The pulse to write a zero is much narrower than the pulse to write a one, so an ion-induced transient could simulate a write pulse for a zero, but not for a one. Our results for Array B are very similar. At LET = 89, we observed about 200 false read errors (zeroes read as ones) for each exposure of 10^7 particles/cm^2, but no false reads of ones. At LET = 55, the number of errors was reduced by perhaps 40%. That is, the SET cross-section for false reads is about 2E-5 at LET =89, and about 1.2E-5 at LET = 55. The lowest LET used in this test was 55, so the only conclusion we can draw about the threshold is that it was less than 55. However, we did observe one bit with two read one errors at LET = 116. We also observed one false write, of a one to a zero, very similar to the BAE result. In this case, the LET was 89, and the total fluence at LET = 89 or greater

was 2.2E8 particles, so the cross-section is about 5E-10, and the threshold LET is 89. We also observed some read one errors in Array D. In the differential configuration, one cell is written with the data true, and one cell is the data complement. These are normally read and compared. That is, each bit has a cell in the high resistance state, and one in the low resistance state. An error can occur when either one is misread or rewritten, so there should be no preferential tendency for errors in one direction rather than the other.

BAE conducted dynamic write testing, but concluded that the errors were due only to the dynamic read part of the cycle, which has been described above. The memory was written with the beam on, and read (also with the beam on) to see if the write was completed correctly. That is, the dynamic write test cannot be done without also doing the dynamic read. For Array B, our results are also qualitatively consistent with the dynamic read results alone, which have already been presented. No read/write one errors (that is, ones read as zeroes) were observed, regardless of LET. At LET = 89, about 80-90 read/write zero (zeroes read as ones) errors were observed for each exposure. At LET = 55, this error rate was reduced by a factor of 2-3. Some read/write one errors were observed in array D, but (again) both logical states of the bit correspond to a high resistance cell and a low resistance cell, the same physical state.

No latch-up (SEL) was observed at any point in the testing. The highest LET used in testing was 116, and the total number of particles, at LET = 116, was $6x10^7/cm^2$ for array B. Therefore, the maximum SEL cross-section is less than 2E-8 at LET =116.

VI. Recommendations

Although the test samples were engineering samples, and a long way from product chips, the underlying technology seems to be very robust for space applications. All the testing was done at LET well above that of the real space environment—it had to be in order to make anything happen. BAE believes the false write problem is due to a flaw in the write circuit, which will be easily corrected in the next version of the chip. Static upsets would not be expected in space, based on these results. The false read does not change the stored information, so it should be easily handled at the system level, even if it occurs.

Reference

1. J.D. Maimon, K.K. Hunt, L. Burcin, and J. Rodgers, *Chalcogenide Memory Arrays: Characterization and Radiation Effects*, IEEE Trans. Nuc. Sci., **NS-50**, 1878 (2003).

Table 1: Run Data

Exposure	Sample	Mfg	# of bits	Vdd	Temp	Freq	Test	Pattern	Ion	E(MeV)	LET(eff)	Range	Flux	Fluence	Angle	Errors	Xsec	Xsec per FF	TID	TID(cum)	Comments
1	w5/mod6/B	BAE	65536	3.3	25	0	Static	CB	Au	1695	88.6	91	4.63E+04	1.00E+07	0	0	0.00E+00	0.00E+00	1.40E+04	1.40E+04	
2	w5/mod6/B	BAE	65536	3.3	25	0	Static	0	Au	1695	88.6	91	4.27E+04	2.40E+06	0	0	0.00E+00	0.00E+00	3.40E+03	1.74E+04	BAD RUN - do not use
3	w5/mod6/B	BAE	65536	3.3	25	0	Static	0	Au	1695	88.6	91	4.40E+04	1.00E+07	0	0	0.00E+00	0.00E+00	1.42E+04	3.16E+04	
4	w5/mod6/B	BAE	65536	3.3	25	0	Static	1	Au	1695	88.6	91	4.70E+04	1.00E+07	0	0	0.00E+00	0.00E+00	1.42E+04	4.58E+04	
5	w5/mod6/B	BAE	65536	0	25	0	Static	CB	Au	1695	88.6	91	4.87E+04	9.98E+06	0	0	0.00E+00	0.00E+00	1.42E+04	6.00E+04	
6	w5/mod6/D	BAE	32768	3.3	25	0	Static	CB	Au	1695	88.6	91	4.75E+04	9.98E+06	0	0	0.00E+00	0.00E+00	1.42E+04	7.42E+04	
7	w5/mod6/D	BAE	32768	3.3	25	0	Static	1	Au	1695	88.6	91	5.35E+04	1.00E+07	0	0	0.00E+00	0.00E+00	1.42E+04	8.84E+04	
8	w5/mod6/D	BAE	32768	3.3	25	0	Static		Au	1695	88.6	91			0		#DIV/0!	#DIV/0!		8.84E+04	Part started having errors w/beam blocked
9	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	0	Au	1695	88.6	91	6.02E+04	9.99E+06	0	203	2.03E-05	3.10E-10	1.42E+04	1.03E+05	
10	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	1 ****	Au	1695	88.6	91	8.02E+04	9.97E+06	0	229	2.30E-05	3.50E-10	1.42E+04	1.17E+05	***** Data has all zero's but expects all 1's
11	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	0	Au	1695	88.6	91	8.61E+04	9.98E+06	0	182	1.82E-05	2.78E-10	1.42E+04	1.31E+05	
12	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	1	Au	1695	88.6	91	8.40E+04	9.97E+00	0	???	#VALUE!	#VALUE!	1.42E+04	1.45E+05	Errors after beam blocked
13	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	1	Au	1695	88.6	91	1.69E+05	9.96E+06	0	0	0.00E+00	0.00E+00	1.42E+04	1.59E+05	
14	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	1	Au	1695	88.6	91	1.97E+05	1.01E+07	0	753	7.46E-05	1.14E-09	1.43E+04	1.74E+05	
15	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	0	Au	1695	88.6	91	8.80E+04	1.00E+07	0	208	2.08E-05	3.17E-10	1.42E+04	1.88E+05	
16	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	0	Au	1695	88.6	91	1.28E+05	1.00E+07	0	199	1.99E-05	3.04E-10	1.42E+04	2.02E+05	
17	w5/mod6/B	BAE	65536	3.3	25	0	Static	0	Au	1695	116	67	9.33E+04	1.00E+07	40	0	0.00E+00	0.00E+00	1.86E+04	2.21E+05	
18	w5/mod6/B	BAE	65536	3.3	25	0	Static	1	Au	1695	116	67	2.25E+05	1.00E+07	40	2	2.00E-07	3.05E-12	1.88E+04	2.40E+05	
19	w5/mod6/B	BAE	65536	3.3	25	0	Static	CB	Au	1695	116	67	1.58E+05	1.00E+07	40	1	1.00E-07	1.53E-12	1.86E+04	2.58E+05	
20	w5/mod6/B	BAE	65536	0	25	0	Static	CB	Au	1695	116	67	1.08E+05	1.00E+07	40	0	0.00E+00	0.00E+00	1.85E+04	2.77E+05	
21	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	0	Au	1695	116	67	1.18E+05	1.01E+07	40	247	2.45E-05	3.73E-10	1.85E+04	2.96E+05	
22	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	1	Au	1695	116	67	2.38E+05	1.01E+07	40	1e4?	#VALUE!	#VALUE!	1.86E+05	3.14E+05	errors after beam blocked
23	11461	BAE	32768	3.3	25	0	Static	0	Au	1695	88.6	91	1.90E+05	9.92E+06	0	3	3.02E-07	9.23E-12	1.41E+04	1.41E+04	
24	11461	BAE	32768	3.3	25	0	Static	0	Au	1695	88.6	91	7.03E+04	1.00E+07	0	0	0.00E+00	0.00E+00	1.42E+04	2.83E+04	
25	11461	BAE	32768	3.3	25	0	Static	0	Au	1695	88.6	91	6.99E+04	9.98E+06	0	2	2.00E-07	6.12E-12	1.42E+04	4.25E+04	
26	11461	BAE	32768	3.3	25				Au	1695	88.6	91	6.77E+04	2.91E+06	0		0.00E+00	0.00E+00	4.13E+03	4.66E+04	Bad Run
27	11461	BAE	32768	3.3	25	0	Static	0	Au	1695	88.6	91	7.18E+04	1.00E+07	0	0	0.00E+00	0.00E+00	1.42E+04	6.08E+04	
28	11461	BAE	32768	3.3	25	0	Static	0	Au	1695	88.6	91	7.08E+04	9.99E+06	0	1	1.00E-07	3.05E-12	1.42E+04	7.50E+04	
29	11461	BAE	32768	3.3	25	0	Static	1	Au	1695	88.6	91	8.11E+04	9.97E+06	0	1	1.00E-07	3.06E-12	1.42E+04	8.92E+04	
30	11461	BAE	32768	3.3	25	625K	Dyn. Read	1	Au	1695	88.6	91	6.10E+04	1.00E+07	0	27	2.70E-06	8.24E-11	1.42E+04	1.03E+05	
31	11461	BAE	32768	3.3	25		Dyn. Read	1	Au	1695	88.6	91	6.33E+04	9.99E+06	0	0	0.00E+00	0.00E+00	1.42E+04	1.18E+05	
32	11461	BAE	32768	3.3	25	625K	Dyn. Write	1	Au	1695	88.6	91	6.51E+04	9.99E+06	0	7000	7.01E-04	2.14E-08	1.42E+04	1.32E+05	
33	11461	BAE	32768	3.3	25				Au	1695	88.6	91	6.78E+04	9.98E+06	0		0.00E+00	0.00E+00	1.42E+04	1.46E+05	Data File Missing
34	11461	BAE	32768	3.3	25	0	Static	1	Au	1695	116	67	6.61E+04	9.97E+06	40	0	0.00E+00	0.00E+00	1.86E+04	1.65E+05	
35	11461	BAE	32768	3.3	25	0	Static	1	Au	1695	116	67	6.90E+04	9.99E+06	40	0	0.00E+00	0.00E+00	1.86E+04	1.83E+05	
36	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	0	Xe	1176	54.9	92	7.47E+04	9.99E+06	0	144	1.44E-05	2.20E-10	8.78E+03	3.23E+05	
37	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	1	Xe	1176	54.9	92	6.97E+04	1.00E+07	0	18	1.80E-06	2.75E-11	8.80E+03	3.32E+05	
38	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	0 ****	Xe	1176	54.9	92	1.64E+05	1.00E+07	0	17	1.70E-06	2.59E-11	8.83E+03	3.40E+05	
39	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Read	1	Xe	1176	54.9	92	7.61E+04	1.00E+07	0	22	2.20E-06	3.36E-11	8.79E+03	3.49E+05	
40	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	0	Xe	1176	54.9	92	1.18E+05	1.00E+07	0	148	1.48E-05	2.26E-10	8.85E+03	3.58E+05	
41	w5/mod6/B	BAE	65536	3.3	25	625K	Dyn. Write	1	Xe	1176	54.9	92	1.69E+05	9.98E+06	0	27496	2.76E-03	4.20E-08	8.79E+03	3.67E+05	

Table 1: Bit Errors:

Exposure	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15	Bit 5+1 other	Bit 9+1 other	Raw Data run #
1																			
2																			
3																			
4																			
5																			
6																			
7																			
8																			
9	40	26	16	14	22	25	32	28		16								16	8
10	36	33	19	29	19	26	35	32		15								15	9
11	8	15	16	11	11	11	11	14		19								10	10
12						18202							34111						11
13																			
14						377							753						14
15	12	18	10	16	13	13	13	13		20								10	15
16	22	11	10	11	9	12	17	10		8								4	16
17																			
18							2			2			3						18
19							1						1						19
20																			
21	6	3	6	5	6	6	4	4		4								2	21
22						18880	2						18882						22
23			1	1			1												23
24																			24
25			2																25
26																			
27																			27
28								1											28
29			1																29
30	2	4	1	5	7	27	2										21		30
31																			
32	13	1	1			2282	3	1									5		32
33																			
34																			
35																			
36	17	15	16	15	23	19	21	17		15								15	37
37										16									38
38										14									39
39										19									40
40	3	4	3	4	6	3	4	10		12								6	41
41						13741							27496						42

Table 2: Summary of Bit Fails:

Bit Fails:	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15	Bit 5+1 other	Bit 9+1 other
Array B, Dyn Read 0 & R/W 0	144	125	96	105	109	115	137	128	0	109	0	0	0	0	0	0	0	78
Array B, Dyn Read 1 & R/W 1	0	0	0	0	0	51200	2	0	0	49	0	0	81242	0	0	0	0	0
Array D, Dyn Read 0 & R/W 0	None performed																	
Array D, Dyn Read 1 & R/W 1	15	5	2	5	7	2309	5	1	0	0	0	0	0	0	0	0	26	0
Without bits 5,9,12:	Without bits 5,9, & 12:																	
Array B, Dyn Read 0 & R/W 0	144	125	96	105	109		137	128	0		0	0		0	0	0		2
Array B, Dyn Read 1 & R/W 1	0	0	0	0	0		2	0	0		0	0		0	0	0		
Array D, Dyn Read 0 & R/W 0	None performed																	
Array D, Dyn Read 1 & R/W 1	15	5	2	5	7		5	1	0		0	0		0	0	0		6