FREQUENCY SYNTHESIS FOR TIMING CALIBRATION

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1. Introduction

A design and analysis technique for accurate timing of electronic pulses is presented. The design is based on a low-noise microwave phase lock loop technique at 800 MHz, phase locked to the 10 MHz from the GPS receiver. The generated 800 MHz sine wave has a jitter of less than 1 ps rms, and the derivative frequencies of 80 MHz, 100 MHz and 200 MHz have a jitter of less than 2 ps rms. The generated calibration start/stop impulses have a jitter of less than 3 ps rms, whereas start/stop events are phase locked to the fundamental frequency of 10 MHz, ie to the generated 800 MHz and its divided frequency components.

2. 800 MHz PLL/Calibrator System

The following block diagram shows the 10 MHz bandpass filter plus the quartz filter for the 10 MHz input stage, the 800 MHz PLL, the delay cable for the calibrator, the one-shots for generating the calibration impulses and some measurement, taken with a 50 GHz sampling scope.

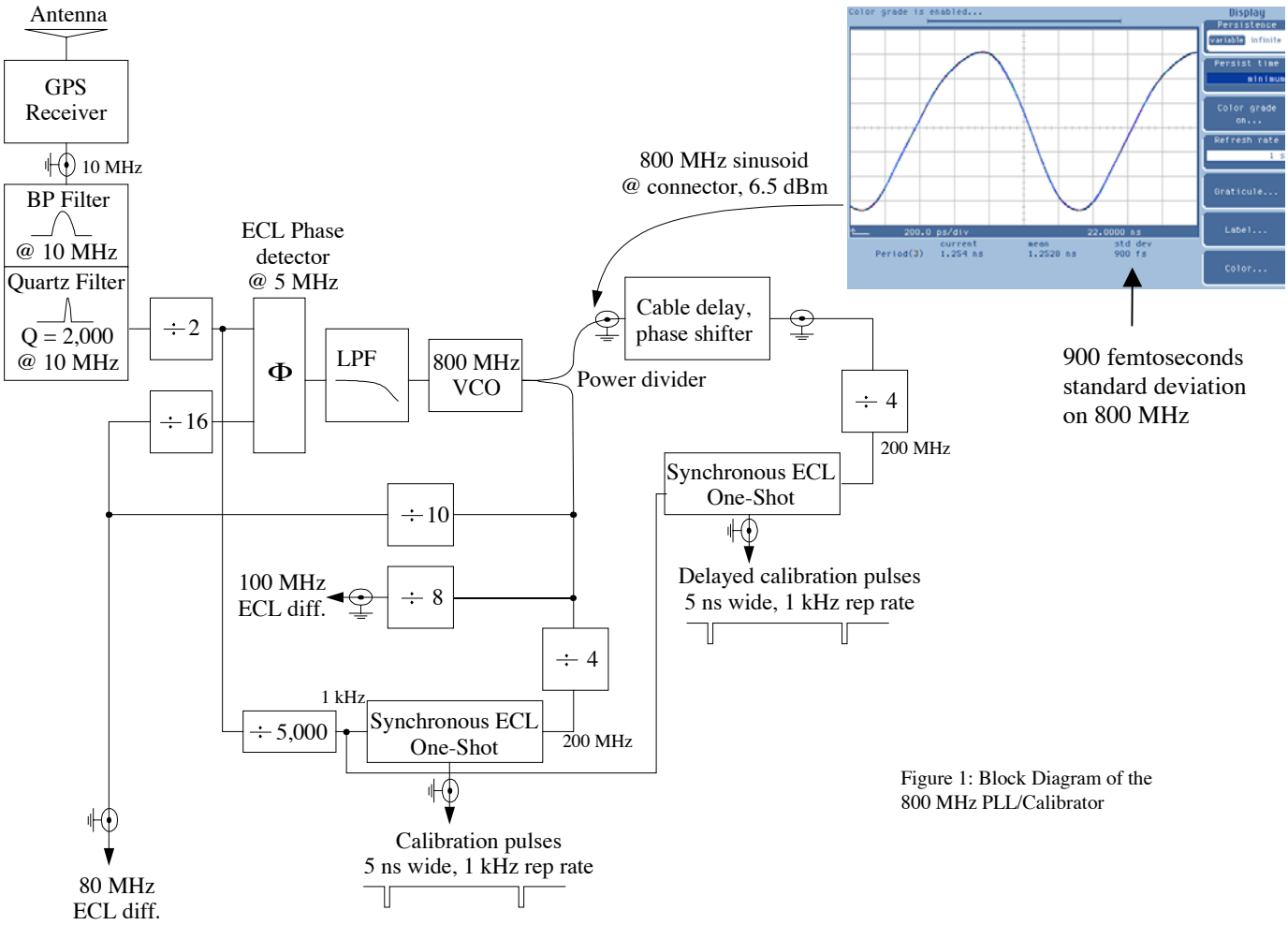

Figure 1: Block Diagram of the 800 MHz PLL/Calibrator

3. 10 MHz Filter

The frequency stability of the 10 MHz input is very good, but due to the slow risetime and falltime, the cycle-to-cycle jitter of 40 – 50 ps rms can be improved [8]. If processing the 10 MHz sine wave – like converting into ECL level – it is favourable to perform high quality filtering in order to reduce the noise bandwidth [6]. A two stage bandpass filter design is introduced. The first stage is a symmetric transformer coupled bandpass filter with $S_{11} = S_{22} = 50\ \Omega$ at 10 MHz centre frequency and $Q \cong 10$ at 10 MHz.

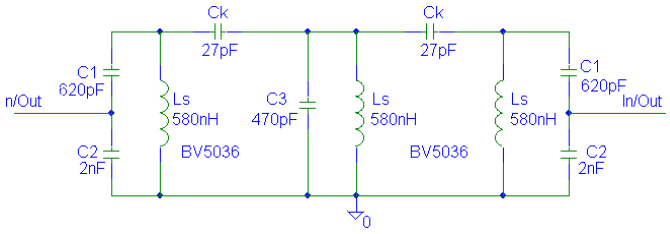

Figure 2: Schematics for a 10 MHz bandpass filter

Due to the capacitive voltage division of that specific filter architecture, it can reach a reasonable high Q of about 10 at 10 MHz by an insertion loss of 3 dB with a 50 Ω load. It can be easily shown that the source/load resistance of 50 Ω is transfered as parallel resistance R_p into the LC tank circuit as:

$$R_p := 50\ \Omega \cdot \left(\frac{C_1 + C_2}{C_1} \right)^2$$

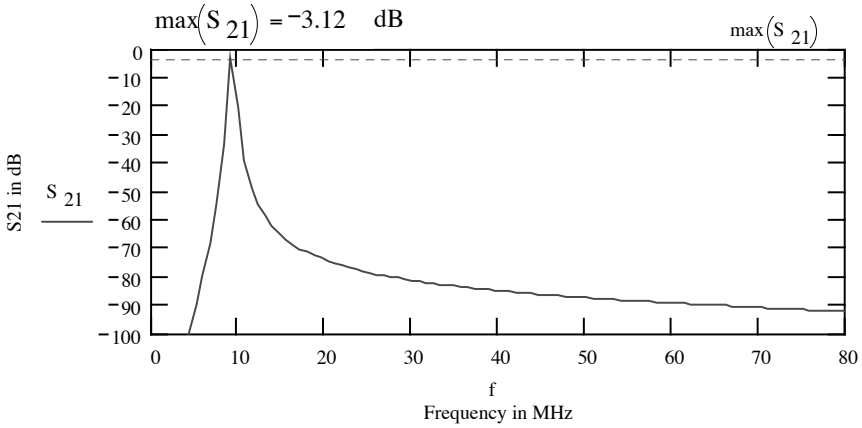

Figure 3: Filter transfer function S21 simulated with Puff, analyzed with MathCAD

A very cheap and powerful simulation tool for computer aided design for microwave integrated circuits is „PUFF“ [10]; it has been found as cost effective alternative for filter synthesis which matches the actual design behaviour very well.
By applying noise reduction techniques (like high-Q filtering), the system performance has improved even further [7]. A cascaded high-Q quartz filter with Q = 2,000 (!) at 10 MHz centre frequency at 50 Ω is reducing the noise bandwidth through its narrow transfer function further down to [6]:

$$\left(f_{U3dB} - f_{L3dB} \right) \cdot \frac{\pi}{2} = 7.854 \cdot kHz$$

The insertion loss is typically less than 3 dB. The German company KVG GmbH is manufacturing such quartz filters at 10 MHz centre frequency.

4. AC Coupling

There are several possibilities to convert a sine wave into ECL level, depending on the signal strength. If the input signal reaches 800 mV peak-to-peak, the following design uses an ECL buffer for ac coupling. That Motorola design works well up to 800 MHz, but only with a good RF coupling capacitor (e. g. from Dielectric Laboratories Inc.); beyond that frequency, the output amplitude is decreasing because of the system's 3-dB bandwidth of about 900 MHz

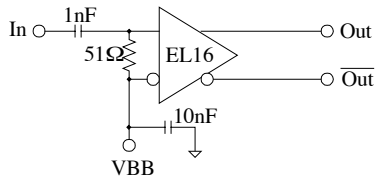

Figure 4: AC coupling architecture

If the signal in amplitude is to weak for ECL specifications, there are several high-speed small signal to ECL converters available on the market:

- Analog Devices, AD96687
- Maxim, MAX9687
- Motorola, MC10E1651
- Signal Processing Technologies, SPT9689
- NEL, NTT Electronics Technology Corporation, NLB6292

Especially the device from Signal Processing Technologies is very attractive because of its 900 MHz 3-dB-bandwidth and an output falltime of about 80 ps only.

5. Phase Locked Loop Design

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). Figure 5 is showing a PLL using a linearized model [1] with phase detector, loop filter voltage controlled oscillator, and feedback divider; whereas Figure 6 shows a more detailed design implementation of the same components.

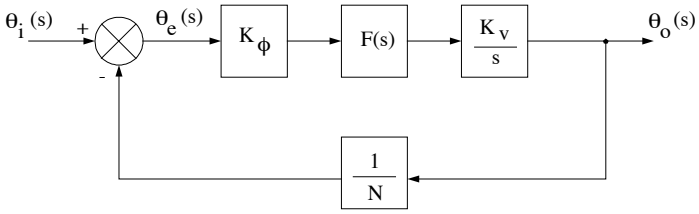

Figure 5: Phase locked loop feedback system

The parameters in Figure 5 are defined as:

$\theta_i(s)$ Phase input
$\theta_o(s)$ Output phase
$\theta_e(s)$ Phase error
G(s) Forward gain (product of the individual feed forward transfer function)
H(s) Feedback gain (product of the individual feedback transfer function)
K_ϕ Phase detector gain factor (V/rad)
K_v Voltage controlled oscillator gain factor (rad/Vs)

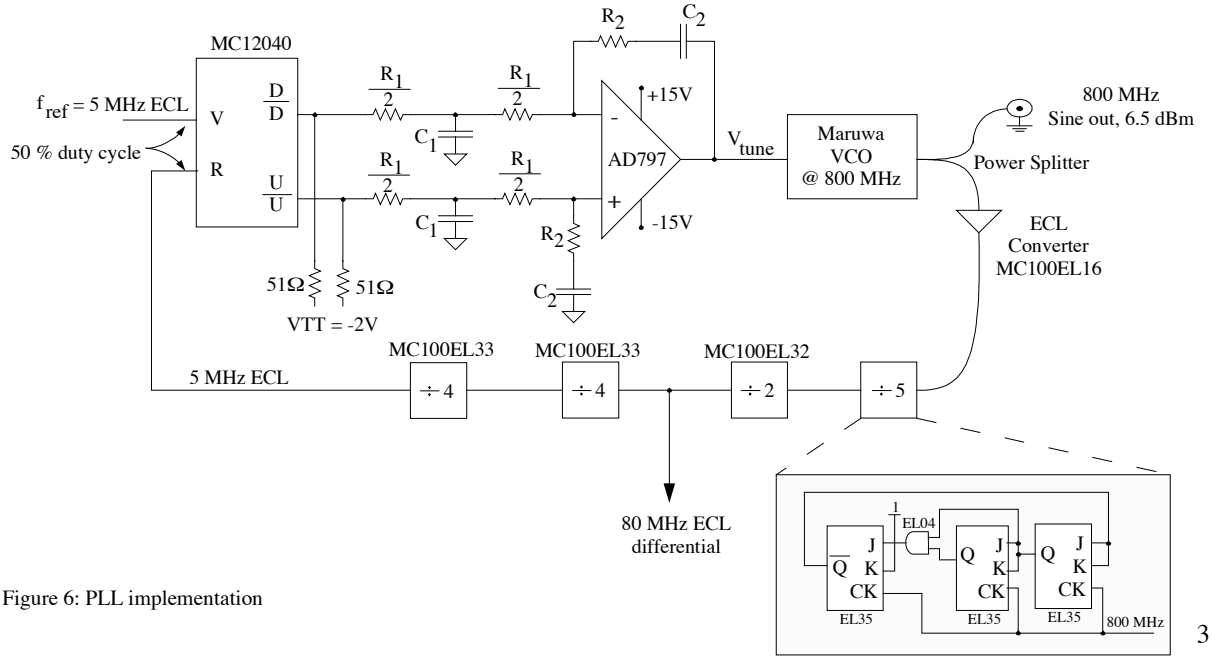

Figure 6: PLL implementation

The reference frequency which inputs to the phase detector is:

$$f_{ref} := \frac{10 \cdot MHz}{2} \qquad f_{ref} = 5 \cdot MHz$$

The required output frequency from the voltage controlled oscillator shall be: $f_{out} := 800 \cdot MHz$

That requirement drives the multiplication factor, ie the definition for the feedback transfer function:

$$N := \frac{f_{out}}{f_{ref}} \qquad N = 160$$

The feedback transfer function (feedback gain): $H(s) := \frac{1}{N}$

The phase detector gain from Motorola MC12040:

$$K_\phi := 0.16 \cdot \frac{volt}{rad}$$

The VCO gain factor (relation between tuning frequency and tuning voltage in radians) is taken from the Maruwa specifications:

$$K_v := \frac{(814.1 - 785.5) \cdot MHz}{(10 - 1) \cdot volt} \cdot 2 \cdot \pi$$

To analyze the performance of the design, the actual design parameters in figure 6 are taken:

$$R_1 := 9.4 \cdot k\Omega \qquad R_2 := 3 \cdot k\Omega$$

$$\frac{R_1}{2} = 4.7 \cdot k\Omega \qquad C_2 := 100 \cdot nF$$

Dividing the resistance R_1 together with C_1 shall improve the transient suppression from the reference frequency f_{ref} C_1 has no direct impact on the loop properties.
The active loop filter F(s) is in the form:

$$F(s) := \frac{R_2 \cdot C_2 \cdot s + 1}{R_1 \cdot C_2 \cdot s}$$

The forward gain G(s) of the loop:

$$G(s) := K_\phi \cdot \left(\frac{R_2 \cdot C_2 \cdot s + 1}{R_1 \cdot C_2 \cdot s} \right) \cdot \frac{K_v}{s}$$

Wheras the closed loop transfer function $\underline{F}_{cL}(j\omega)$ can be found by using the servo theory as:

$$\text{closed loop transfer function} = \frac{\text{forward\_gain}}{1 + \text{open\_loop\_gain}}$$

with $\sigma := 0$ and $s(\omega) := \sigma + j \cdot \omega$

we optain the closed loop transfer function:

$$F_{cL}(\omega) := \frac{G(j \cdot \omega)}{1 + G(j \cdot \omega) \cdot H(j \cdot \omega)}$$

The following plot shows the magnitude of the closed loop transfer function versus the angular frequency, showing the normalized angular frequency ω_n (see below).

$\omega := 2 \cdot \pi \cdot 1 \cdot Hz, 2 \cdot \pi \cdot 100 \cdot Hz .. 2 \cdot \pi \cdot 1 \cdot MHz$

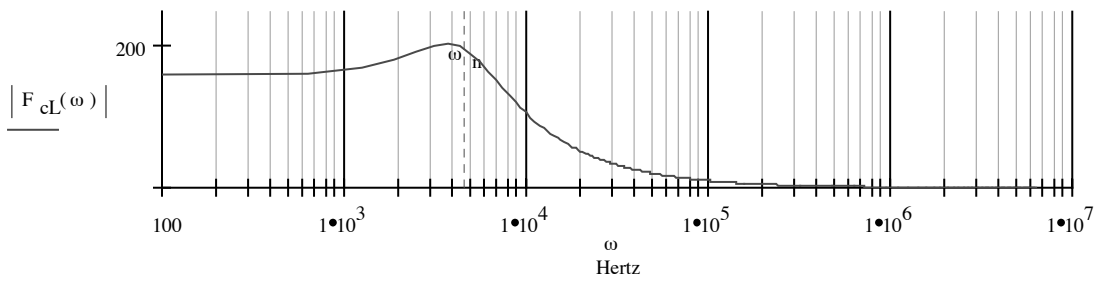

Figure 7: Closed loop transfer function of the PLL

The open loop transfer function $\underline{F}_{oL}(j\omega)$ and the phase function $\phi_{oL}(\omega)$ is needed for the stability analysis:

$$F_{oL}(\omega) := G(j\cdot\omega)\cdot H(j\cdot\omega) \qquad \phi_{oL}(\omega) := \arg\left(F_{oL}(\omega)\right)\cdot\frac{360}{2\cdot\pi}$$

The easiest way to analyze the loop stability is to plot the magnitude and phase of the open-loop transfer function versus frequency [2]. That specific Bode plot might seem to be instable for different feedback systems because the system has an open loop gain greater one for frequencies less than ω_c (see below).

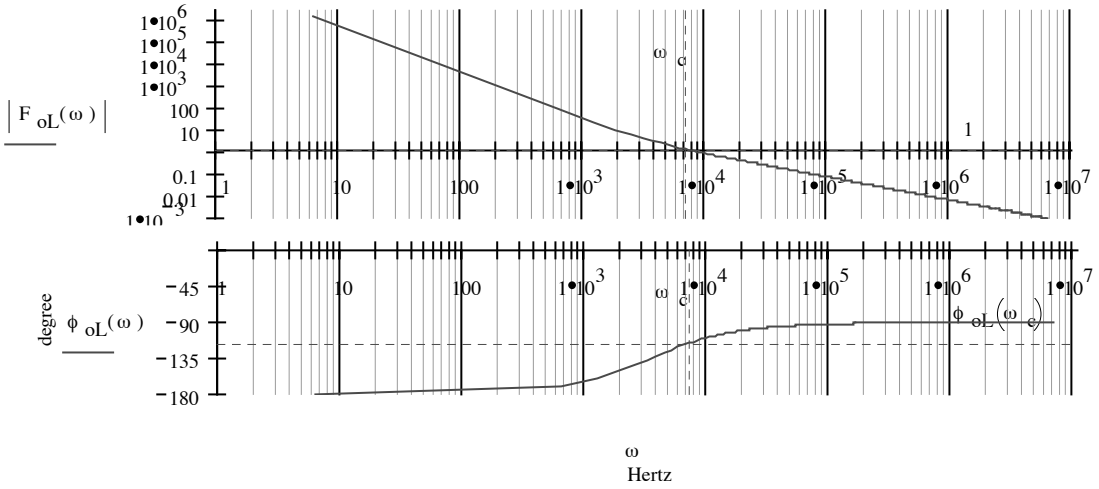

Figure 8: Open loop transfer function of the PLL and the phase diagram

The frequency ω_c is the frequency at which the open-loop gain is unity:

$\omega_c = 7\cdot kHz$

$\left|F_{oL}(\omega_c)\right| = 1$

That is, the phase margin is equal to 180 ^{o} plus the phase shift of the open-loop transfer function (a negative number) at the open-loop crossover frequency ωc. The greater the phase margin ϕ_M, the more stable the system and the more phase lag from parasitic effects can be tolerated.

$\phi_M := 180 + \phi_{oL}(\omega_c)$

$\phi_M = 65$ degree. That is a favourable value for sufficient stability margin.

Working out the phase error by applying a unit step input of the following form, requires the error transfer function from phase error $\theta_e(s)$ related to phase input $\theta_i(s)$:

$$C_p := 1\cdot rad \qquad \theta_i(s) := \frac{C_p}{s}$$

$$\theta_e(s) := \frac{1}{1 + G(s)\cdot H(s)}\cdot\theta_i(s)$$

Inserting the functions for G(s) and H(s) yields:

$$\theta_e(s) := \frac{1}{\left[1 + K_\phi\cdot\left(\frac{R_2\cdot C_2\cdot s + 1}{R_1\cdot C_2\cdot s}\right)\cdot\frac{K_v}{s}\cdot\frac{1}{N}\right]}\cdot\frac{C_p}{s}$$

The steady state error (t goes to infinity in the time domain, wheras s goes to zero in the s plane):

$$\lim_{s\to 0}\ \theta_e(s) = 0$$

Simplifying and re-arranging the equation for $\theta_e(s)$:

$$\theta_e(s) := \frac{s\cdot C_p}{s^2 + \frac{K_\phi\cdot K_v\cdot R_2}{R_1\cdot N}\cdot s + \frac{K_\phi\cdot K_v}{R_1\cdot C\cdot N}}$$

Normalizing yields:

$$\omega_n := \sqrt{\frac{K_\phi\cdot K_v}{R_1\cdot C_2\cdot N}} \qquad \xi := \frac{R_2\cdot C_2}{2}\cdot\sqrt{\frac{K_\phi\cdot K_v}{R_1\cdot C_2\cdot N}} \qquad \omega_n = 4.61\cdot kHz \qquad \xi = 0.69$$

With ω_n as normalized angular frequency and ξ as damping factor.

Using the defined normalized values for the phase error $\theta_e(s)$ yields:

$$\theta_e(s) := \frac{s \cdot C_p}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

Laplace's transform of the phase error $\theta_e(s)$ into the time domain:

$$\theta_e(t,\xi) := -C_p \cdot \xi \cdot \exp\left(-\xi \cdot \omega_n \cdot t\right) \cdot \frac{\sinh\left(\omega_n \cdot \sqrt{-1+\xi^2} \cdot t\right)}{\sqrt{-1+\xi^2}} + C_p \cdot \exp\left(-\xi \cdot \omega_n \cdot t\right) \cdot \cosh\left(\omega_n \cdot \sqrt{-1+\xi^2} \cdot t\right)$$

Overshoot as a function of the damping factor ξ is illustrated by various plots show clearly vanishing the steady state error for $\xi = 0.7$. That is the error remaining after all transients have died out.

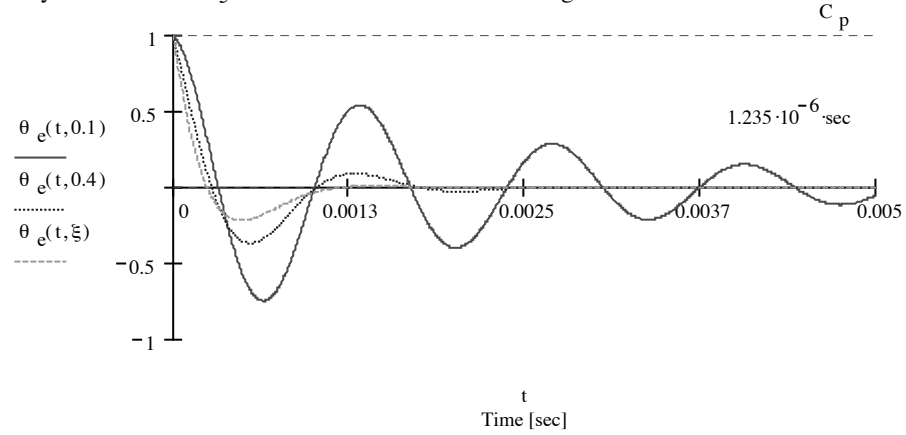

Figure 9: Phase error for different ξ for a unit input step

Analyzing the phase output $\theta_o(s)$ of the PLL system for a unit input step (detailed calculation is not shown here):

$$\theta_o(s) := \frac{G(s)}{1 + G(s) \cdot H(s)} \cdot \theta_i(s)$$

The obtained output response X(t) in the time domain (via inverse Laplace's transform):

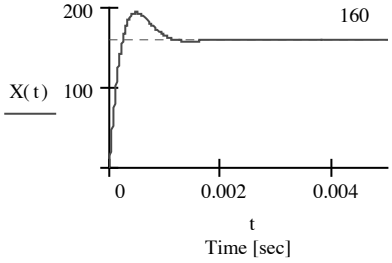

Figure 10: Phase output response for a unit input step

In synthesizer designs it is interesting to determine the system's noise bandwidth, B_n, which is defined as:

$$B_n = \frac{1}{2\pi} \cdot \int_0^{\infty} F_{cL}(j \cdot \omega)\, d\omega$$

The 3-dB bandwidth can be determined by solving the equation substituting $|B_n(j\omega| = 0.707$; the resulting $j\omega$ would then be the 3-dB bandwidth, the complex variable j deleted [1]. For the presented PLL B_n is:

$$B_n := \frac{\frac{K_\phi \cdot K_v}{N} \cdot \frac{R_2}{R_1} + \frac{1}{R_2 \cdot C_2}}{4} \qquad B_n = 2.426 \cdot \text{kHz} \qquad \frac{B_n}{\omega_n} = 0.526$$

The 3-dB bandwidth of the PLL is given by [1]:

$$\omega_{3dB} := \omega_n \cdot \sqrt{1 + 2 \cdot \xi^2 + \sqrt{2 + 4 \cdot \xi^2 + 4 \cdot \xi^4}} \qquad \omega_{3dB} = 9.39 \cdot \text{kHz}$$

The Phase noise calculation/interpolation follows, considering phase noise of the GPS receiver, voltage controlled oscillator and the phase detector MC12040. Units in the left culomns are the offset frequencies in Hertz, in the right culomns the values are single sideband phase noise in dBc/Hz.

$$VCO := \begin{bmatrix} 1 & -38 \\ 10 & -58 \\ 100 & -78 \\ 1000 & -98 \\ 10000 & -122 \\ 35000 & -134 \\ 100000 & -140 \\ 200000 & -143 \end{bmatrix} \qquad GPS := \begin{bmatrix} 1 & -90 \\ 10 & -120 \\ 100 & -135 \\ 1000 & -145 \\ 10000 & -165 \\ 35000 & -175 \\ 100000 & -184 \\ 200000 & -190 \end{bmatrix} \qquad PD := \begin{bmatrix} 1 & -100 \\ 10 & -110 \\ 100 & -120 \\ 1000 & -130 \\ 10000 & -140 \\ 35000 & -145 \\ 100000 & -149 \\ 200000 & -152 \end{bmatrix}$$

$VCO := csort(VCO, 0)$ $\quad GPS := csort(GPS, 0)$ $\quad PD := csort(PD, 0)$

$V := VCO^{<1>}$ $\quad R := GPS^{<1>}$ $\quad P := PD^{<1>}$

$X := VCO^{<0>}$ $\quad i := 0 .. length(X) - 1$

$vco(x) := linterp(X, V, x)$ $\quad gps(x) := linterp(X, R, x)$ $\quad pd(x) := linterp(X, P, x)$

Considering the phase noise of a single segment between offset frequencies f_a and f_b ($f_a < f_b$), we can work out the power law with a single valued exponent n (example with phase noise from GPS):

$$n = \frac{\frac{1}{10}\cdot\left(\frac{N_{op}}{C}\right)_a - \frac{1}{10}\cdot\left(\frac{N_{op}}{C}\right)_b}{\log\left(\frac{f_b}{f_a}\right)}$$

$$n := \frac{-18.4 - (-19)}{\log\left(\frac{200000}{100000}\right)} \qquad n = 1.99$$

GPS phase noise for 35 kHz offset frequency found with interpolation:

$$10\cdot\left[n\left(\log\left(\frac{100000}{35000}\right)\right) - 18.4\right] = -174.9 \quad \text{dBc/Hz}$$

That interpolation technique for single sideband phase noise density is very useful if only a few values for phase noise are known of a device.

Phase Noise Calculations:

$\underline{F}_{cL}(j\omega)$ is a low-pass transfer function and $\underline{F}_{oL}(j\omega)$ is a high-pass transfer function. The PLL functions as a low-pass filter for phase noise arising in the reference signal and phase detector, and it functions as a high-pass filter for phase noise originating in the VCO. Since the VCO noise is a low-frequency noise, the output noise due to the VCO noise is minimized by having the loop bandwidth as wide as possible. At the same time, the loop bandwidth should be less than the reference frequency in order to minimize the effect of the phase noise of the phase detector, which is dominated by spurious frequency components at the refernece frequency and its harmonics (that is the reason of the divide-by-2 of the 10 MHz reference frequency) [1,2].
The closed loop transfer function $\underline{F}_{cL}(j\omega)$ is a low-pass function (as in figure 7):

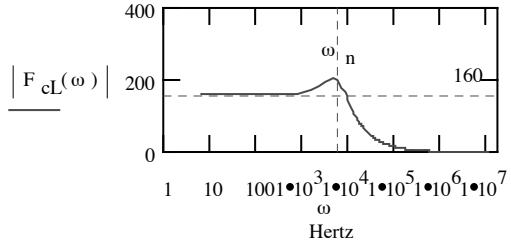

Figure 11: Closed loop transfer function as low-pass for reference phase noise and phase detector phase noise

Whereas the phase error transfer function $\underline{F_e}(j\omega)$ is a high pass function:

$$F_e(\omega) := \frac{1}{1 + G(j\cdot\omega)\cdot H(j\cdot\omega)}$$

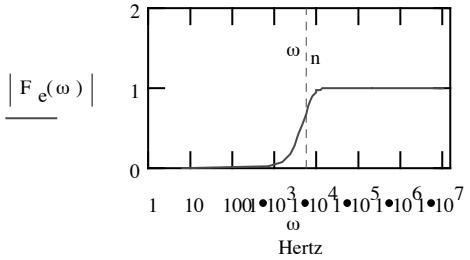

Figure 12: Error transfer function as high-pass for phase noise of the VCO

The effect of the low pass and high pass functions on the individual phase noise contributions is shown below [1,2], and the final result of single sideband phase noise of the 80 MHz is shown as a plot phan(X_i).

$$phn(i) := 10\cdot\log\left[\frac{\sqrt{\left(\left|F_e\left(2\cdot\pi\cdot X_i\cdot Hz\right)\right|\cdot 10^{\frac{V_i}{10}}\right)^2 + \left(\left|F_{cL}\left(2\cdot\pi\cdot X_i\cdot Hz\right)\right|\cdot 10^{\frac{P_i}{10}}\right)^2 + \left(\left|F_{cL}\left(2\cdot\pi\cdot X_i\cdot Hz\right)\right|\cdot 10^{\frac{R_i}{10}}\right)^2}}{10}\right]$$

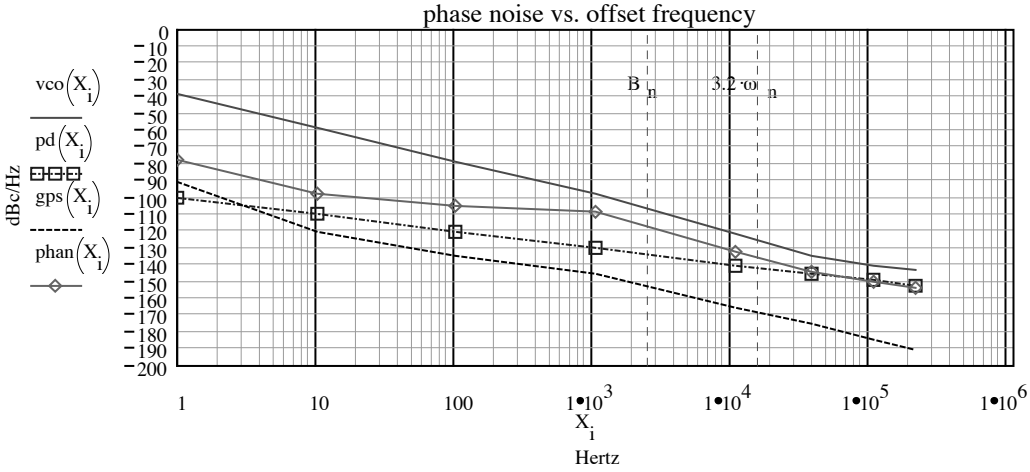

Figure 13: Resulting phase noise for 80 MHz

The frequency deviation δf related to one 80 MHz cycle can be calculated using the reciprocal relationships between phase noise and frequency stability [5] (frequency domain to time domain transformations and their inverses):

$$\delta f := \sqrt{\sum_i \left[\int_{1\cdot Hz}^{2.5\cdot\omega_n} 2\cdot\left[\frac{10^{\frac{phan(X_i)}{10}}}{Hz}\right]\cdot f_m^{\,2}\, df_m\right]} \qquad \delta f = 129\cdot Hz$$

The PLL design is using an extremely low noise output regulator circuitry for the VCO power supply. It is based on the fact that the current generating PNP transistor produces much less noise than its emitter follower equivalent [1].

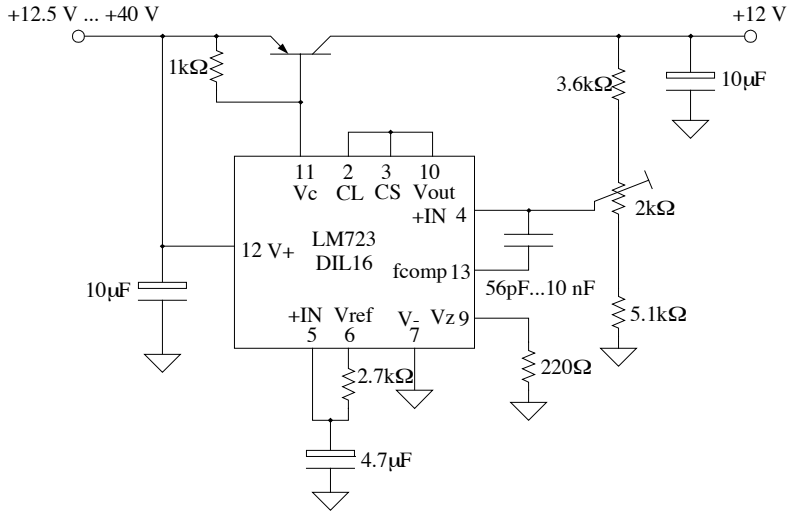

Figure 14: Ultra low-noise power supply circuit for the VCO

As a final result of several low-noise design methods, the 80 MHz NIM output signal is measured with a high bandwidth sampling oscilloscope. The rms jitter is 1.6 ps.

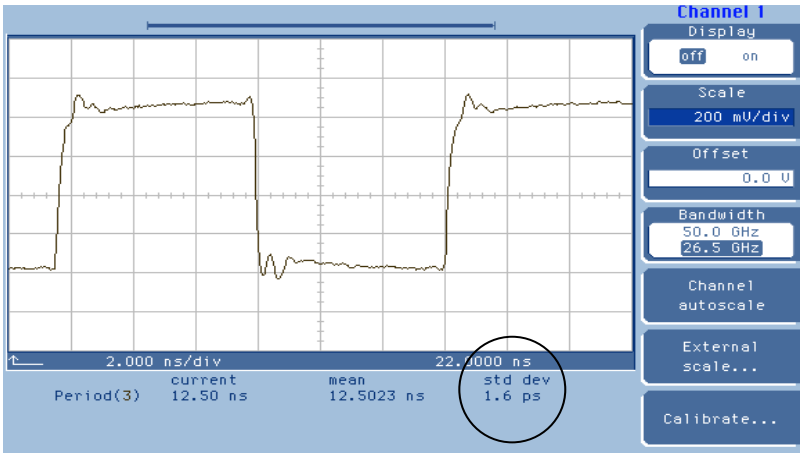

Figure 15: Time jitter of 1.6 ps rms of the 80 MHz NIM signal

6. Timing Calibrator Option

Instead of using the delay cable to produce low-jitter pulses, the 800 MHz source (< 1 ps rms) can be used to provide programmable calibration pulses (Figure 16). It is favourable to use Teflon with low ε_r as PCB material in order to minimize propagation delay and insertion loss. Such a synchronous design works reliable if the

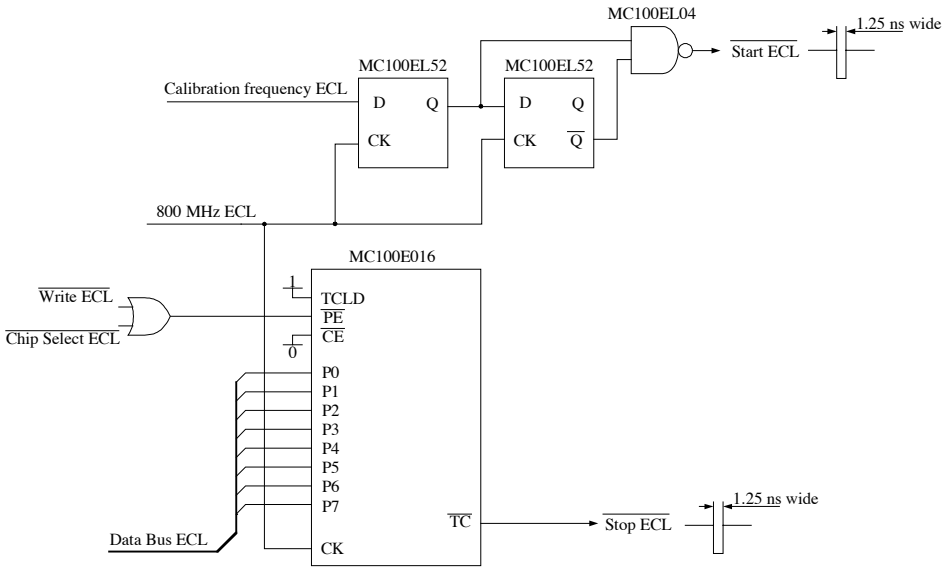

Figure 16: Hardware for programmable calibration start/stop pulses

propagation delay between data input D and data output Q (t_{QFF1}) plus the track delay on the PCB (t_{track}) and plus some combinatoric delay (not in fig. 15) plus the setup time of the next flip-flop (t_{SUFF2}) is less than 1.25 ns.

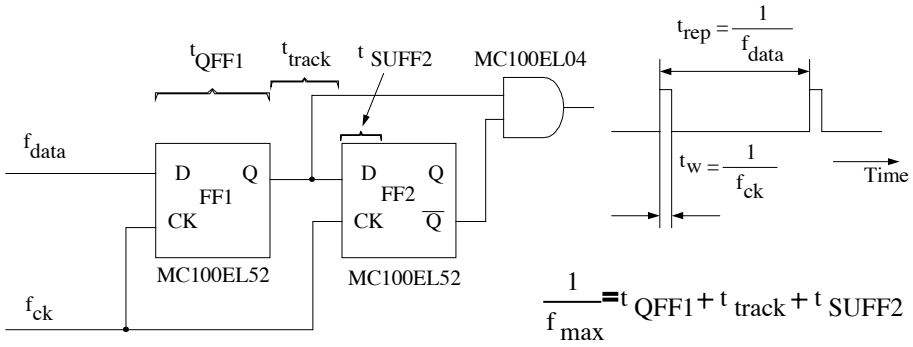

Figure 17: ECL one-shot, and its requirement for the maximum toggle frequency

ECL chips have exceptionally low jitter properties, especially dividing circuits. With that setup in Figure 14, a wide range of calibration time (256 times 1.25 ns) with less than 3 ps rms jitter, running at 800 MHz over the whole calibration range can be realized. The counter is set up for loading when Terminal Count (TC) goes high.

7. ECL to NIM Conversion

The NIM signal is a shiftet ECL signal. With the following design, an effective level conversion is shown. With the 50 Ω termination from the measurement equipment (oscilloscope, time interval counter), the differential amplifier is in balance. By paralleling two transistor pairs, the noise is reduced by √2. Additional stages would decrease the noise voltage proportinal to the square root of the number of stages [6]. The transistor array shall have a high transit frequency f_T and a low noise figure NF, like the HFA3046B from Harris Semiconductor.

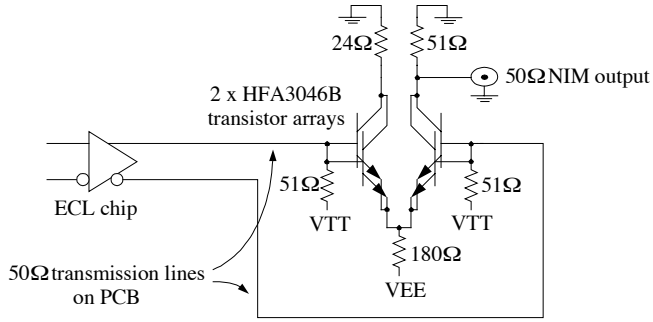

Figure 18: ECL to NIM converter

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