Fast Computation of Electrical Circuits: Speeding Up Charging Circuit Simulations

Researchers at Sandia National Laboratories have achieved a 600 times speed up over a traditional simulation for a highly oscillatory charging circuit. This advance represents a big step forward in simulating highly oscillatory circuits. These circuits typically have relatively slow behavior mapped on to very fast oscillations which consequently require huge computational integration times to solve. Applications include: communication circuits, charging circuits, trigger circuits and oscillators. These circuits represent critical sub-components of more sophisticated systems, are often quite small in size, and yet take very long to simulate. Until now, advanced analysis of these circuits, e.g. optimization and sensitivity calculations, have not been possible due to the huge overhead in simulation.

Sandia researchers have applied new research ideas in Multiple-Time Partial Differential Equations (MPDE) to achieve these results. The main idea behind MPDE algorithms is to introduce two artificial time variables. The first variable represents the highly oscillatory behavior of the circuit and the second represents the relatively slow behavior. This decouples the different rates of change in the problem and allows for considerable savings in integration. This new approach not only provides substantial speed-up but also allows for coarse design based simulations of these circuits, which were simply not possible before. This new algorithm is being implemented in **Xyce**, Sandia's large scale parallel circuit simulator, and will soon be available to designers.

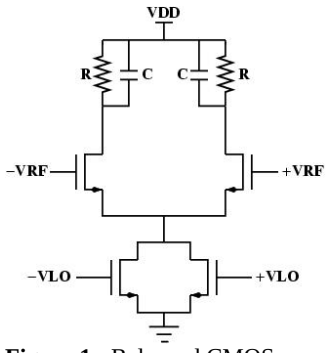

Figure 1: Balanced CMOS down-conversion mixer that was simulated for this speed-up comparison. The lower pair of MOSFETs generates a current that doubles the LO frequency and the upper pair forms a differential pair. The circuit implements multiplications of the RF and LO signals. The LO signal is a 450Mhz sinusoid modulated by a 2.5kHz sinusoid. The RF signal is a 900MHz carrier modulated by a bit-stream at 10kbps.

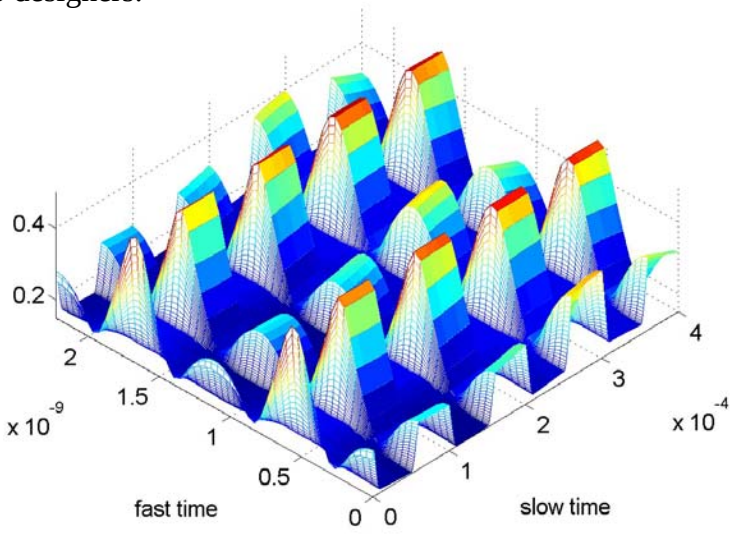

Figure 2: MPDE solution for the voltage at the drains of the upper MOSFETs.

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