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Radiation Effects in CDF Switching Power Supplies

R.J. Tesarek, C. Rivetta
Fermilab, Batavia, IL 60510

R. Napora
Johns Hopkins University, Baltimore, MD 21218-2695

C. Rott
Purdue University, West Lafayette, IN 47907-1396

Abstract

Recent switching power supply failures in the CDF collision hall have been attributed to single event burn out (SEB) in power metal oxide semiconductor field effect transistors (MOSFET). We measure the SEB cross sections for the power MOSFETs used in the switching circuits of the CDF VME low voltage power supplies and two candidate replacement components. Similar measurements are made for a MOSFET used in the bias power supplies of the CDF silicon detector and its candidate replacement. We find all candidate replacement components sufficiently radiation tolerant to eliminate SEB as a failure mode over the lifetime of CDF.

1 Introduction

CDF uses a variety of power switching power supplies to provide both low and high voltages for various systems. The trigger and readout systems use 9U VME crates with low voltages provided, for the most part, by 2.5 kWatt, switching power supplies [1]. These modular power supplies were specially manufactured by ASTEK for use in CDF. The high voltage bias power supplies for the silicon detectors were also manufactured according to CDF specifications by Costruzioni Apparecchiature Elettroniche Neucleari S.p.A. (CAEN). In order to minimize electronic noise and to keep the power dissipation in cables to a minimum, many of these power supplies are located in the CDF collision hall.

After initial burn in, those VME power supplies located in the CDF collision hall were observed to fail at a rate of approximately one per week [1]. The nature of these failures became particularly evident on November 25th (Saint Catherine's day) when 12 VME power supplies failed in a single day. Analysis of these failures found that a single component failed in all cases. For the VME supplies, the component which failed was a 500 V, n-channel, power metal oxide silicon field effect transistor(MOSFET). This device is the switching transistor of the AC/DC power factor corrector module for the power supply. It switches 385 volts at 100 kHz. Figure 1 is a photograph of a failed component from one of the VME power supplies.

In addition to the 12 VME power supply failures on November 25th, 10 silicon high voltage bias supplies failed. These supplies, also located in the CDF collision hall, were being tested at the time near their maximum operating voltage and were not connected to detectors. Again the component that failed was a 1000 V n-channel power MOSFET (International Rectifier part IRFBG20).

The pattern of failures indicated radiation as the likely culprit. Thermal luminescent dosimeters were placed near all the power supplies that were failing and subsequently harvested after a single VME power supply failed. Data from these dosimeters indicated radiation doses no larger than 100 mRad of ionizing radiation or 1.5 Rad of low energy neutrons ($E_n < 200$ keV). This result ruled out possible effects due to total radiation exposure which are not expected to cause significant problems until exposures of several kRad.

The characteristics of the component failures are consistent with a mechanism known in the literature as single event burnout (SEB). The SEB mechanism can be thought of as the biased transistor behaving as a slightly more complicated version of an ionization chamber. An ionizing particle passing through the transistor creates a narrow (diameter $\approx 1\mu$m) sheath of electron-hole pairs in bulk of the transistor. When the drain-source bias (V_{ds}) is large enough, the electrons and holes drift in the applied electric field. The resulting current density can be in excess of 10^4 A/cm^2. The vertical current deflects to flow laterally in the insulator-silicon interface to the body region. This flow induces a voltage drop between the P-body and the source regions (V_{bs}). The source, P-body and N-Epi regions form an effective N-P-N bipolar transistor. When V_{bs} exceeds 0.7 V the bipolar transistor is forward biased. Under the forward bias, a positive feedback is established and the local current density surrounding the track is increased by several orders of magnitude. Heating from the high local power density

[1] Linear supplies are used for the readout of the cherenkov luminosity monitor and calorimeters.

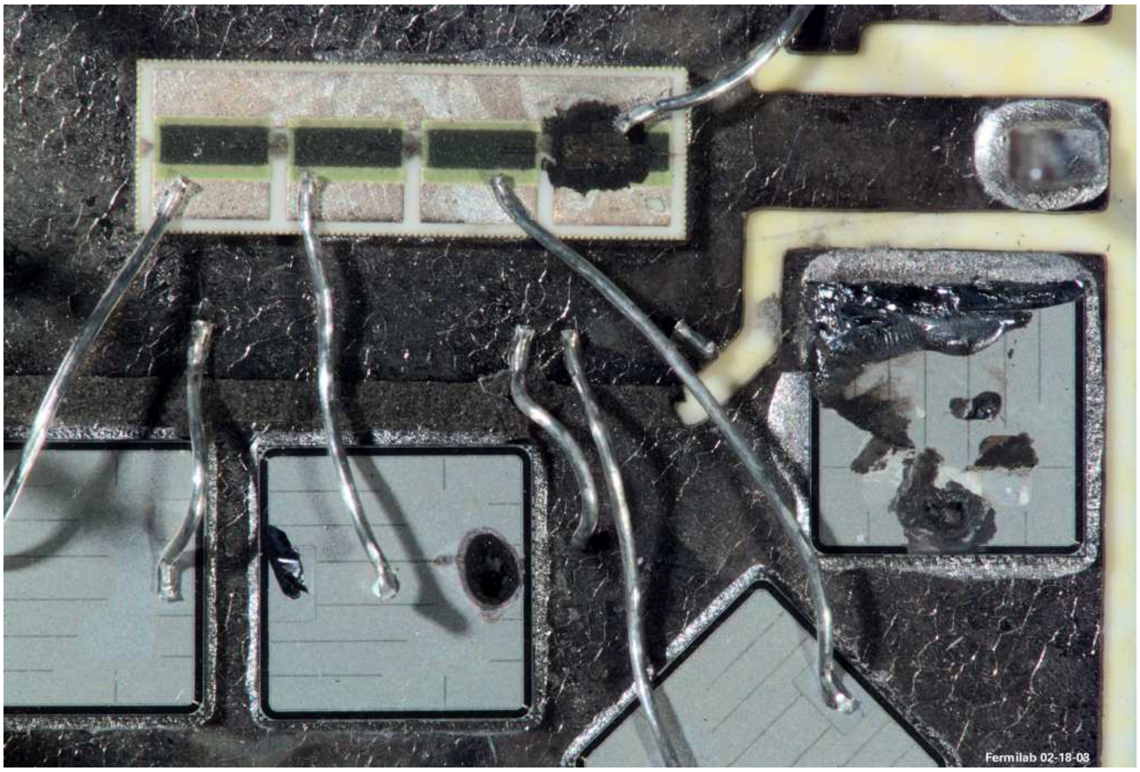

Figure 1: Failed power MOSFETs in a hybrid circuit as part of the CDF VME power supplies. Note the loss of wire bonds and fracture of the silicon indicating a catastrophic failure.

may be sufficient to sublimate the silicon, resulting in catastrophic failure. Figure 2 shows a schematic of this process. In the above mechanism, the failure is related to the local ionization from the radiation, the bias voltage applied to the transistor and the stored energy in the transistor circuit. There are N-channel MOSFETs in the market which are designed to be SEB robust. Another technique for minimizing this type of effect in a given radiation environment is to operate the transistor far from its maximum operating voltage (de-rating the transistor). A comprehensive overview of this subject may be found in Titus and Wheatley's 1996 article [2].

For the VME readout power supplies, these failures effectively shut the power supply off. However, in the silicon high voltage bias supplies, the failing MOSFETs regulate the bias voltages put across the detector. When they experience a SEB the full voltage of the supply is put across the detector and the channel cannot be turned off short of dropping the AC power to the power supply crate supporting the individual supply. For the innermost detector (L00) supplies, $V_{ds} \simeq 530$ V . For the other silicon (SVX, ISL) bias voltage supplies $V_{ds} \simeq 270$ V. If this failure were to occur in a power supply cabled to the detector it could result in permanent damage

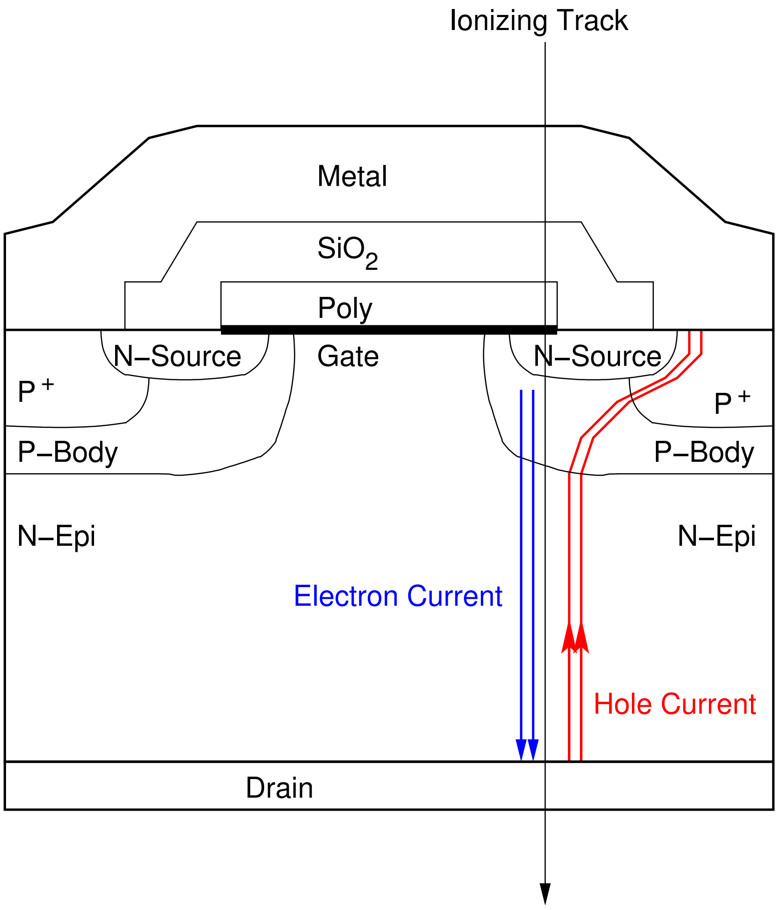

Figure 2: Schematic diagram of the mechanism for single event burnout (SEB).

to the corresponding silicon sensors.

To date, these failures in the silicon HV supplies have only been observed in the L00 supplies (which have a higher V_{ds} than those for SVX and ISL) and only prior to their being cabled to the detector. Since this failure was first observed the MOSFETs in all L00 supplies have been replaced with bipolar junction transistors (BJTs, part number: BUH2M20AP) which are believed to be more radiation tolerant. A crowbar circuit has also been designed and implemented for the L00 power supplies to prevent damage to the detector if this failure were to re-occur [5]. At present the SVX and ISL power supplies have not been modified.

An additional concern was the use of a silicon controlled rectifier (SCR) in the crowbar circuit (part number: TCR22-8). It was theorized that the SCR would be susceptible to a single event latch up (SEL) when irradiated. While SEL would not cause any serious damage, it would result in a blown fuse preventing a silicon ladder from being biased until the fuse could be replaced. If this failure happens with sufficient frequency it would cause operational difficulties.

An SCR is a NPNP junction with the gate attached to the second P layer. The

SCR can be most easily visualized as two transistors, one PNP and the other NPN, which are joined together. Under normal operation, the gate first receives a current activating the first transistor (PNP) which, in turn, activates the second (NPN) transistor. This second transistor then provides the current to keep the first transistor activated so that a current no longer needs to be applied through the gate for the SCR to remain conducting.

Single event latch up occurs in an SCR when an ionizing particle passes through the reverse biased portion of the SCR. The ionizing particle creates a series of electron-hole pairs which act as charge carriers producing a small current. If this current is comparable or greater than the latching current, the SCR would turn on and then stay on until the current is externally removed.

2 Irradiation Tests

We evaluated the SEB hypothesis by mounting transistors of the same type as those found in the VME power supplies (Q_1) on a test board along with another power MOSFET with a well measured SEB cross section (Q_2). The test boards limited the maximum current switched by the transistor so as not to cause a catastrophic failure. However, by monitoring the drain-source current in the transistor, one may count the failures. One may then calculate a SEB cross section for Q_1 by taking the ratio of SEB events N_Q, for both transistors and multiplying by the Q_2 cross section:

$$\sigma_{SEB,Q_1} = \sigma_{SEB,Q_2} \left(\frac{N_{Q_1}}{N_{Q_2}} \right). \tag{1}$$

These boards were installed in the CDF collision hall on top of the low beta quadrupoles, east of the CDF detector. Figure 3 shows the setup used in the CDF collision hall. Figure 4 shows an oscilloscope trace of a SEB failure signal.

Two different bias voltages (V_{ds}) were applied in two different study periods lasting a total of seven weeks. For the first period the transistors were biased at $V_{ds} = 400$ V. For the second period the transistors were biased at $V_{ds} = 450$ V. During these two periods, a total of 104 SEB events were observed for the MOSFETs from the CDF power supplies and 10 SEB events from the transistors measured previously. Based on the observed SEB failures one can estimate the number of power supply failures during a similar period of time. For this estimate only the failures for the transistors operating with a bias of 400 V were used. We also assume that the radiation comes from the beamline which forms a line source ($1/r$ scaling). Under these assumptions, one would expect 2.5 VME power supply failures in the period between 10 January and 3 March and 5 were observed.

Candidate replacement insulated gate bipolar transistors (IGBT) were also installed during the later period. The candidate replacement device was chosen to have a maximum operating voltage of 1000 V. The maximum operating voltage of the MOSFETs operating in the VME supplies is 500 V. A single SEB event was observed

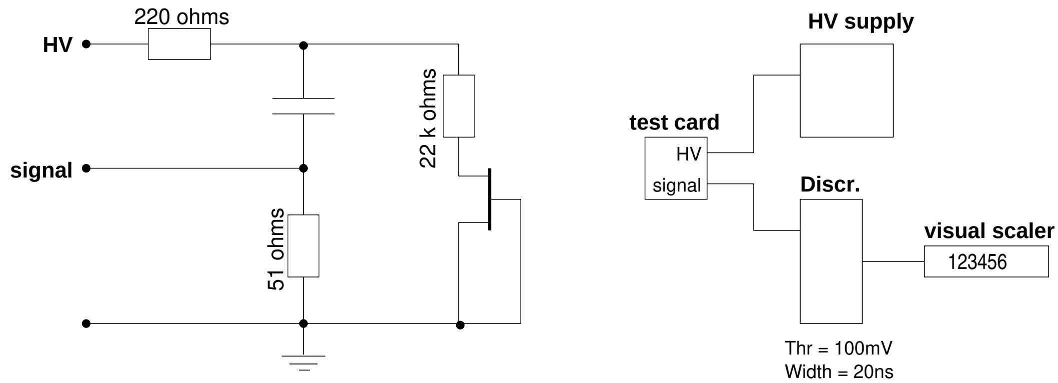

Figure 3: Transistor test setup installed in the CDF collision hall and Fermilab booster radiation damage facility.

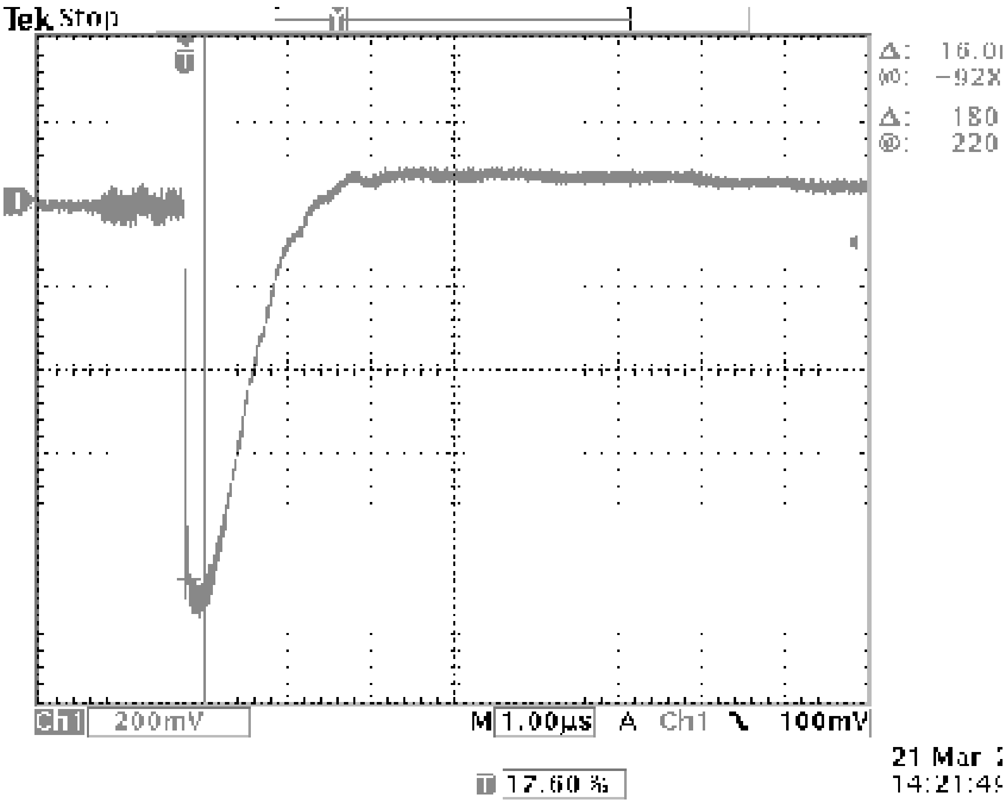

Figure 4: Oscilloscope trace of a typical SEB failure event.

Table 1: Summary of SEB studies performed in the CDF collision hall. The three transistors correspond to Q1: ASTEK power MOSFET, Q2: candidate insulated gate bipolar transistor replacement, Q3: Vicor power MOSFET measured previously [4].

Irradiation			V_{ds}	SEB events			σ_{SEB} (cm^2)	
Start	End	Location	(Volts)	Q1	Q2	Q3	Q1	Q2
01/10	01/30	CDF	400	15	1	–	$< 3 \times 10^{-8}$	–
02/02	03/05	CDF	450	89	9	1	$\approx 6 \times 10^{-7}$	$< 7 \times 10^{-9}$
02/21	02/28	Booster	400	164	56	0	6.4×10^{-8}	$< 1 \times 10^{-10}$

on the candidate replacements during an access to the CDF collision hall. Previous experience had shown a sensitivity to work in the collision hall near our test setup. If this event is counted as spurious, we estimate that the IGBT has a sensitivity to SEB less than 0.011 times that of the MOSFETs used currently.

Due to the low rates in the CDF collision hall, tests were also performed in the Fermilab booster Radiation Damage Facility (RDF) located near the booster abort line. For our tests, no beam was run to RDF. Because of the proximity of the booster abort line, the RDF area sees much higher radiation levels. The average SEB event rate was considerably higher for the transistors measured and the previous result was confirmed. Tests of candidate replacement transistors with V_{ds} of 450 V found no SEB events so upper limits were established on the SEB cross section of 1×10^{-10} cm^2 ($V_{ds} = 400$ V) and 6×10^{-9} cm^2 ($V_{ds} = 450$ V). Table 1 summarizes the results of the collision hall and booster studies.

Measurements of the SEB cross sections for the failing VME power MOSFETs and two candidate replacements, the IGBT discussed above and a 1000 V n-channel MOSFET, were subsequently made at the Indiana University cyclotron Radiation Effects Research Facility (IUC-RERF). The cyclotron is capable of providing proton beams in the range 20–200 MeV with a beam flux ranging between 10^6–10^{10} p/cm^2/s spread nearly uniformly over a 6 cm diameter circle. Details of the facility are more fully described elsewhere [3].

The setup for these tests was similar to that used in the CDF and booster evaluations. Four transistors were mounted to boards using the circuit shown in Figure 5 and supplied with a common bias voltage. The drain-source current from each transistor was then monitored with a discriminator scaler arrangement similar to that used in the CDF and booster tests. The transistors were centered in the beam and test pulses were sent to confirm signal continuity for one transistor. Each transistor was then irradiated using a 200 MeV proton beam with an average flux of 3–4$\times 10^8$ p/cm^2/s. The bias voltage was kept constant during the course of each irradiation which ranged from 0.5–2.0 $\times$ 10^{11} p/cm^2. In order to avoid total dose effects, we limited the total fluence delivered to 2.0×10^{11} p/cm^2 for any set of transistors. The SEB cross sections

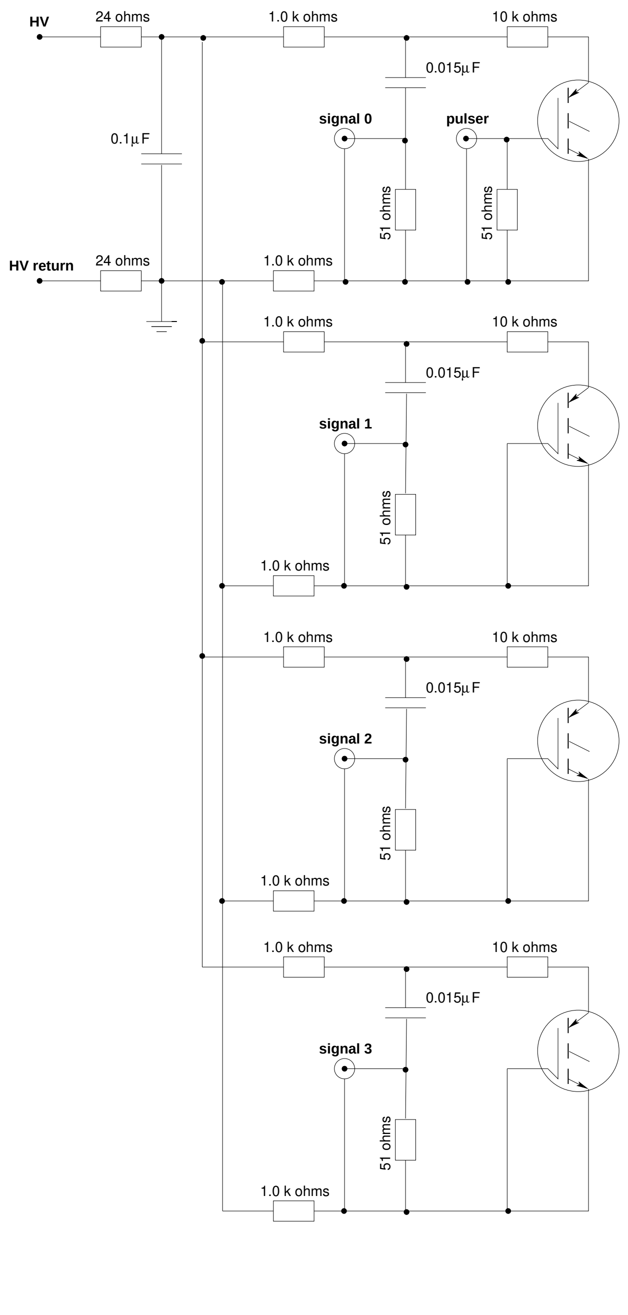

Figure 5: Schematic drawing of the circuit used for transistor irradiation tests at the Indiana University cyclotron. For the SCR tests the same circuit board was used with the following modifications: the 10k resistors on the source side of the SCRs were replaced with a jumper wire, the 1k resistors on the HV supply side of the circuit were replaced with a 1M ohm resistor and the 51 ohm resistor in parallel with the pulser output was replaced with a jumper wire.

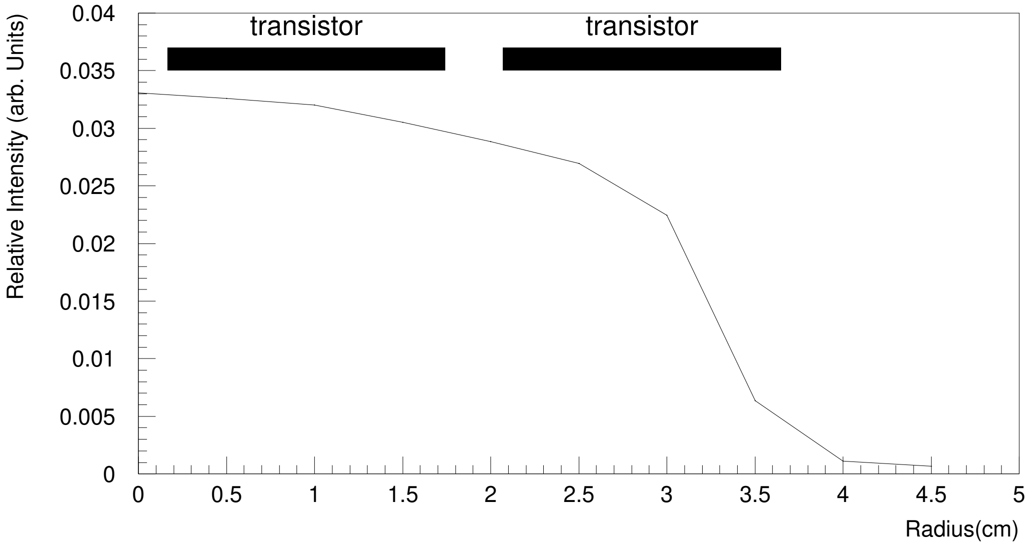

Figure 6: Proton beam intensity as a function of distance from the beam axis. Locations of transistors in the irradiations are superimposed.

were then calculated dividing the average number of counts by the delivered fluence. Uncertainties in the cross sections were estimated using the spread in the number of SEB events for a given irradiation.

The non-uniformity in the beam introduces a systematic bias in the mean cross section. The beam intensity profile is shown in Figure 6 with transistor locations superimposed. Integrating the beam profile over the area of the transistors and again averaging the results shows that the cross sections need to be corrected up by a factor of 1.30.

Spurious counts were observed due to electromagnetic interference from a solenoid controlled beam stop upstream of the irradiation area. These counts all came at the end of a run when the beam stop was inserted into the beam line. Measurements of this effect were made with the beam off and the number of counts seen had a mean of 3, a mode of 0, and a maximum value of 55, i.e. this effect was generally small (or zero) but could have large spikes. This noise could be identified in measurements where the count rate was low by recording the values shortly before the beam stop went in. In high rate measurements this noise could not be distinguished from the signal. Any data with obviously spurious counts was removed. Figure 7 shows the corrected SEB cross sections. The measurements made in the CDF collision hall are in good agreement with those in the booster.

The MOSFET used in the silicon HV supplies and their replacement BJT were

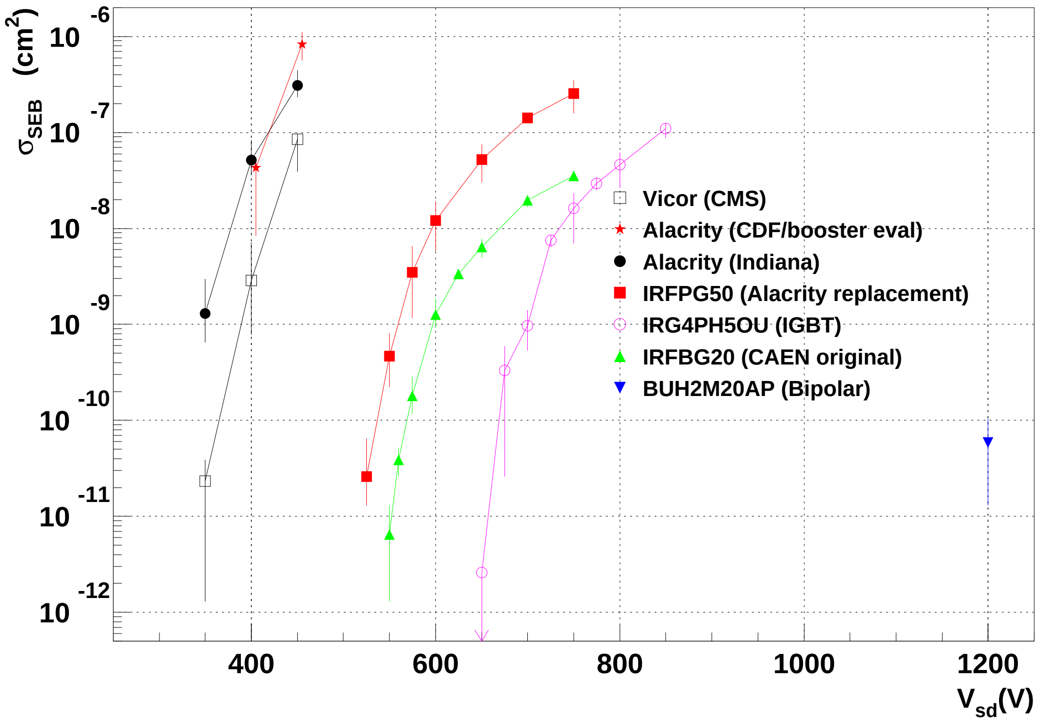

Figure 7: Measured SEB cross sections vs drain-source bias voltage (V_{ds}) for the transistors tested. The uncertainties indicate the spread in the data. The shaded region indicates the the upper limit on the sensitivity of our measurements.

also evaluated using the same test circuit described earlier. Measurements were made on the BJTs with applied collector-emitter voltages of 800, 1000, 1100, 1150 and 1200V at fluences varying between (0.5-2.0)$\times 10^{11}$ p/cm^2. The only events seen on the BJTs were at 1200V where the average cross section was 2.25×10^{-11} cm^2.

However, BJTs are known to suffer a loss in gain when irradiated. This gain loss can occur both through displacement damage and ionization damage. *Displacement damage* occurs when a neutron or energetic charged particle interacts with a silicon atom and disrupts its position within the lattice resulting in a vacancy at a given lattice site or the atom located in the region between lattice sites (interstitials). Interstitials create energy levels within the previously forbidden band gap. In the base they serve as additional recombination centers resulting in a higher recombination current within the base and a subsequently lower pass-through current to the collector (gain loss). *Ionization damage* results from a charged particle creating an electon-hole pair. When one or both of these charges becomes trapped in the insulating SiO_2 layer the local change in the electric field can result in gain loss through two

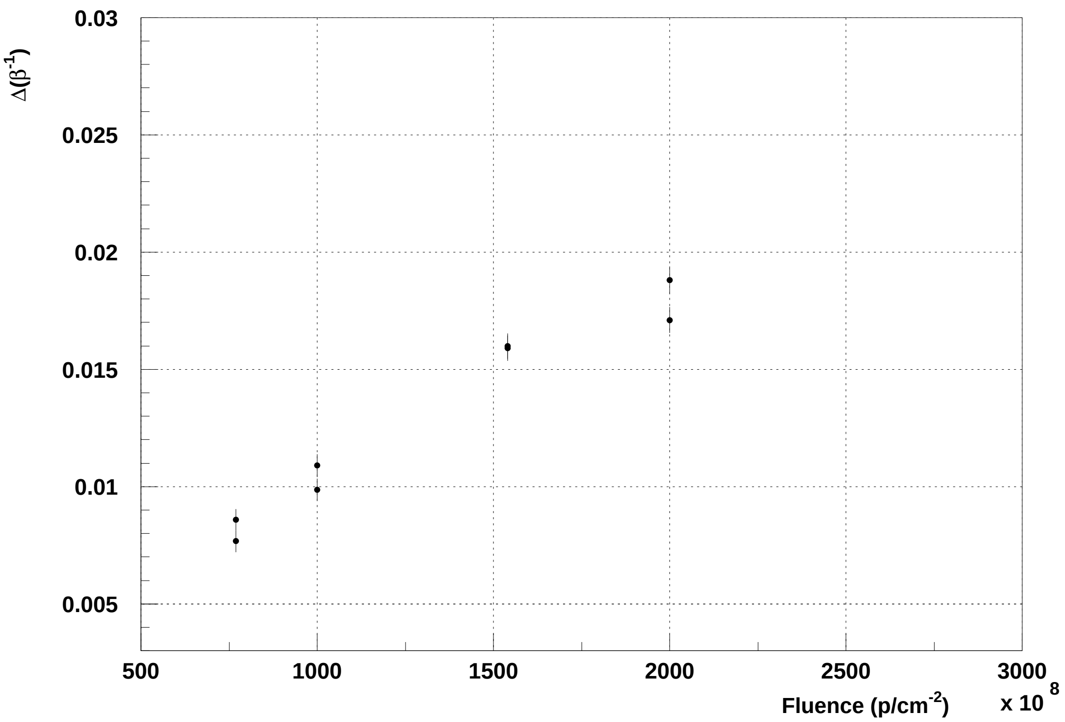

Figure 8: Change in the inverse gain ($\Delta(\beta^{-1})$) vs fluence for the bipolar junction transistors exposed at IUCF. The error bars are for the individual gain measurements whereas the distribution of the points is representative of the differences between individual transistors

main mechanisms. The first is when a channel is extended from the emitter region into the base region at the SiO_2 surface which results in an increased surface current. The second is when the oxide charge makes the depletion layer between the base and emitter region widen thereby increasing the recombination current. An increase in either of these currents results in a decrease of the collector current, or a loss in gain.

The gains (β) of eight of the BJTs were measured prior to their irradiation in Indiana. They were then re-measured after a cool-down period of several weeks. For these measurements the collector-emitter voltage (V_{ce}) was 6V and the base current (I_{base}) was 1 mA. Results can be summarized in Figure 8.

The test circuit for the SCRs had to be modified slightly from that used for the transistors to insure that the SCR did not remain active after a latch up event was recorded. A first test at the cyclotron was done at 550V using this test board. The board received a total fluence of 2×10^{11} p/cm^2 with no SEL events counted. Fearing that the test board was at fault, a simpler circuit shown in Figure 9 was

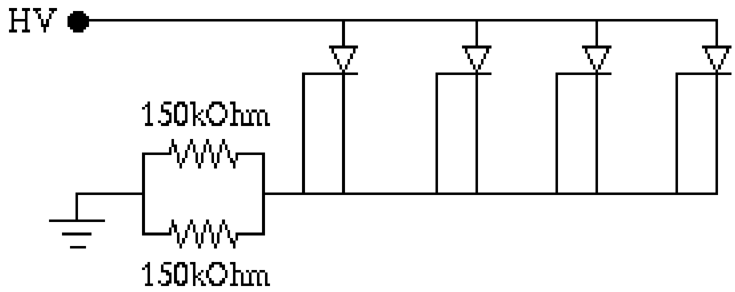

Figure 9: Modified SCR test circuit.

Table 2: Leakage currents for the modified SCR boards

Applied Voltage (V)	Fluence (p/cm^2)	Current(nA) pre-run	post-run
500	$(5.030 \pm 0.014) \times 10^{10}$	–	–
600	$(4.970 \pm 0.014) \times 10^{11}$	710	750
600	$(1.000 \pm 0.003) \times 10^{11}$	750	770

used for the next measurement. If an SCR in the second circuit were to suffer SEL the resulting current draw would have tripped the HV power supply. This board received a total fluence of 2×10^{11} p/cm^2 over a course of three runs with voltages up to 600V (the maximum rated voltage of the SCR). No latch up events where seen with the modified test board, although the leakage current in the SCR was observed to increase from approximately 700 nA to 1100 nA when the beam was running. A small amount of radiation damage was observed as an overall increase in the leakage current comparing before/after the irradiation. Table 2 summarizes the SCR leakage current observations.

3 Discussion and Conclusions

For the VME power supplies, we find that the IGBT and alternate candidate replacement MOSFET transistors have SEB cross sections which are smaller than our cross section sensitivity when operated at $V_{ds} = 385$ V. If one makes the conservative assumption that the real SEB cross section is at the limit of our ability to measure, the projected failure rate is approximately 3.5 orders of magnitude smaller than the 500V MOSFETs currently in the VME supplies. This would give a conservative SEB failure rate of one power supply every 60 years.

For the silicon HV power supplies, A naive application of the measured cross sections to the racks where the silicon HV supplies are located yields a failure rate significantly lower than has already been observed. However, predicting the failure rates for the silicon supplies is more difficult than for the VME supplies. The number of failures in the CDF collision hall were low and the radiation conditions in the CDF collision hall are different than that at IUC-RERF. The data from Indiana does yield a good idea of the *relative* failure rates of each component which is adequate for most of our needs. In all cases where a candidate replacement component has been proposed the new component exhibited a failure rate roughly two orders of magnitude lower than the one that is being replaced. The SCRs had a failure rate too low to be measured which gives us confidence that they will not result in operational difficulties.

The only component that requires further consideration are the CAEN MOSFETs which are currently installed at 250V, since the repercussions of this type of failure would be so severe.

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