RTF DESIGN SPECIFICATIONS

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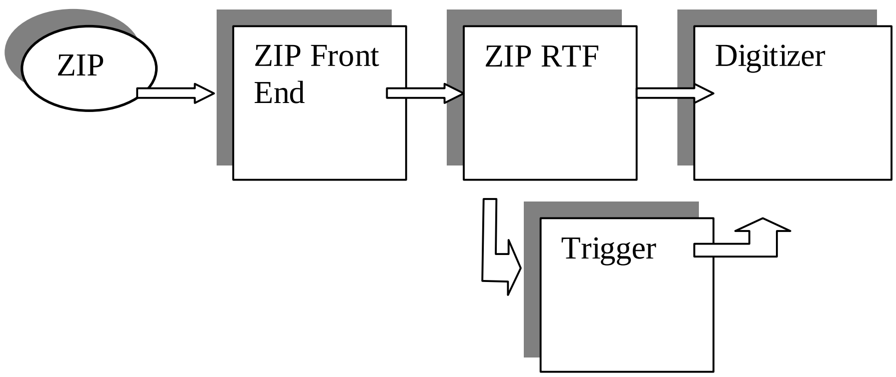


RTF DESIGN SPECIFICATIONS

1 The RTF Module

The RTF (Receive Trigger Filter) module provides an interface between the ZIP (Z-sensitive Ionization and Phonon) front end module and the DAQ (Data AcQuisition) system. The RTF module's multifunctionality is reflected in its name. A block diagram of "The RTF Module" may be viewed on page 11.

2 Receive

Six signals are received from the ZIP front end module; four phonon signals and two charge signals. Each of these signals is received differentially by an INA103K instrumentation amplifier via a 25-pin D connector located at the rear of the module.

The amplifier receives differential signals from the backplane, via the 25-pin D connector and converts them to single-ended signals referenced to analog ground.

Each received signal drives both the Trigger circuitry and the Filter circuitry.

3 Trigger

- Block diagrams of the Charge and Phonon Trigger circuitry may be viewed on pages 12 and 13, respectively.

- Each RTF trigger input signal from the front end will be switchable to either Si or Ge bandpass circuitry. The selection will be via jumpers on the board. The position of the jumper will be clearly labelled on the board.   The present position of the jumper (Si or Ge) will be indicated by an LED on the front panel and via computer.

- Each bandpass will be formed by a low pass and a high pass filter. Each filter will be a single pole filter, with a rolloff of 20dB / decade. The bandpass for each circuit will be determined during Run 20.

- There will be two charge (Q HI and Q LO) and three phonon trigger outputs (P HI, P LO, and P WISP).

- The gain for Q LO, P LO, and P WISP will be 100. The gain for Q HI and P HI will be 1/2.

- Inputs to the summing circuits will be selected via computer-controlled switches.

- To prevent multiple triggering on a noisy signal, the trigger circuit for P HI, P LO, P WISP, Q HI, and Q LO will have 80% hysteresis. The threshold level will drop to 20% of the initial value after triggering. The initial value will be restored after triggering on the lower level as shown in FIG. 1.

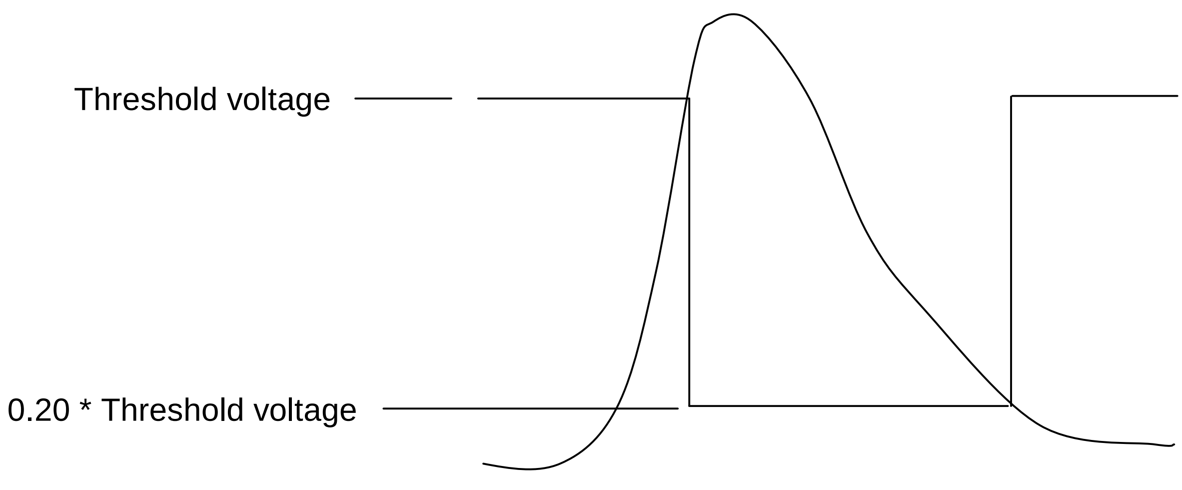


FIG. 1 Hysteresis of threshold voltage

- In the event P WISP has problems with multiple triggering on a noisy signal using the hysteresis circuit described above, an alternative trigger circuit for P WISP using a non-retriggerable one-shot with a 100us delay will be provided. The switch between the two options would require a change in hardwiring.

- There are seven outputs each for P HI, P LO, P WISP, Q HI, and Q LO. These outputs and their destinations are shown in TABLE 1.

Output signal	Destination
Trigger from 1 us oneshor	Trigger conditioner
Trigger from 1 us oneshot	Front panel test port
Trigger from 1 us oneshot	Scalar
Trigger from 20 ms oneshot	Front panel LED
Threshold	Slow ADC
Threshold	Front panel test port
Filtered output	Front panel test port

TABLE 1 RTF board trigger, threshold, and filter output signals

4 Filter

- A block diagram of the filter circuitry, titled "RTF Filter", may be viewed on page 14.

- Either a -1.5 V offset (to match the ±2V bipolar range of the digitizers) or no offset will be applied to the signal via a computer-controlled switch prior to digitization.

- Care will be taken in the design to ensure that signals input to the digitizer do not exceed limits that will cause damage. The input amplifier of the Joerger digitizer is powered by ±5V, so clamping the input signal to the digitizer at ±5V will be sufficient to protect the digitizer.

- There will be two signal outputs per channel.

  One output, filtered by a four-pole Butterworth antialias filter with a jumper-selectable choice of 0.5 MHz or 1 MHz rolloff frequency (corresponding to digitization at 1.25 MHz or 2.5 MHz), will go to the digitizer. The present position of the jumper will be indicated by an LED on the front panel. The filter will be constructed with discrete components with noise <0.5mV (i.e. less than digitizer noise). The front end receiver circuit on the VTR812 Joerger Digitizer is shown on page 18.

  The other output, with no filtering, will go to a front panel test port for monitoring on test equipment.

- These outputs and their destinations are shown in TABLE 2.

Output signal	Destination
Anti-aliased signal (jumper-selectable 0.5 MHz or 1 MHz)	Joerger fast digitizer
Unfiltered signal	Front panel test port

TABLE 2 RTF board signal outputs and their destination

5 Slow signals

- A block diagram of the slow signal circutiry, titled "RTF Slow Signals", may be viewed on page 15.

- There will be provision for five slow signals. Four of these will be used to monitor the SQUID amplifier feedback DC voltage. The remaining one will be a spare.

- The five slow signals will be input via the 25-pin D connector multipin connector on the back of the RTF board. This is the same 25-pin D connector that brings in the four phonon and two charge signals.

- The outputs will be buffered with a gain of one.

- The outputs will be split with one output to a slow ADC and the other output to a front panel test port. These outputs and their destinations are shown in TABLE 3.

Output signal	Destination
Buffered with gain of one	Slow ADC
Buffered with gain of one	Front panel test port

TABLE 3 RTF slow signal outputs and their destination

6 RTF input signal characteristics

Input signal	*Source*	*ZIP Board Source Impedance*	*Typical signal level*	*Absolute maximum voltage*
Phonon (A,B,C,D)	ZIP front end	50 Ω	0-4V	$\pm$15V
Charge (Qi, Qo)	ZIP front end	50 Ω	0-4V	$\pm$15V
Slow signal SQUID dc feedback	ZIP front end	20k Ω	<1V	$\pm$15V

7 RTF output signal requirements

Output signal	*Destination*	*Input impedance*	*Typical signal level*	*Absolute maximum voltage*	*Pulse width and tolerance*
Antialiased signal	Fast digitizer (Joerger VTR812)	50Ω or 10MΩ	0-4V or ±2V	>2V clamp without compromising pulse	
Trigger from 1us oneshot	Trigger conditioner	100kΩ to GND	Logic 0 0 - 1.16V Logic 1 1.6-5.0V defined by XILINX XC4000	5.5 V	
Trigger from 1us oneshot	Scaler	50Ω to GND or 500Ω to 5V	TTL	TTL	10ns<t<1us*
Threshold	Slow ADC	5MΩ in parallel with 50pF	0-5V	10V	
SQUID DC feedback	Slow ADC		<1V	10V	

* Interval chosen to both minimize the chance of double-counting on noise and to avoid missing a count due to pulse pileup

8 Summary of all output signals

For ease of viewing, all RTF outputs described above are presented below:

Output signal	Destination
Trigger from 1 us oneshor	Trigger conditioner
Trigger from 1 us oneshot	Front panel test port
Trigger from 1 us oneshot	Scalar
Trigger from 20 ms oneshot	Front panel LED
Threshold	Slow ADC
Threshold	Front panel test port
Filtered output	Front panel test port

TABLE 1 RTF board trigger, threshold, and filter output signals

Output signal	Destination
Anti-aliased signal (jumper-selectable 0.5 MHz or 1 MHz)	Joerger fast digitizer
Unfiltered signal	Front panel test port

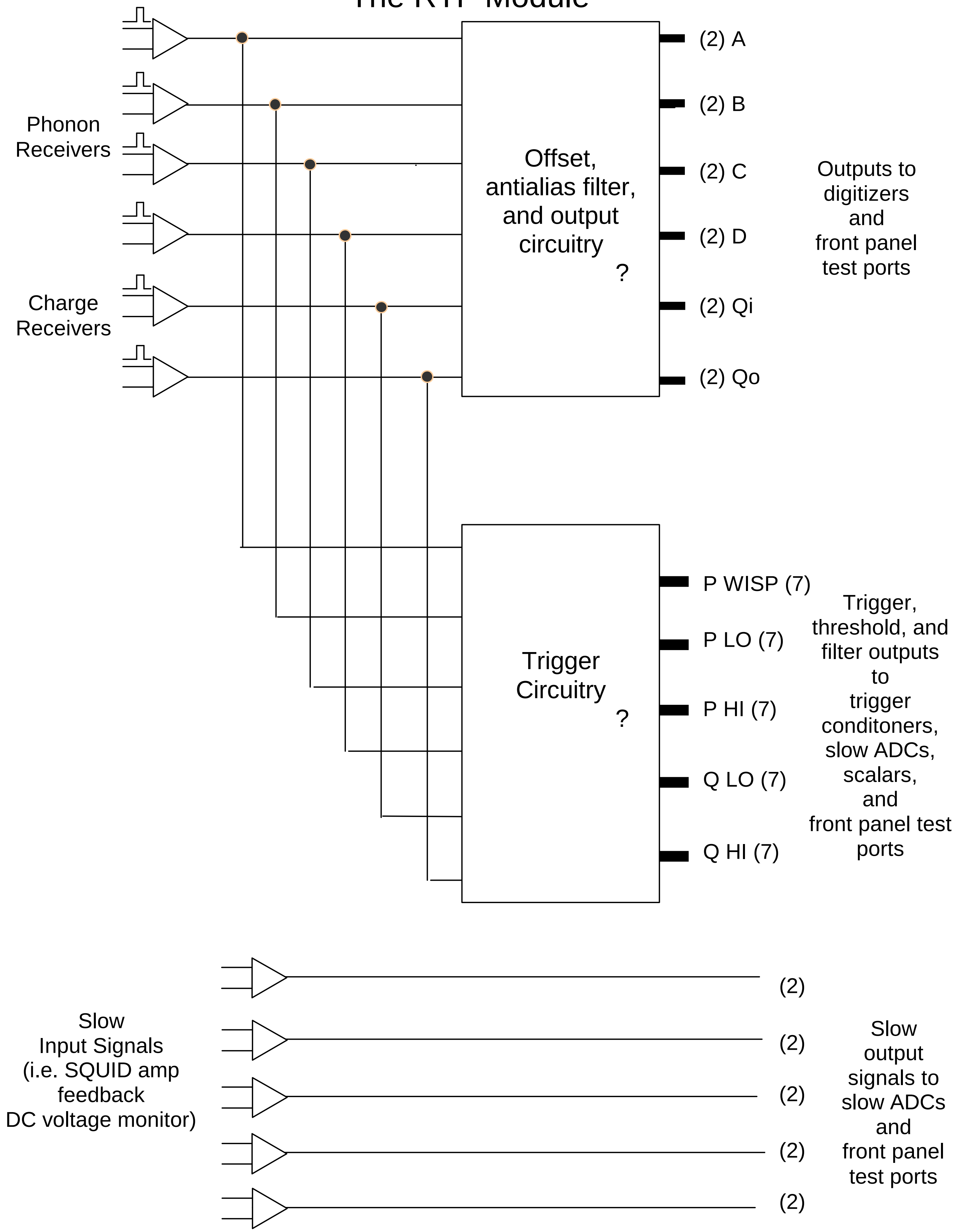
TABLE 2 RTF board signal outputs and their destination

Output signal	Destination
Buffered with gain of one	Slow ADC
Buffered with gain of one	Front panel test port

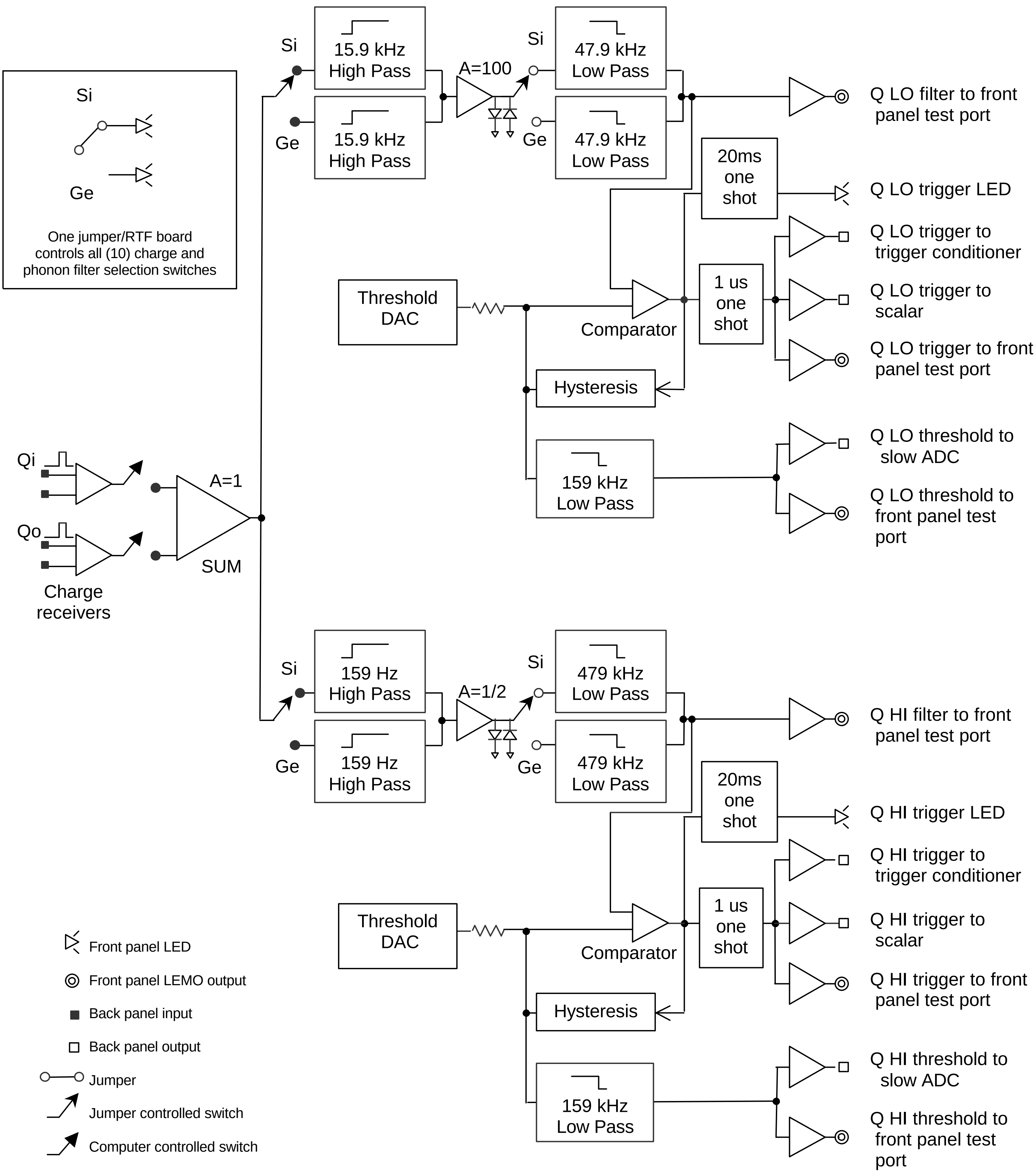
TABLE 3 RTF slow signal outputs and their destination

9 RTF Block Diagrams

The RTF Module

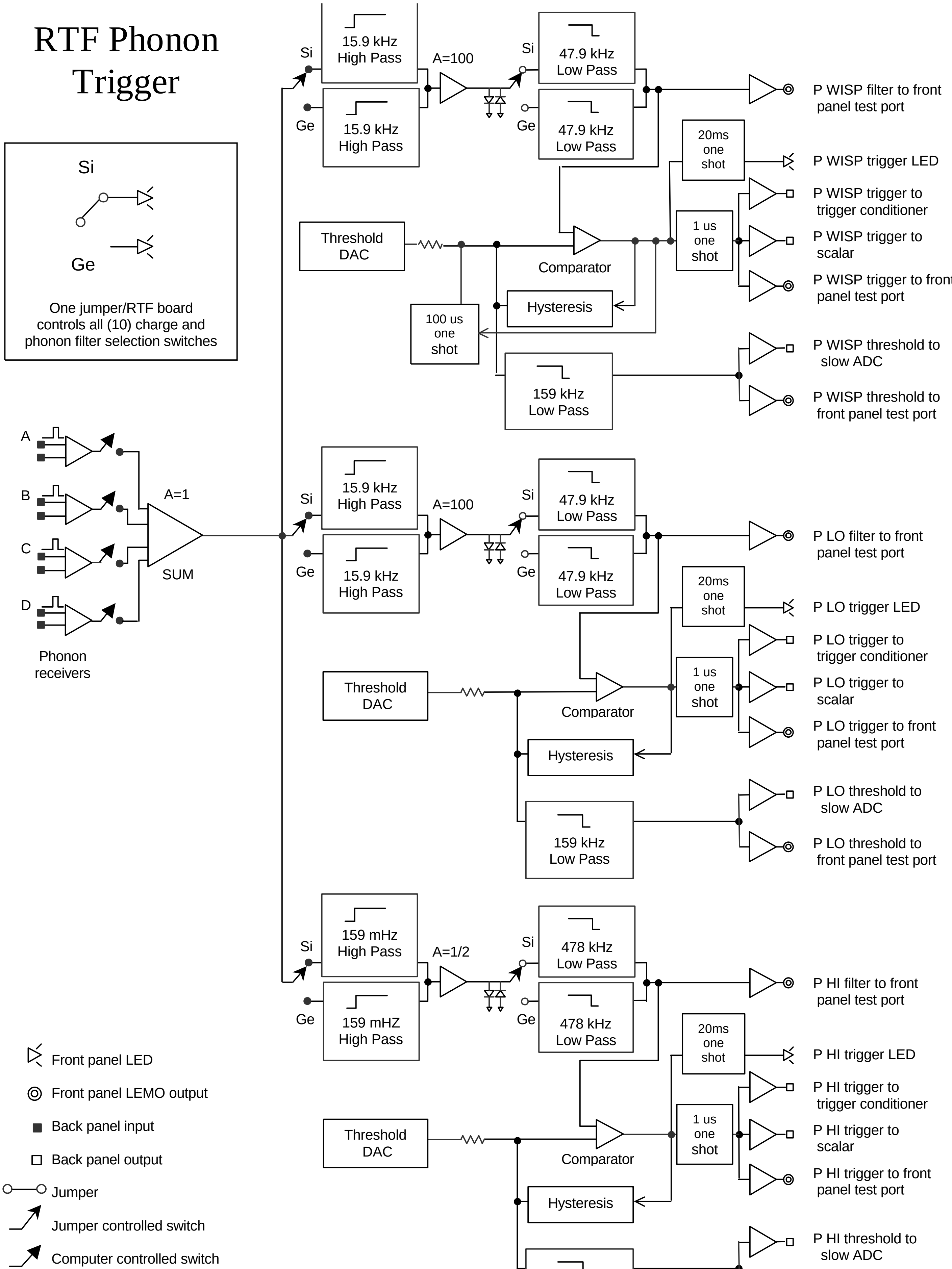


RTF Charge Trigger



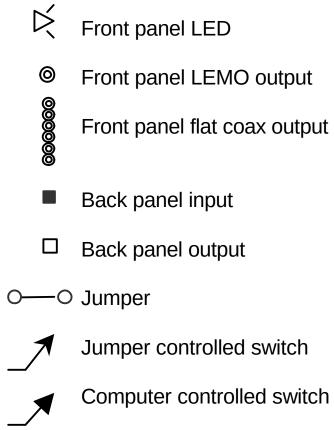
The bandpasses for Si and Ge will be determined during Run 20.
The frequencies shown are those currently used on the RTF board.

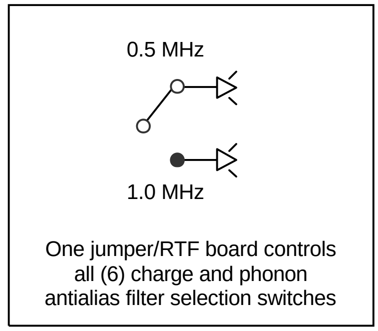
RTF Phonon Trigger

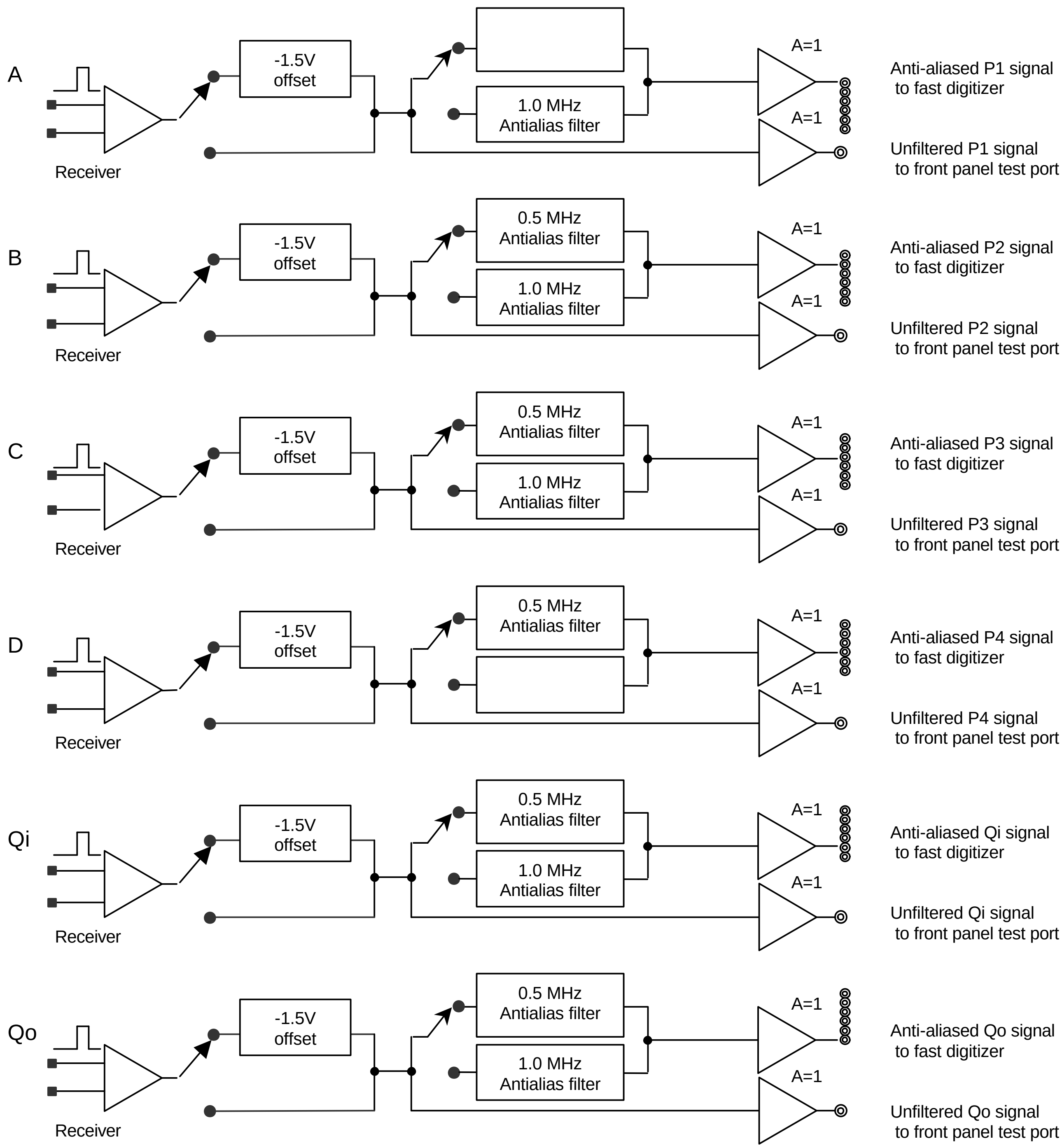


The bandpasses for Si and Ge will be determined during Run 20.
The frequencies shown are those currently used on the RTF board.

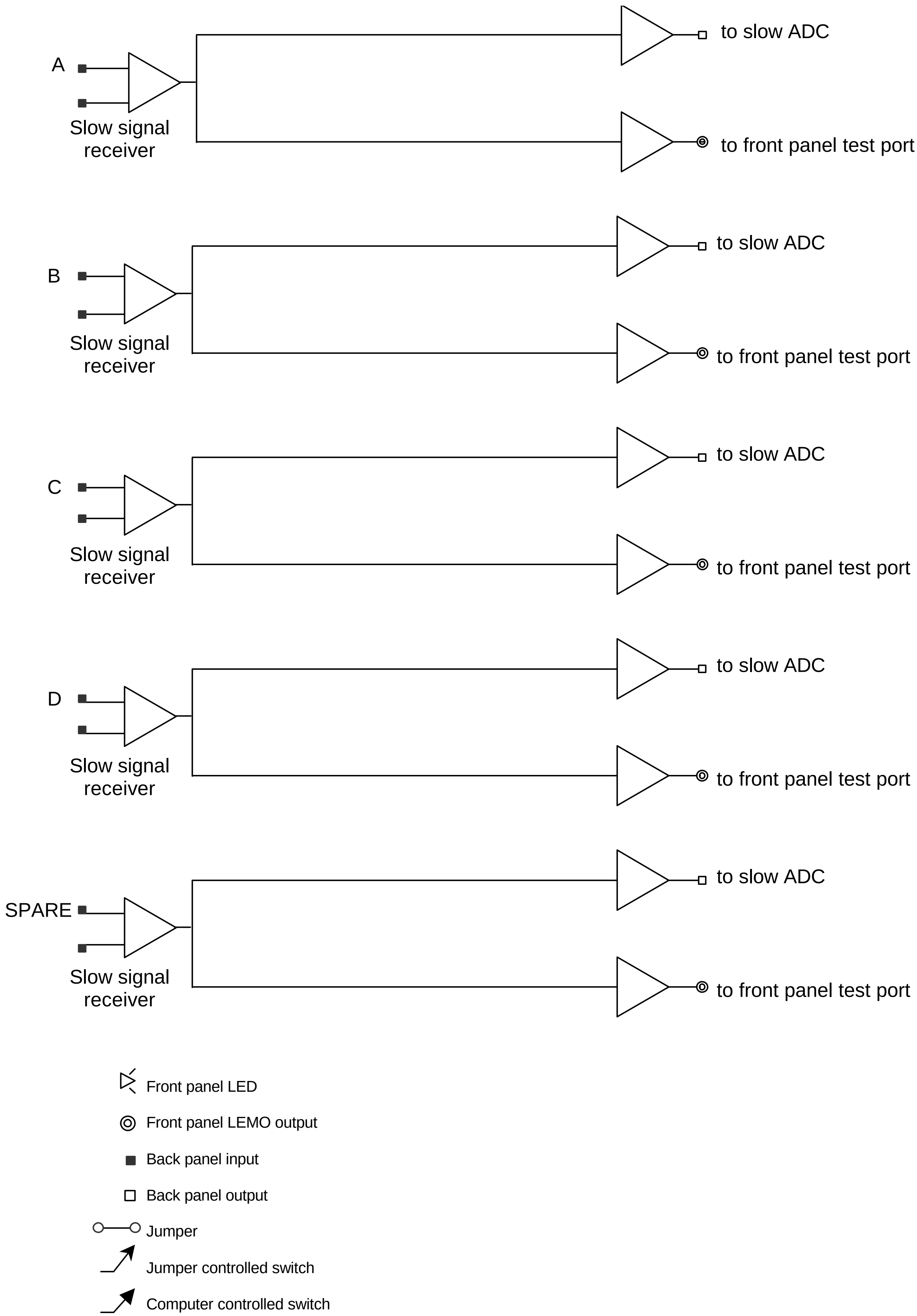
RTF filter (Physics signals)



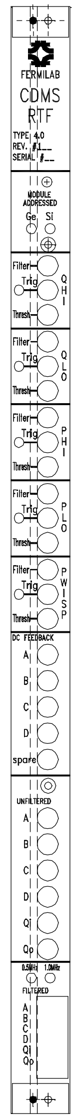




RTF Slow Signals
DC FEEDBACK

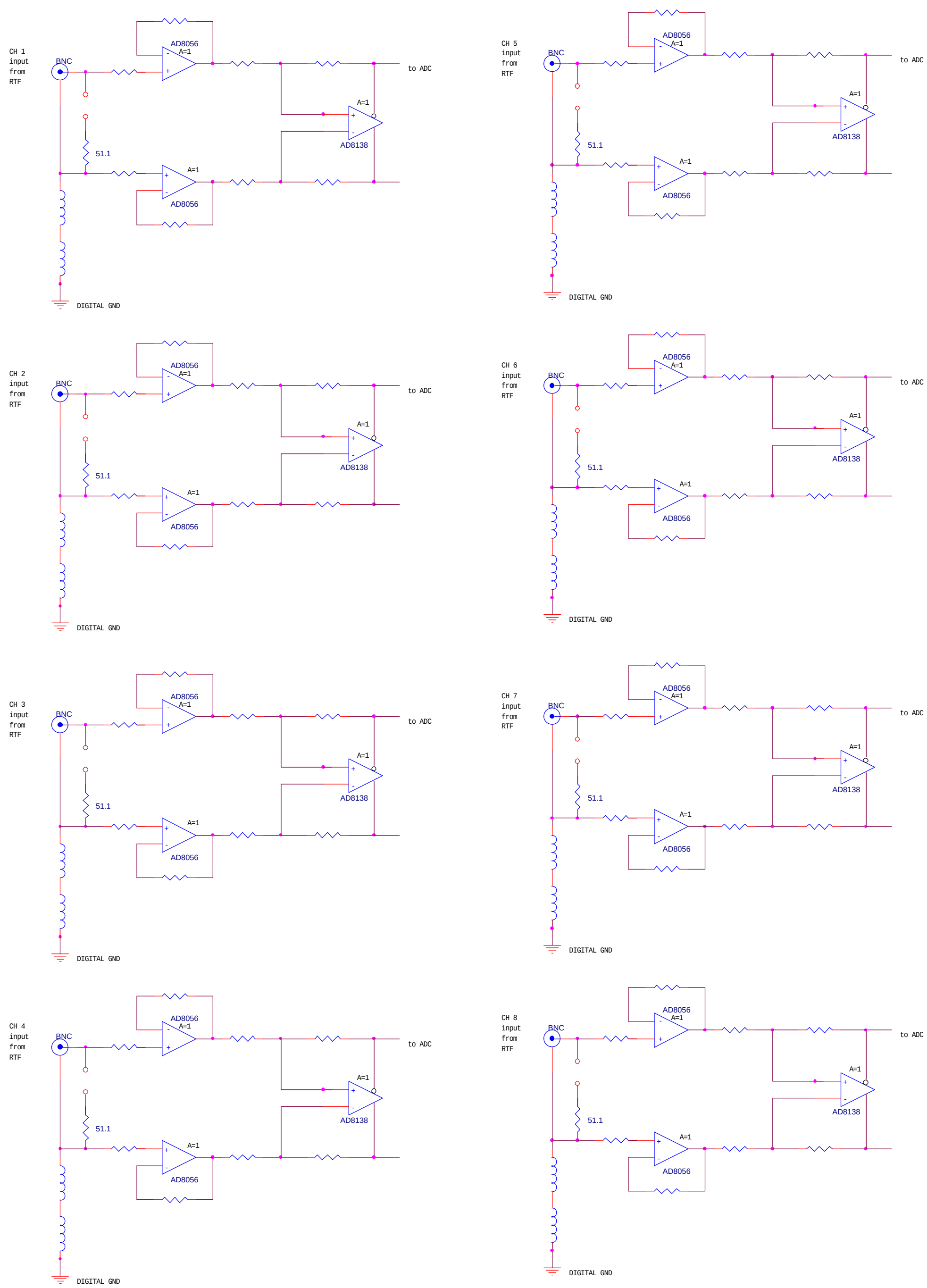


10 RTF front panel



8 Joerger VTR812 front end receiver

Front end receivers on
Joergers VTR812 digitizer



NOTE 1 Each channel has its own ANALOG GND.

NOTE 2 There is one DIGITAL GND.

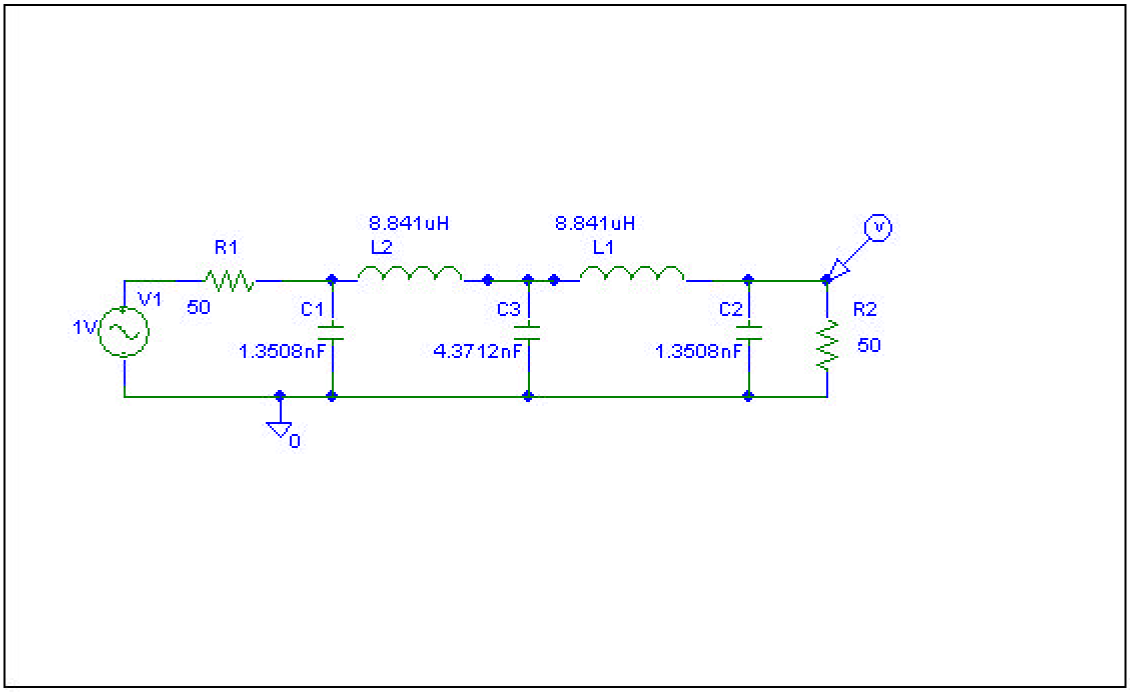
NOTE 3 DIGITAL GND is the same as VME GND.

NOTE 4 The 8 separate ANALOG GNDs are all connected to DIGITAL GND via a series pair of ferrite beads (indicated by inductors in the schematic).

NOTE 5 The beads provide some isolation from channel to channel and impede digital noise from the analog signals.

NOTE 6 The two beads comprising each pair have different values to provide a wide range of frequency isolation.

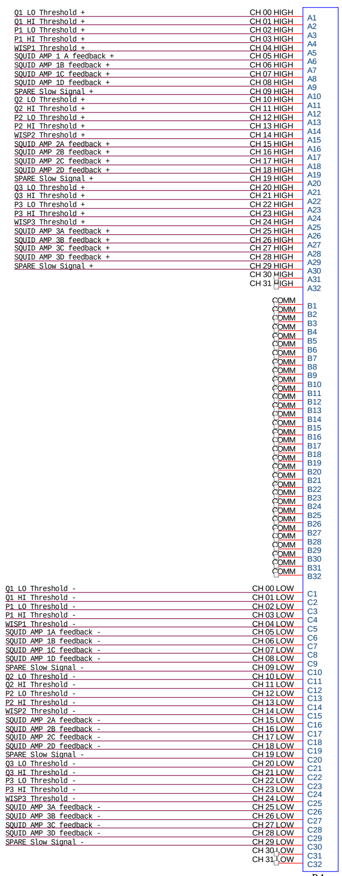
12 Preliminary Butterworth antialias filter



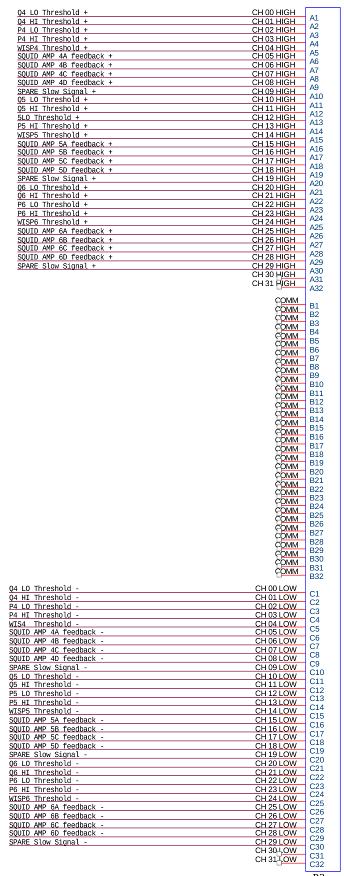
12 Backplane wiring, connectors, and pinouts

TOWER 1

Left Slot
Trigger Conditioner



P4
Slow ADC #1

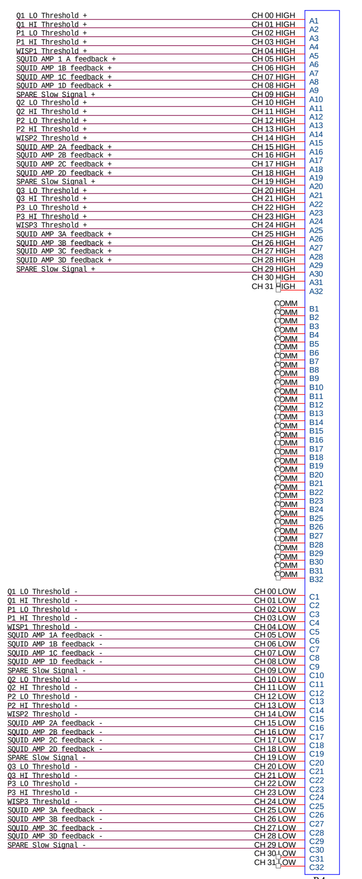


P3
Slow ADC #1

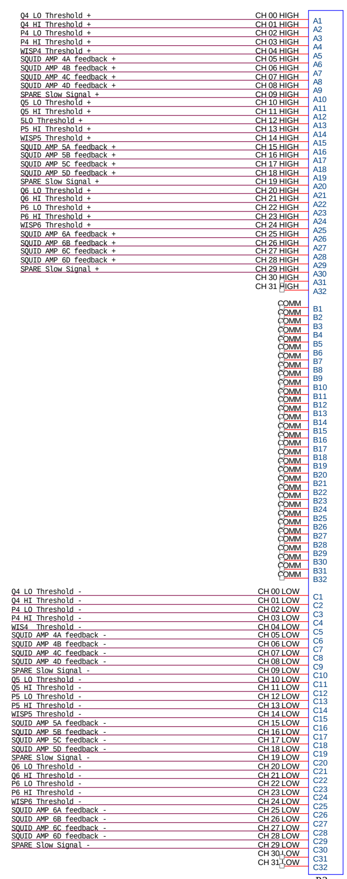
Connector A
Scaler 1

TOWER 2

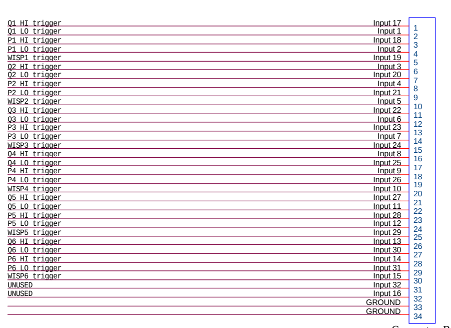
Right Slot
Trigger Conditioner



P4
Slow ADC #2

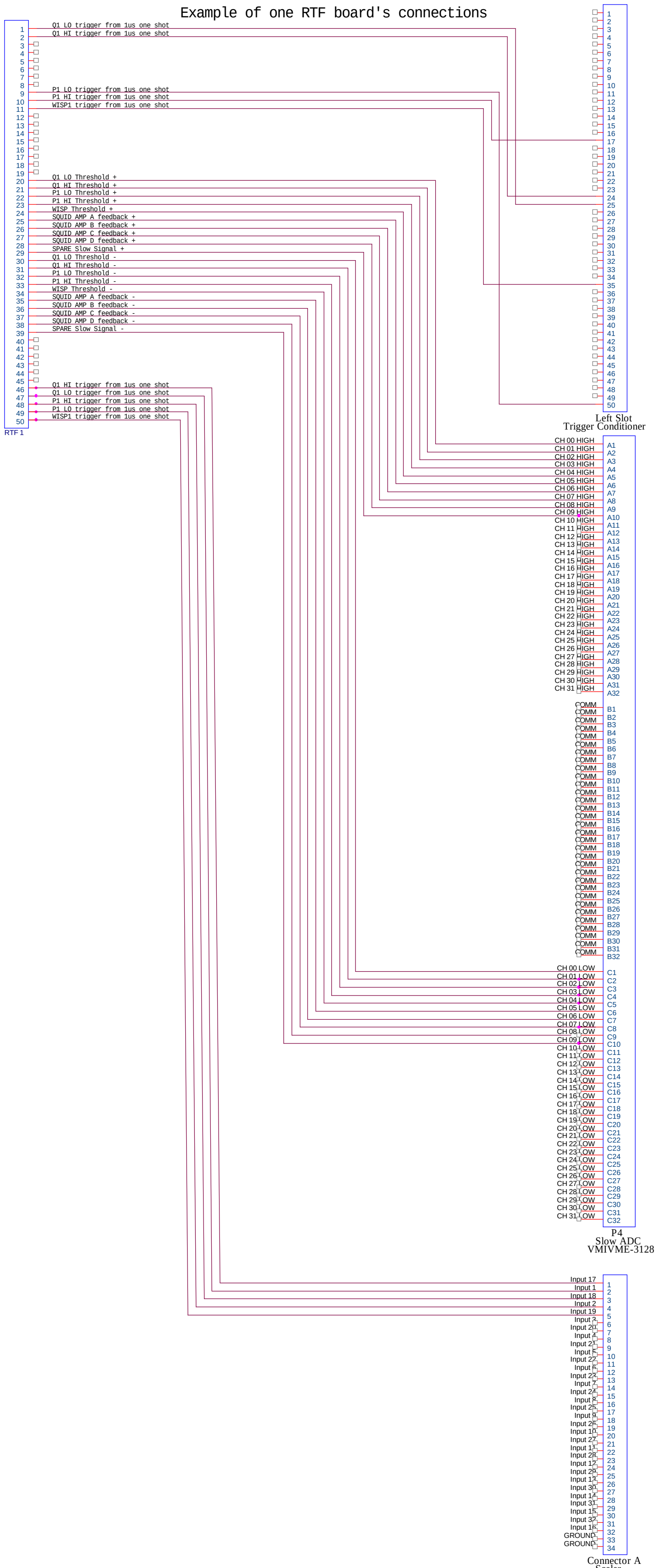


P3
Slow ADC #2

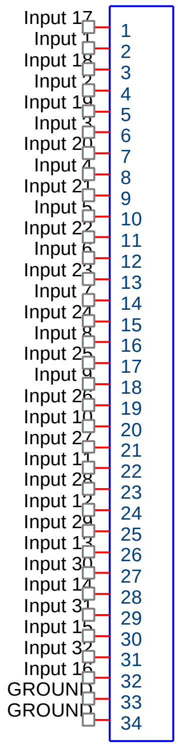


Connector B
Scaler 1

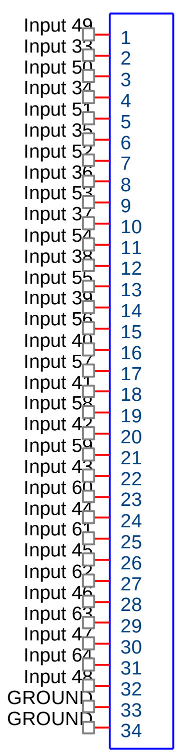
Example of one RTF board's connections



Joerger Model VS64 Scale

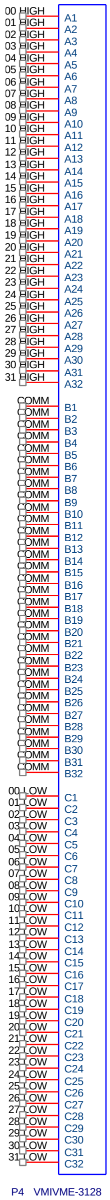


Connector A



Connector B

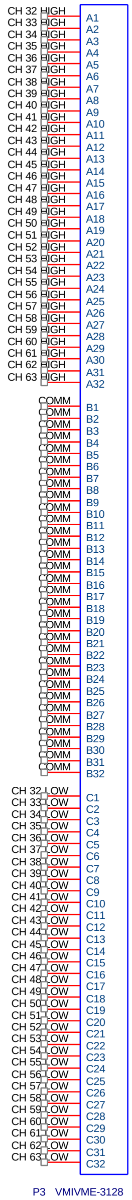
VMIVME-3128 ADC



ROW A = High inputs

ROW B = Analog ground on ADC board
Might connect shields here

ROW C = Low inputs



DIFFERENTIAL MODE
ROW A = high inputs
ROW C = low inputs

PSEUDODIFFERENTIAL MODE
CH 31 LO and CH 63 LO =
Analog ground
This implies all connected
channels must be referenced
to the same ground.

SINGLE ENDED
This method uses on-board
analog ground
as the input signal
reference