

Non-Destructive Evaluation of Thermal Barrier Coatings by Electrochemical Impedance Spectroscopy

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Introduction

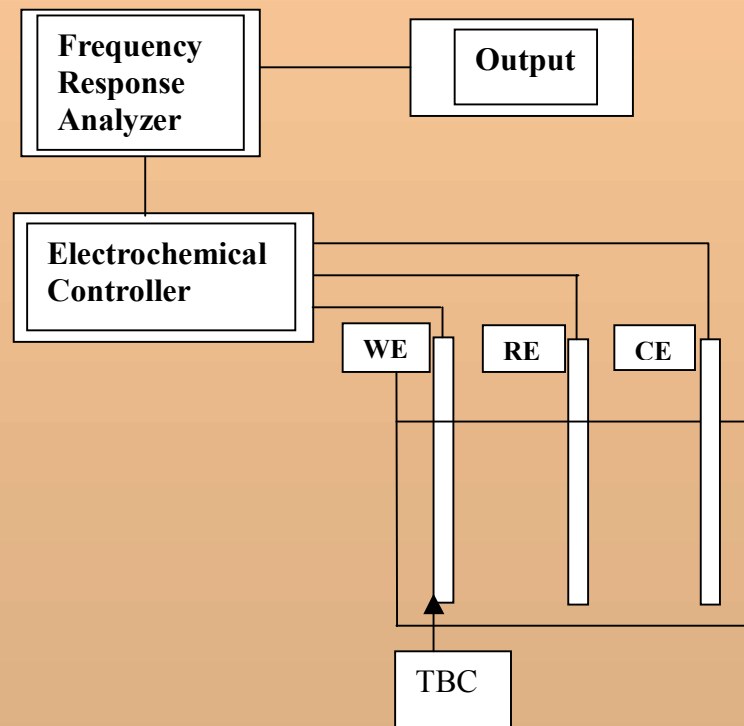
- **The Advanced Turbine Systems (ATS) will operate at Turbine inlet temperatures (TIT) of about 2750°F to obtain 60% and higher efficiencies.**
- **There is a need for the application of thermal barrier coatings (TBCs) at these temperatures, because the superalloys cooled using conventional cooling techniques can not withstand more than 2100°F.**
- **For land based gas turbines, which operate for long periods without inspection, reliability and quality assurance of TBCs is a critical issue. Development of an in-situ NDE technique for the evaluation and monitoring of TBCs is therefore desirable to ensure trouble free service.**
- **Electrochemical impedance spectroscopy (EIS) has been utilized as an NDE technique for the characterization of various coatings in aqueous environments. In the present work, we attempt to evaluate and develop EIS as a tool for the in-situ monitoring of TBCs.**

- **Materials:**

Yttria stabilized ZrO₂ TBCs are used in the present study because of their success in aerospace industry and their potential for use in power generation applications.

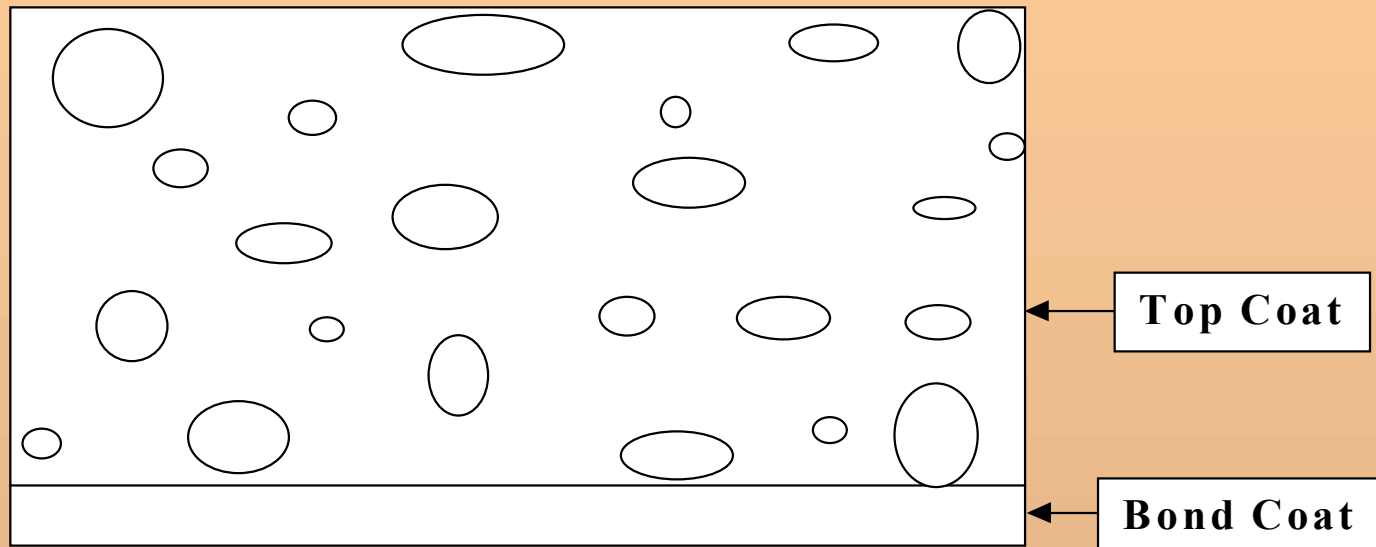
- **EIS Setup:**

The **EIS technique** is a multiple-electrode electro-chemical measurement system. The impedance $Z(\omega)$ of an interface is determined over a large frequency range by applying a small a.c. signal $V(\omega)$ and measuring its response $I(\omega)$.



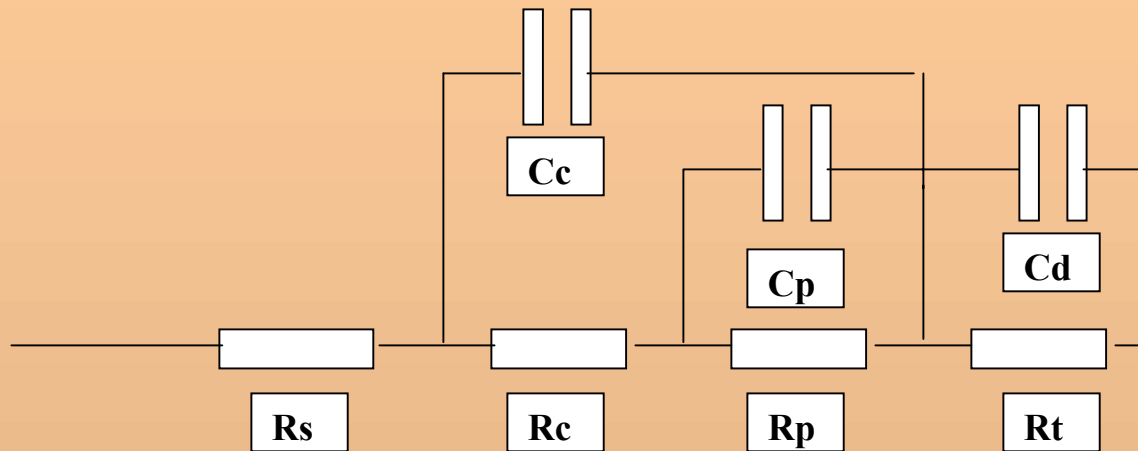
The Schematic of an EIS setup

Morphology of Intact TBC



A TBC consists of two-layers: a ceramic top coat over a metallic bond coat. The ceramic top coat may contain various types of defects, such as porosity (as shown above), cracks, delamination etc.

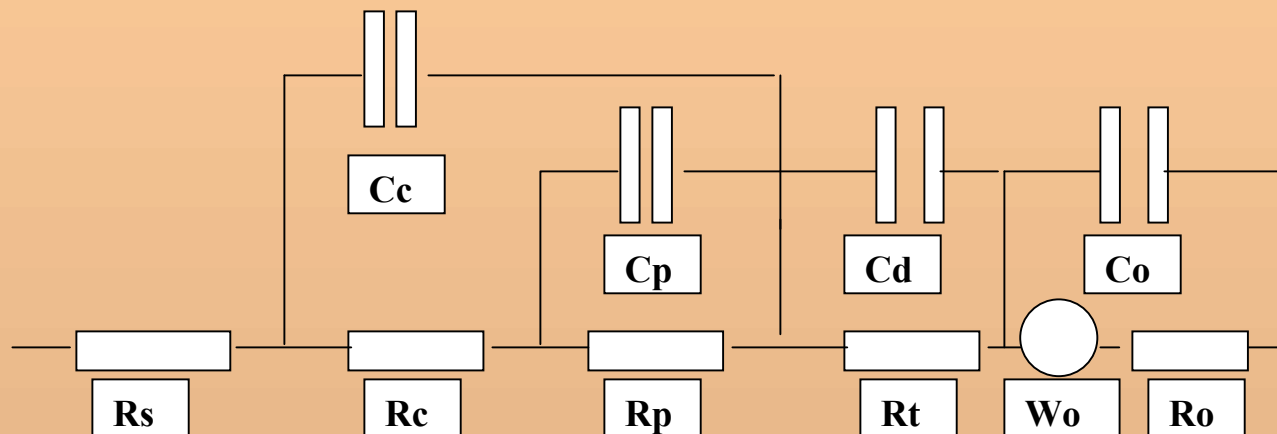
EIS Equivalent AC Circuit for Intact TBC



The impedance $Z(\tilde{\omega})$ of the equivalent circuit can be given by:

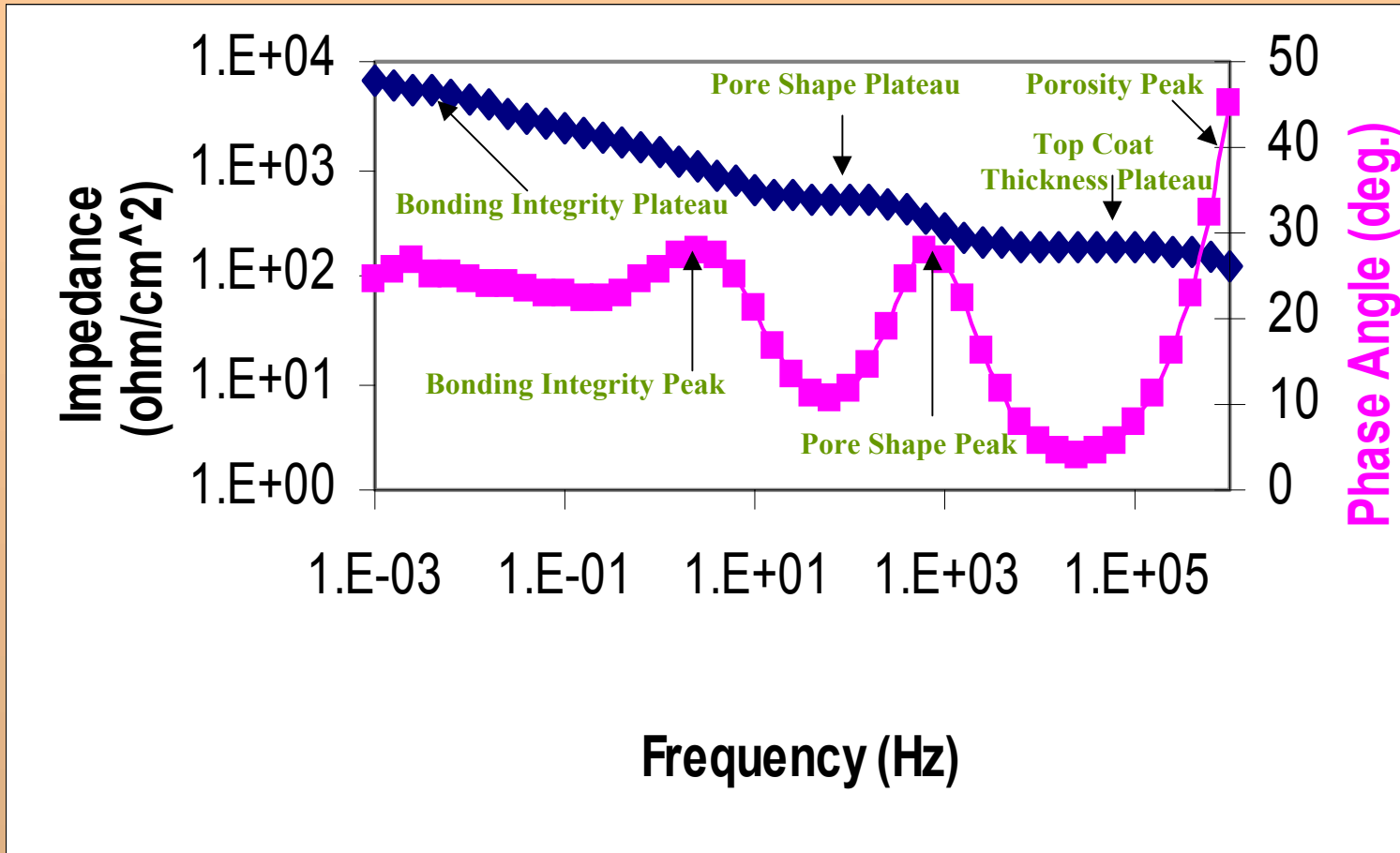
$$Z(\tilde{\omega}) = R_s + \{ [R_c + (j\tilde{\omega} C_p + R_p^{-1})^{-1}]^{-1} + j\tilde{\omega} C_c \}^{-1} + (j\tilde{\omega} C_d + R_t^{-1})^{-1}$$

EIS Equivalent AC Circuit for TBC Exposed to Oxidation and Thermal Shocks

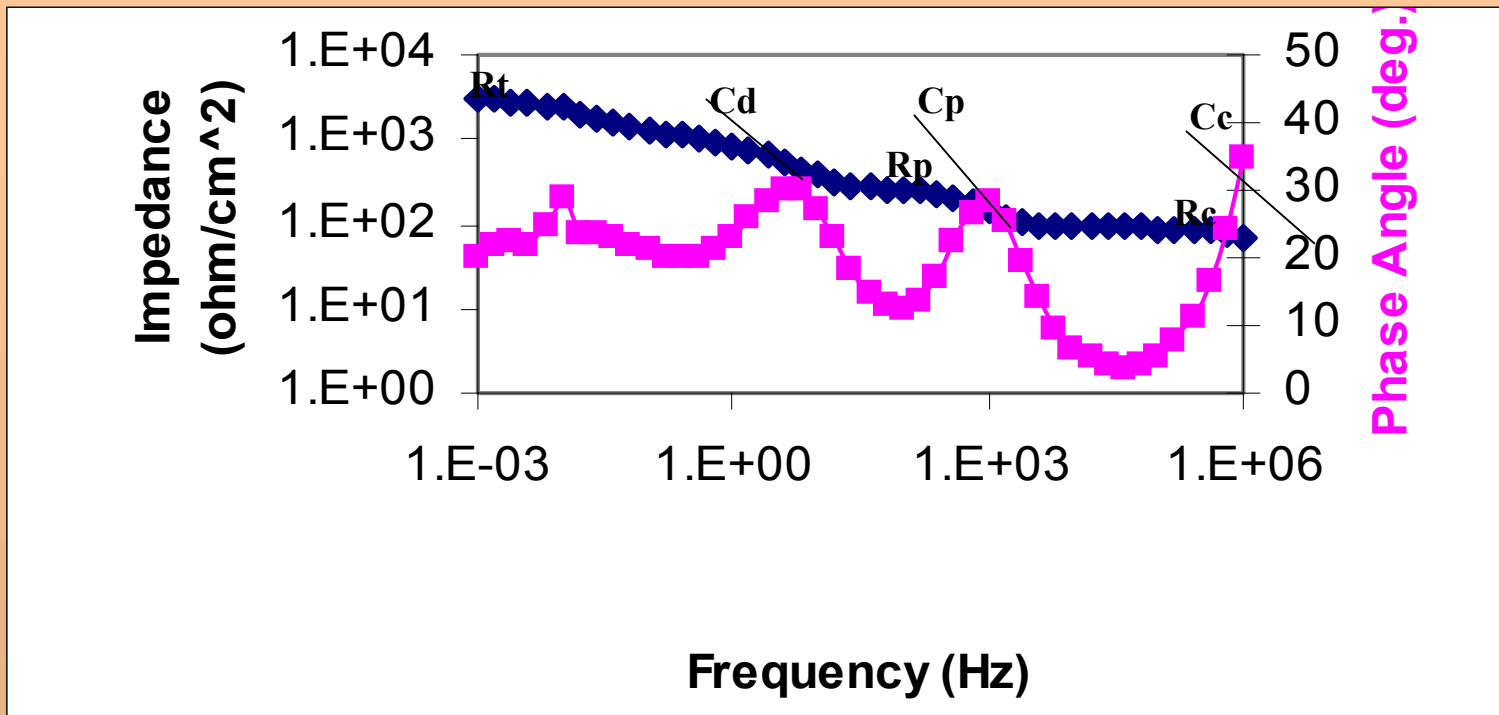


The impedance $Z(\tilde{\omega})$ of the equivalent circuit can be given by:

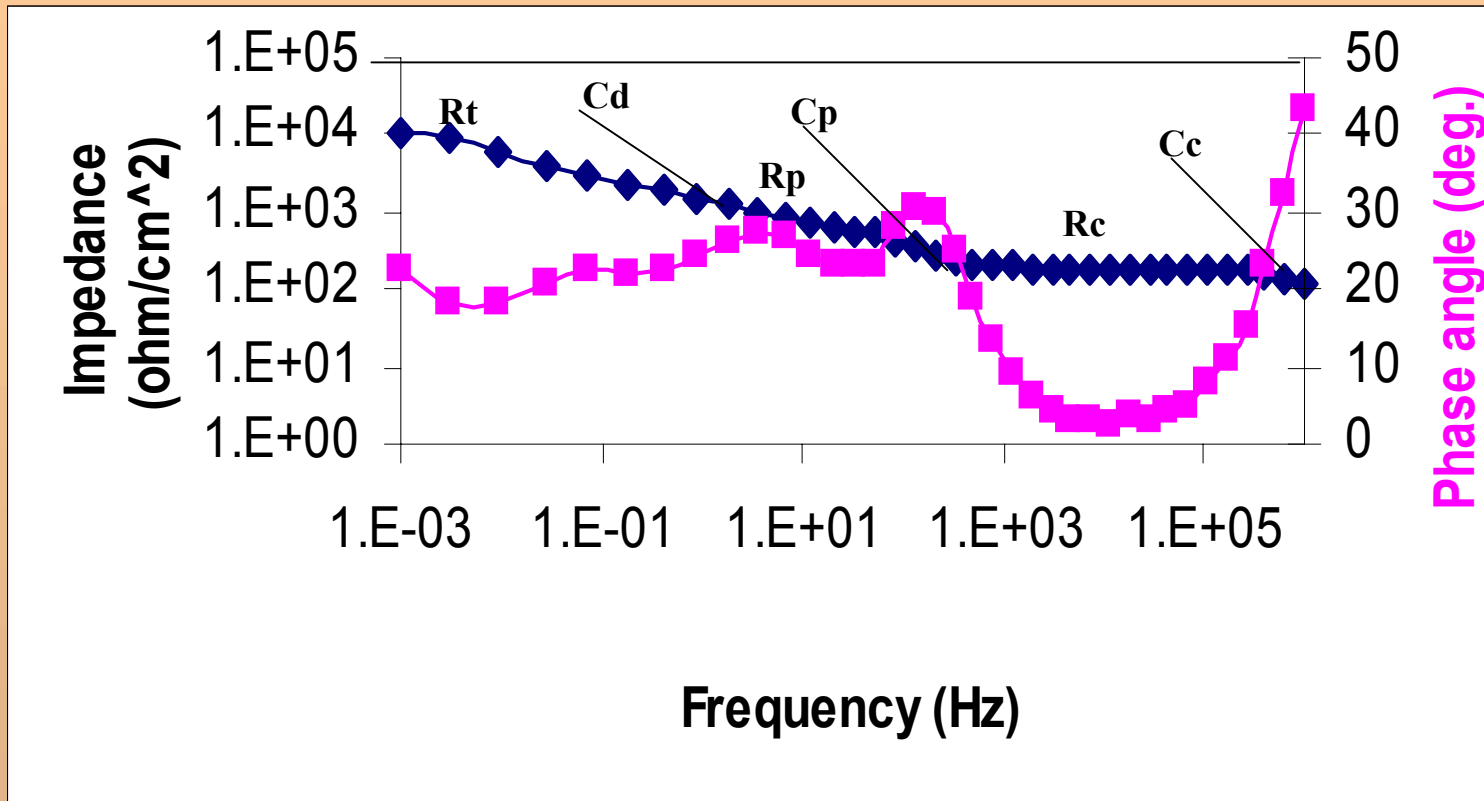
$$Z(\tilde{\omega}) = R_s + \left\{ \left[R_c + (j\tilde{\omega} C_p + R_p^{-1})^{-1} \right]^{-1} + j\tilde{\omega} C_c \right\}^{-1} + (j\tilde{\omega} C_d + R_t^{-1})^{-1} + [j\tilde{\omega} C_o + (W_o + R_o)^{-1}]^{-1}$$



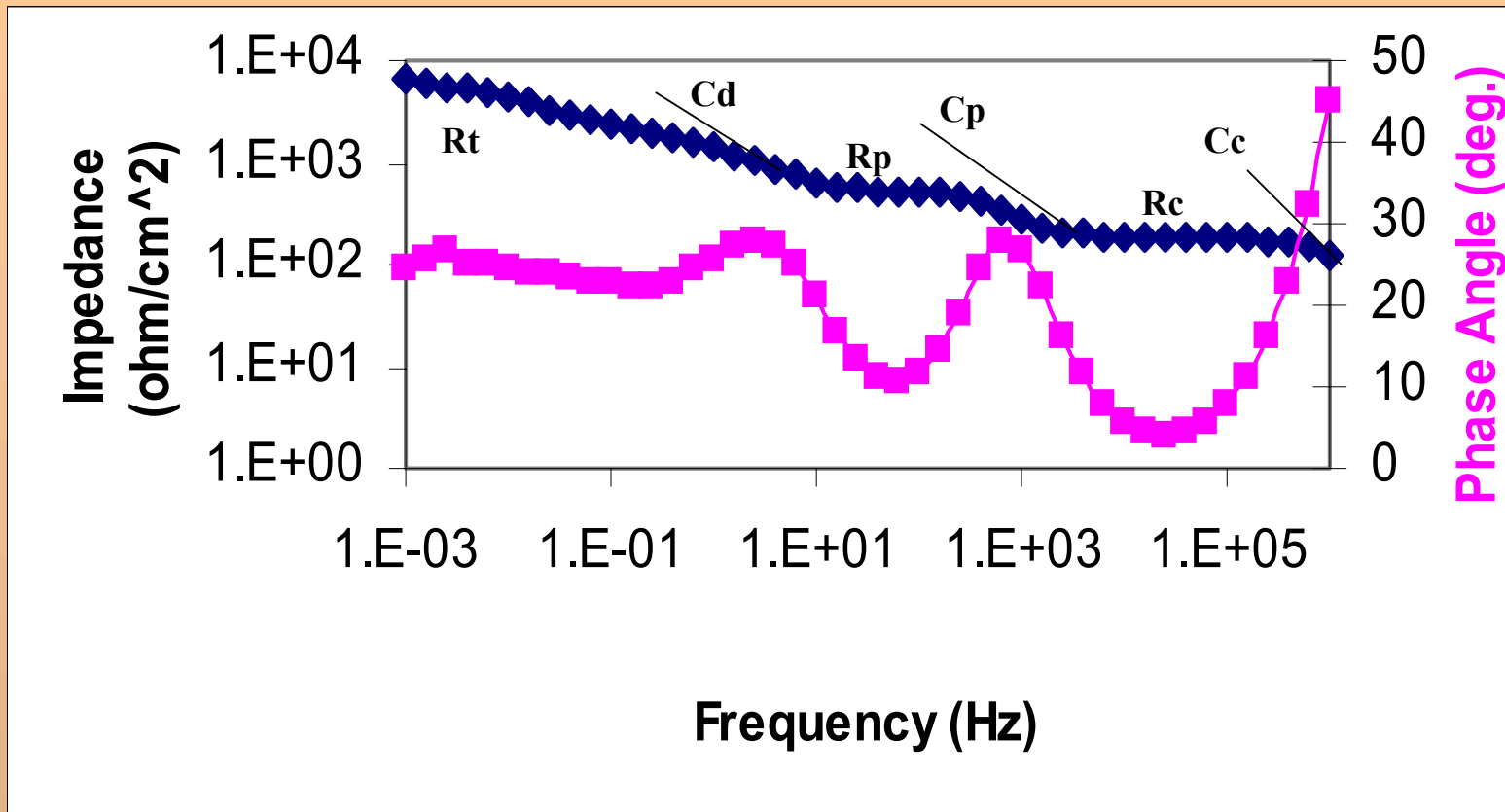
A Typical EIS Bode Plot of Intact TBC



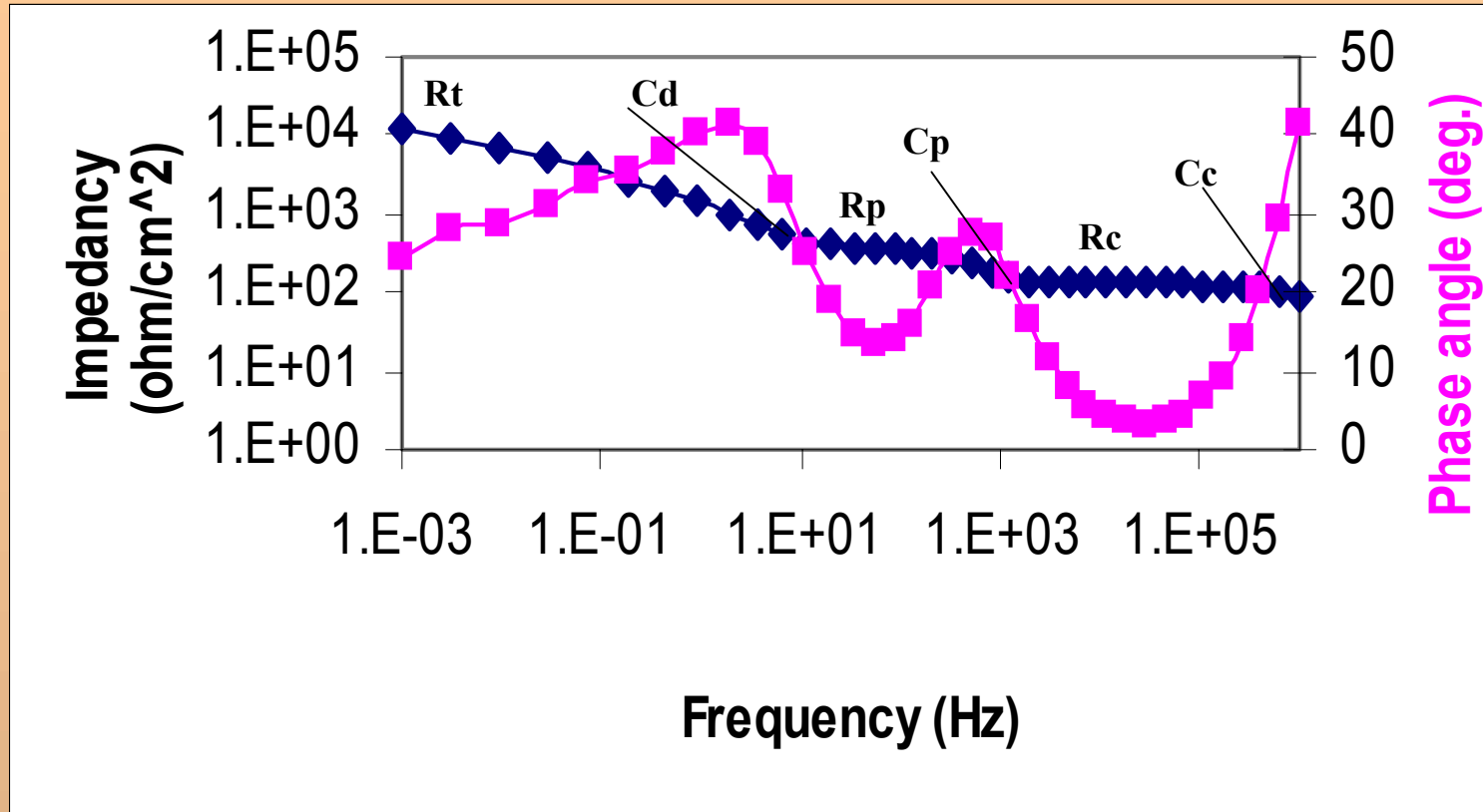
EIS Bode Plot of a TBC with Top Coat Thickness of 200µm
($R_c = 90$ ohms)



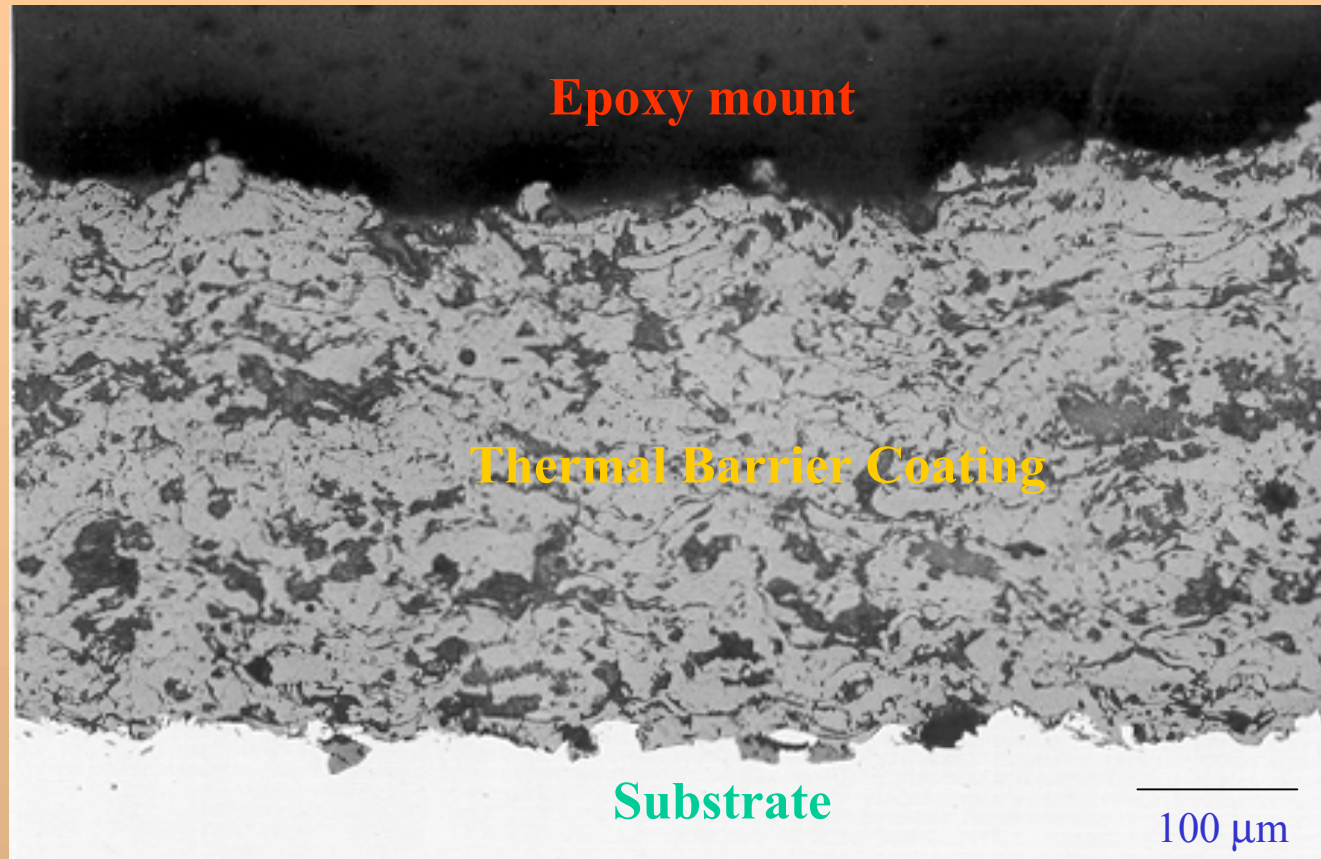
EIS Bode Plot of a TBC with a Top Coat Thickness of 400µm
(Rc = 190 ohms)



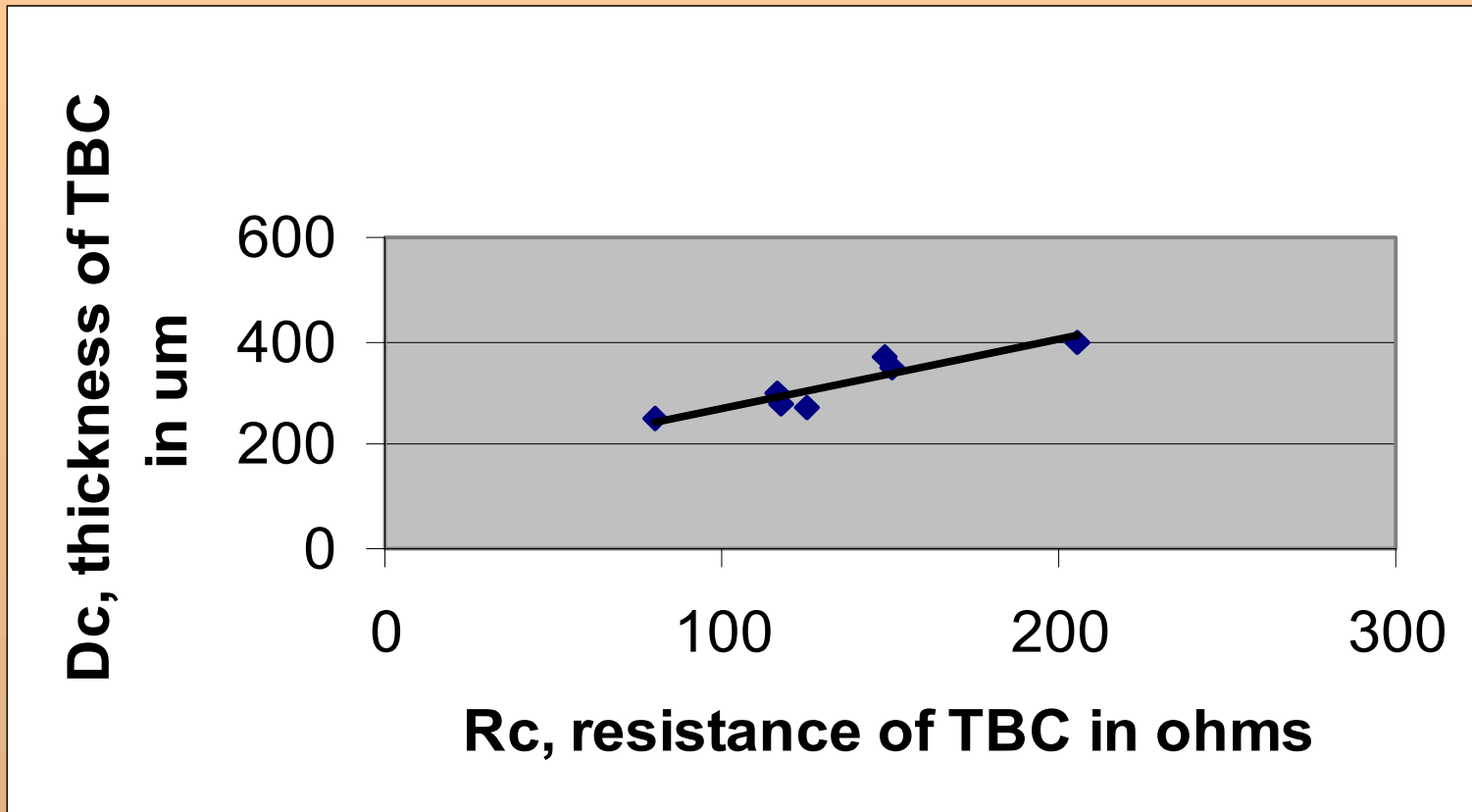
EIS Bode Plot of a TBC with a Low Porosity Top Coat
(Cc = 1.6 nF)



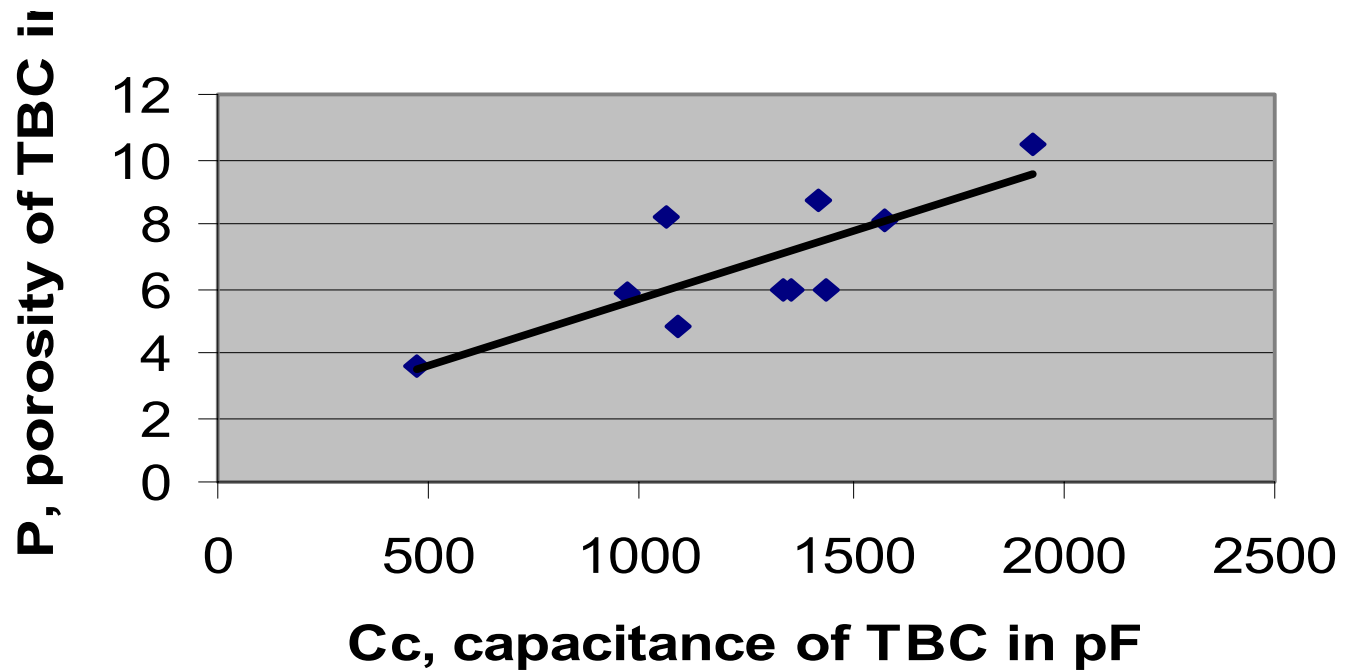
EIS Bode Plot of a TBC with a Higher Porosity Top Coat
($C_c = 3.7$ nF)



Cross-Sectional Morphology of a Typical TBC Top Coat with High Porosity



Linear Relationship between the Thickness, Dc and the Resistance, Rc of Intact TBCs



Linear Relationship between the Porosity, P (%) and the Capacitance, Cc of Intact TBCs

EIS Results for Intact TBCs

- a. Coating thickness, $D_c = (2.1 \pm 0.3) R_c$ (μm)

- b. Coating porosity, High porosity when $C_c \geq 2.5\text{nF}$,
Medium porosity when $C_c = 1.8\text{-}2.5\text{nF}$, and
Low porosity when $C_c \leq 1.6\text{nF}$.

- c. Pore shape, “le” when $R_p \leq 500\text{ohms}$,
“c” when $R_p = 500\text{-}700\text{ohms}$, and
“te” when $R_p \geq 700\text{ohms}$.

(le: longitudinal elongated; c: circular; te: transverse elongated)

EIS Relations for Exposed TBCs

Oxidation

- Theoretical kinetic relationships like the one shown below can be established to correlate % porosity as a function of time and ceramic capacitance.

$$C_c \text{ (theo)} = \{[0.00361 \ln(t) - 0.0243] (152.47P + 233.26)\} + 284.85 \text{ in pF}$$

$$P \text{ (theo)} = [C_c - 284.85] / [0.5504 \ln(t) - 3.705] - 1.53 \text{ in \%}$$

where t is exposure time in days

Thermal Cycling

- Direct co-relations can be established between % porosity and ceramic capacitance as shown below;

$$C_c \text{ (theo)} = -0.774P + 242.5 \text{ in pF}$$

$$P \text{ (theo)} = 0.2642 \exp((946.88 - C_c) / 126.12) - 56.61 \text{ in \%}$$

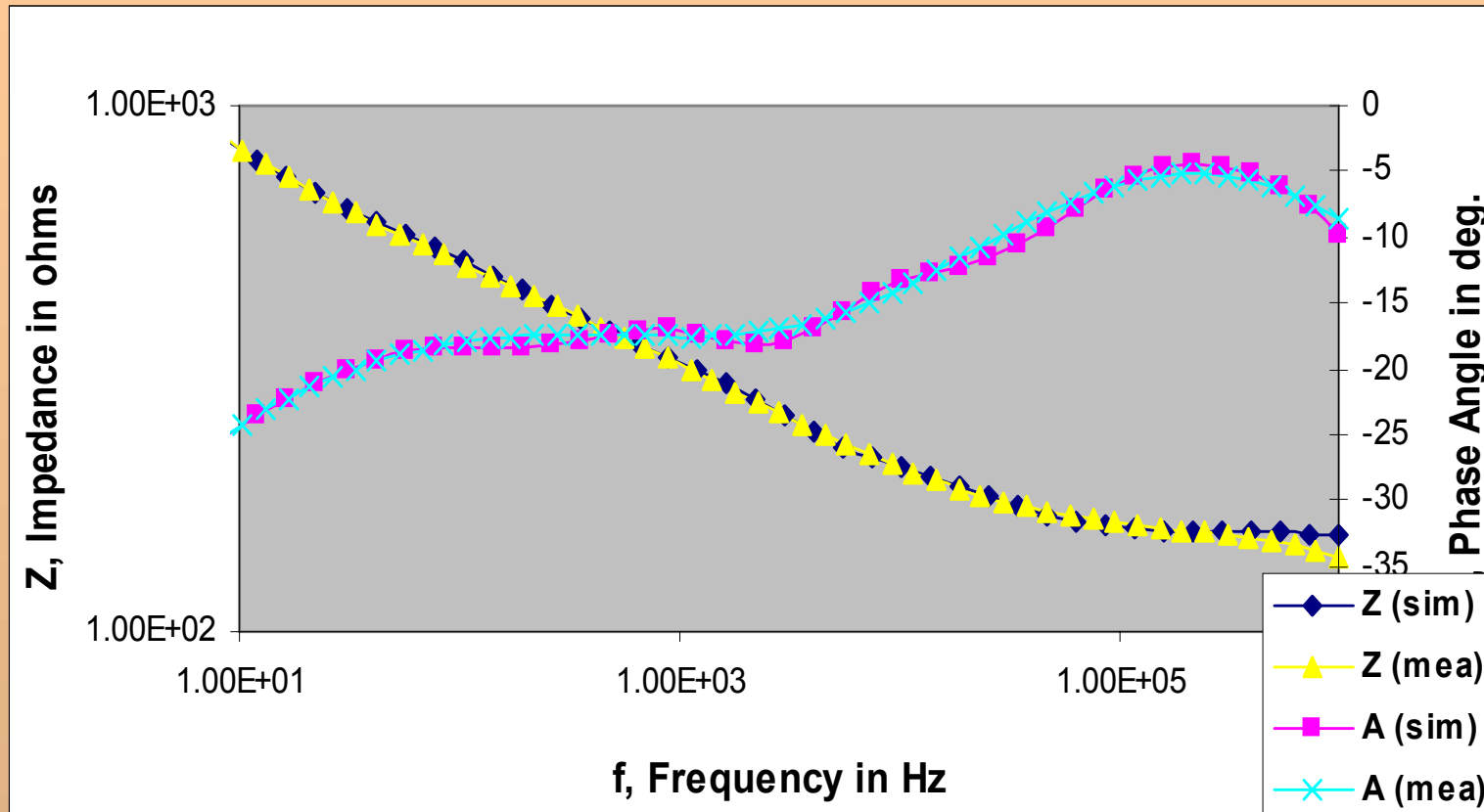
- Simple theoretical kinetic relationships can be established to correlate % porosity with ceramic capacitance as a function of time, t in days which can be modified to account for cycling frequency;

$$C_c \text{ (theo)} = (-24.706t + 70383) / (2P + 261.3) \text{ (pF)}$$

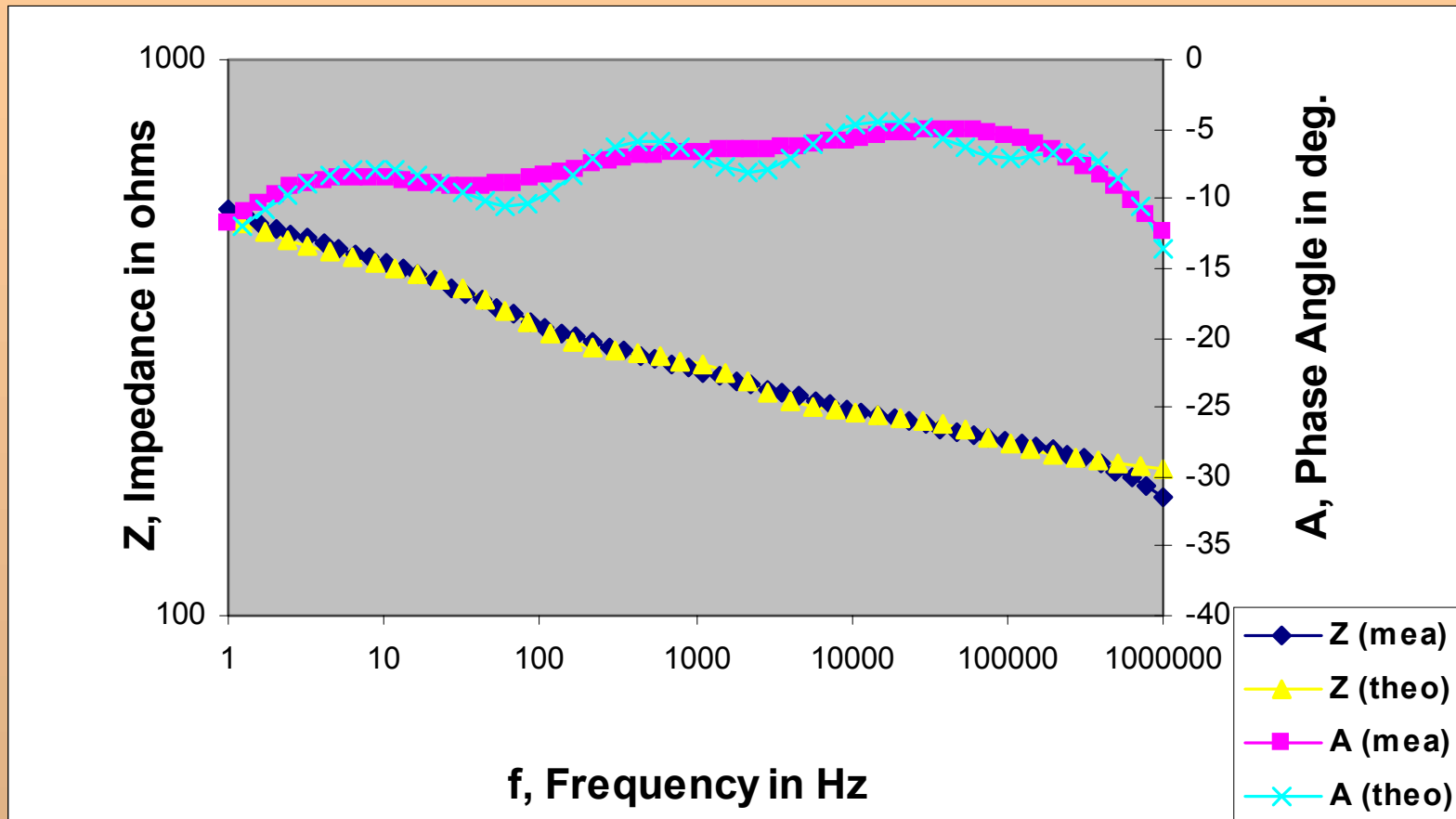
$$P \text{ (theo)} = (-12.353t + 35192) / C_c - 130.7 \text{ (\%)}$$

EIS Results for Exposed TBCs

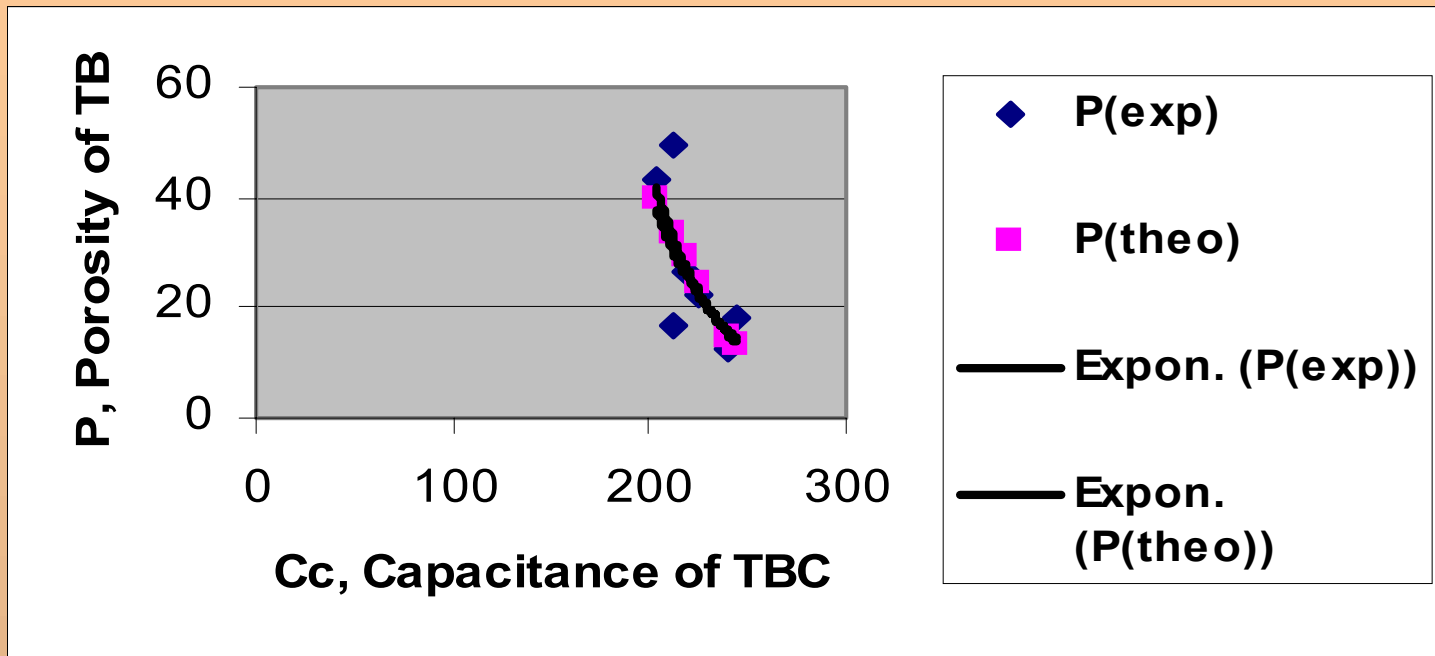
- The thickness and porosity of TBC has a linear relationship with the electrical resistance and the capacitance, respectively as obtained by EIS measurements. However, variations in coating procedures may have to be accounted for to obtain exact relationships.
- The morphological defects, viz. void, crack or delamination, can be determined by the value of pore resistance as measured by EIS.
- Isothermal oxidation generally results in a decrease in the ceramic capacitance and an increase in the ceramic resistance of TBC, while thermal cycling causes an increase in the capacitance and a decrease in the resistance. This implies that failure mode can be distinguished from the EIS data.
- The porosity of TBC exposed to oxidation and thermal cycles shows functional relationship with its capacitance.



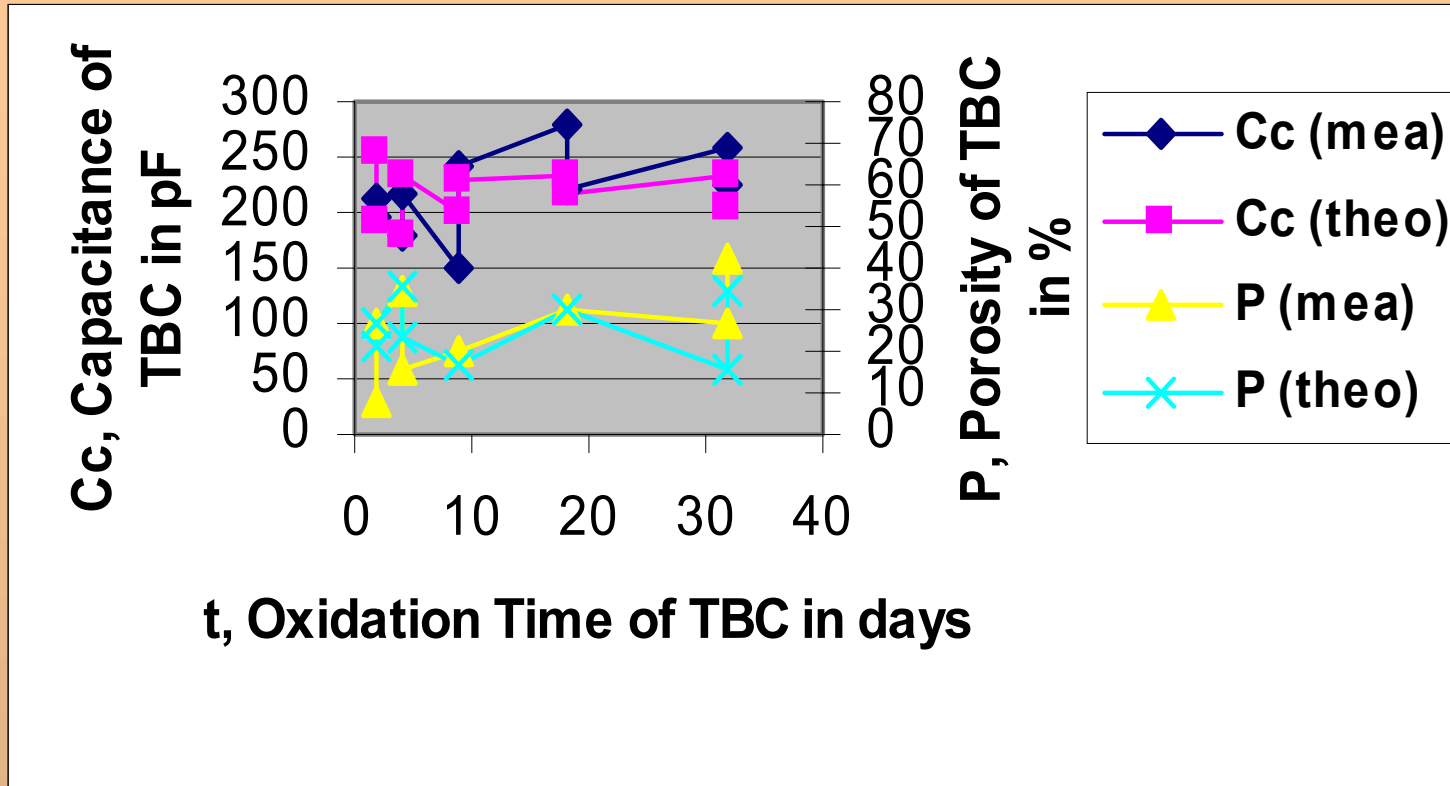
Comparison of Measured and Simulated EIS Bode Plot of a Typical TBC Exposed to Oxidation



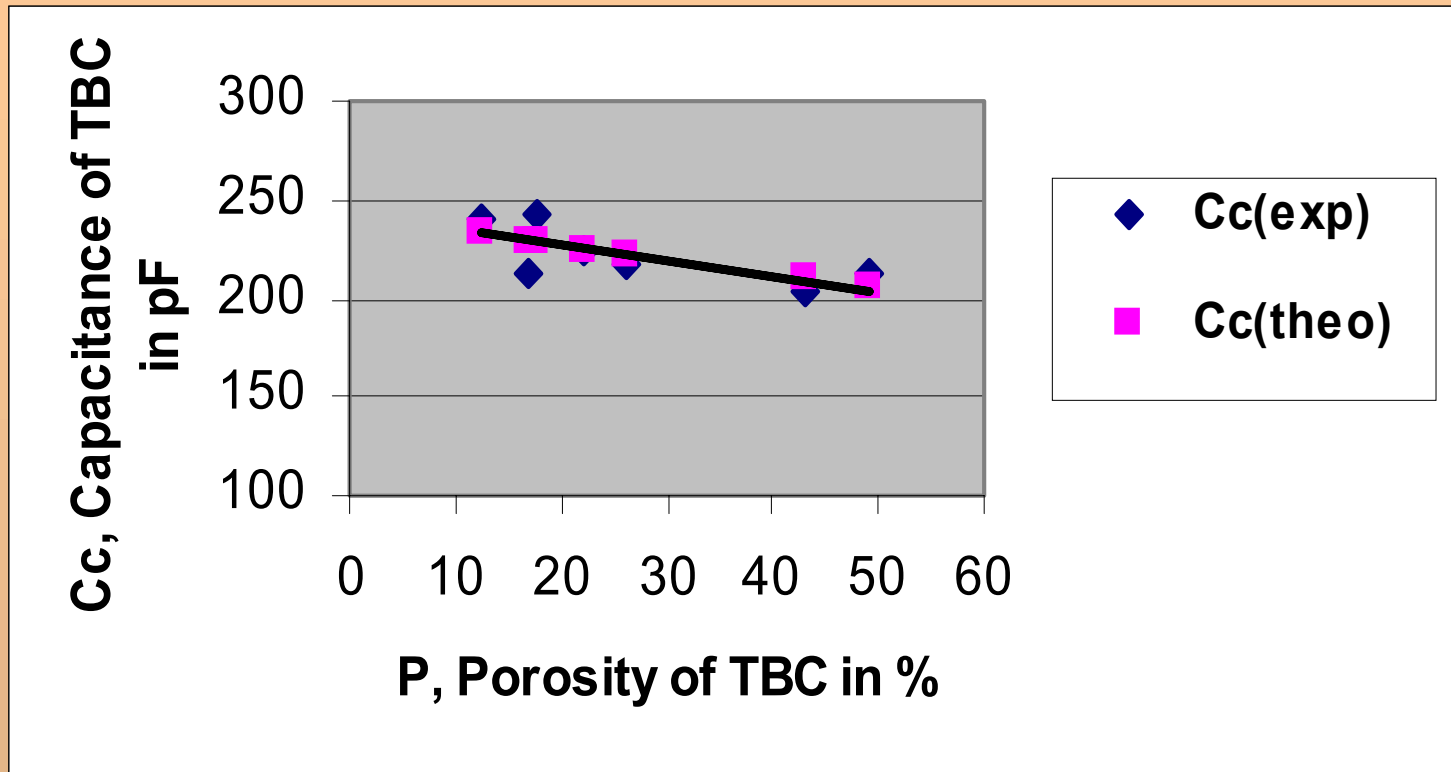
Comparison of Measured and Theoretical EIS Bode Plot of
TBCs Exposed to Thermal Cycles



Comparison of Experimental and Theoretical Porosity with Capacitance of TBCs Exposed to Thermal Cycles



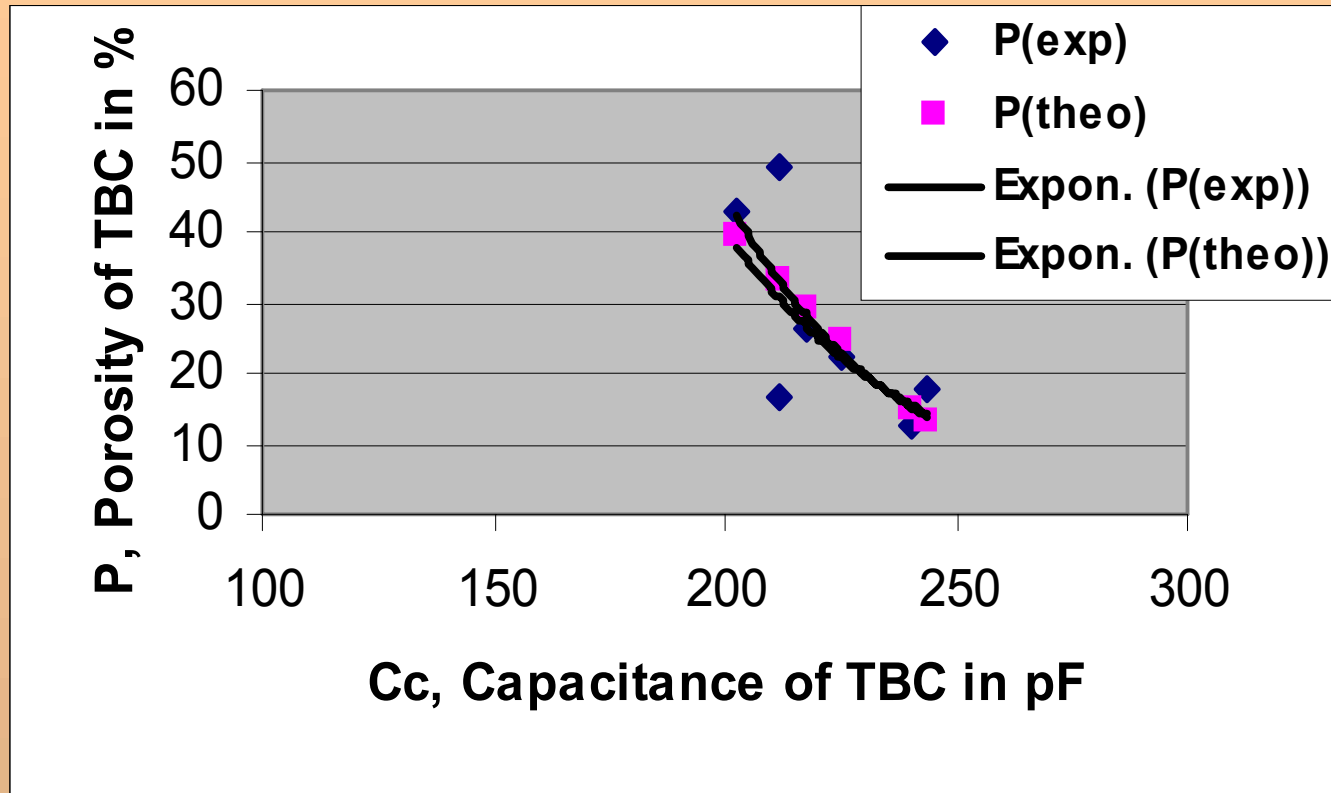
Comparison of Measured and Theoretical Cc, P and t of TBCs Exposed to Oxidation



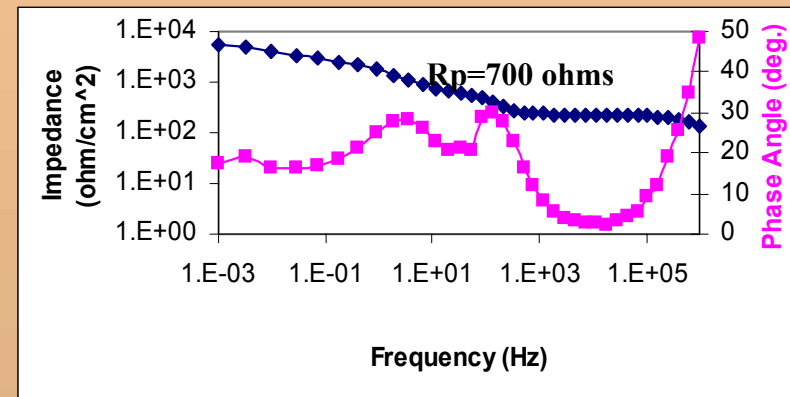
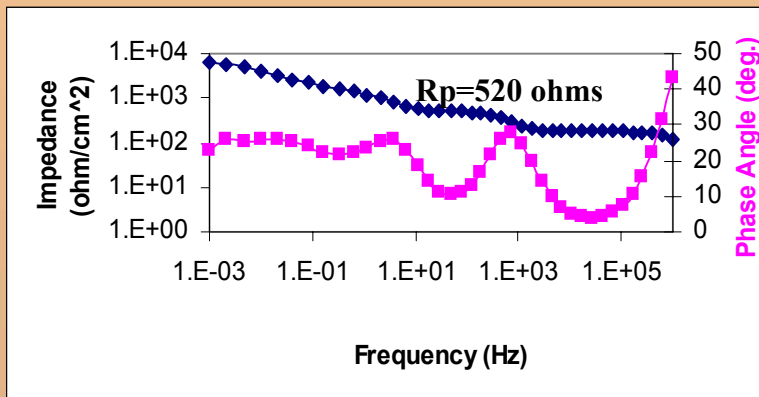
Comparison of Experimental and Theoretical Capacitance
with Porosity of TBCs Exposed to Thermal Cycles

Definition of EIS Circuit Elements

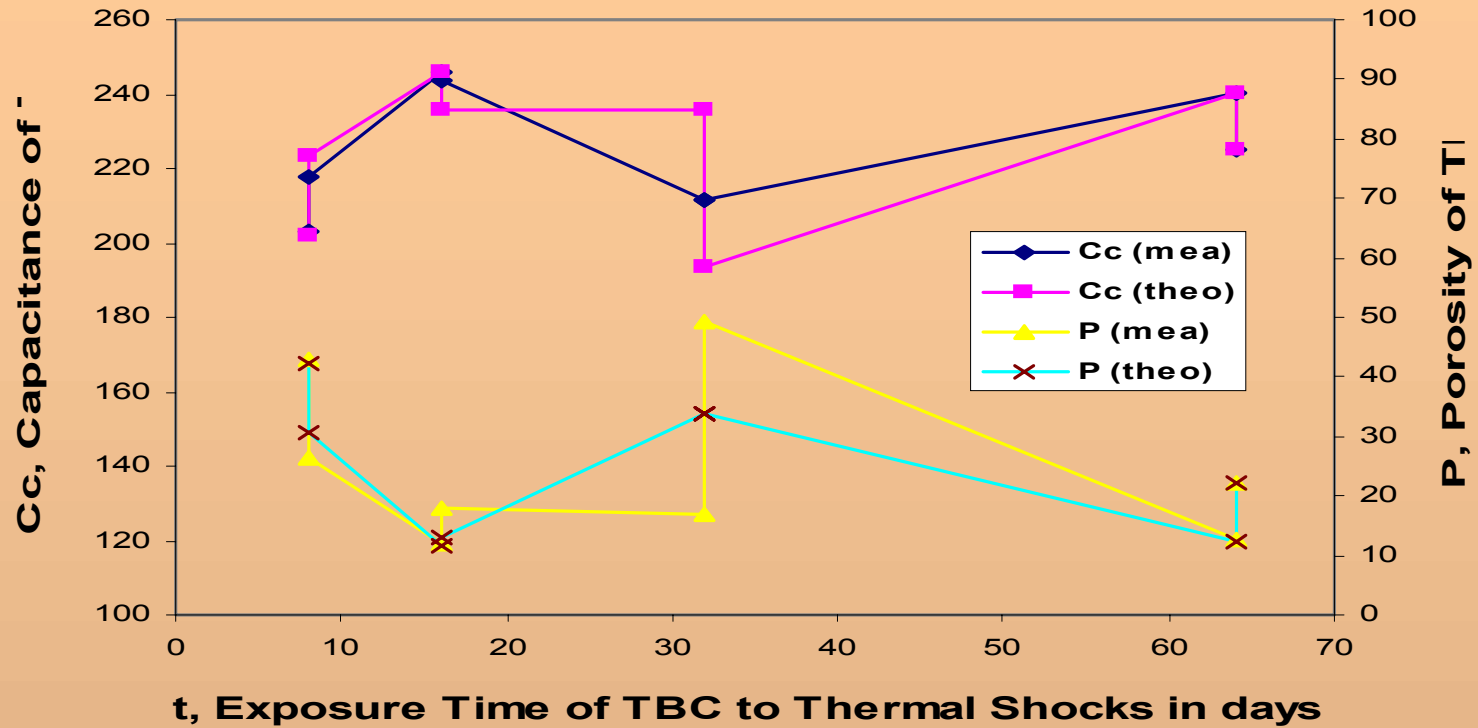
- Z** : Impedance of the system;
- R_s** : Solution resistance between the reference electrode and top coat surface;
- R_c** : Resistance of the ceramic top coat;
- C_c** : Capacitance of the ceramic top coat;
- R_p** : Summation resistance of the defects (pore resistance) in the ceramic top coat;
- C_p** : Summation capacitance of the defects (pore resistance) in the ceramic top coat;
- R_t** : Transmission resistance of the double layer at the interface between the ceramic top coat and metallic bond coat;
- C_d** : Capacitance of the double layer at the interface between the ceramic top coat and metallic bond coat;
- R_o** : Resistance of oxide layer grown on the metallic bond coat;
- W_o** : Warburg impedance in the oxide layer;
- C_o** : Capacitance of the oxide layer;
- û** : Angular frequency of the input sinusoidal wave;
- j** : sign of the imaginary part of complex.



Comparison of Experimental and Theoretical Porosity with
Capacitance of TBC Exposed to Thermal Cycles



EIS Experimental Data of a TBC with a Defect Free Top Coat ($R_p=520$ ohms) and a TBC with a Defective Top Coat ($R_p=700$ ohms)



Comparison of Measured and Theoretical Cc, P and t of TBC Exposed to Thermal Cycles

Conclusions

- 1. EIS is a powerful NDE technique for the evaluation of intact TBCs and quality assurance.**
- 2. EIS has been established as a promising technique to characterize and monitor the exposed TBC in laboratory. More work is needed to advance this technique for on engine off line monitoring of TBCs**
- 3. The thickness and porosity of intact TBCs has a linear relationship with the electrical resistance and capacitance, respectively as measured by EIS. However, variations in coating procedures may have to be accounted for to obtain exact relationships.**
- 4. The morphological defects of TBC (viz. void, crack or delamination) can be related to the pore resistance as measured by EIS.**
- 5. Porosity of TBCs exposed to oxidation and thermal cycles can be correlated to the capacitance of TBC from equivalent circuit.**

Acknowledgements

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