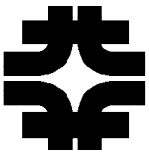

Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project

Master Clock/Trigger Supervisor Interface Adapter Card for the General System Test Module

-- VERSION 1 --

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Document # ESE-SVX- 960426

1 GENERAL INFORMATION

1.1 Introduction

This document describes the Master Clock/Trigger Supervisor Interface Adapter Card, hereafter referred as the MC/TSI adapter card. This adapter is a daughter board module that mounts on a General System Test Module (GSTM) in an SVX II Upgrade Readout Electronics System test stand. The adapter provides multiple streams of specialized command and clock signals for testing Silicon Readout Controller (SRC) boards and for use in test systems including those containing SRC boards.

1.2 Description Of MC/TSI Adapter and How It Fits Into The System

The MC/TSI adapter card is designed to operate as a daughter card to the SVX II GSTM. The GSTM is a 9U X 400mm, double width (8HP) VME board and it can accommodate up to four daughter (or mezzanine) cards. The GSTM mother board performs the common functions such as data storage, flow control and user interface required of a testing module. The daughter cards implement all of the specialized functions including the system dependent intercommunications within the target system being tested. The GSTM specifications are in a separate [1]document.

The MC/TSI adapter card simulates the presence of a CDF Master Clock source and a Trigger Supervisor when used in the testing of Silicon Readout Controller[2](SRC). Test stands for other SVX boards that include SRC boards may also need an MC/TSI adapter board to provide some of the necessary signals and signal paths. The MC/TSI adapter card occupies two adjacent daughter card slots on the GSTM, one transmitter port and one receiver port. The transmitter GSTM port will control both the Master Clock functions and the Trigger Supervisor Interface functions. These functions are described below. At least two other adapter boards are necessary to completely test all the functions of an SRC board.

1.2.1 Master Clock Section Functions

The Master clock signals provided to the SRC board by the Research Division Master Clock System or by the MC/TSI card are defined in the SRC specifications. The signals use Low Voltage Differential Signaling (LVDS) transmission standard as described in IEEE 1596 documents. The signals are:

- **CDF Clock** - the equivalent to the CDF Master system clock at approximately 53.104 MHz synchronized to the Tevetron clock. The clock frequency will vary over a small range depending on the beam energy. The clock has a 50% duty cycle.
- **SYNC** - This clock is one seventh of the CDF clock or approximately 7.6 MHz. and has a 132 ns. period and 19 ns. duration. It indicates the possible presence of a proton-antiproton

[1] "General System Test Module (Motherboard)", Mingshen Gao, Fermilab ESE Document ESE-SVX-960126
[2] "Silicon Readout Controller (SRC)", Colin Gay, John Huth, John Oliver, Maria Spiropulu, Harvard University, ESE document.

bunch crossing as only one out of seven cycles of the CDF clock is defined to contain particles. This clock is active high.

- **BX** - The bunch crossing clock has a 132 ns. or 396 ns. period depending on accelerator operating mode and position of bunch gaps. It tags the presence of a proton-antiproton bunch crossing. This clock is active high with a 19 ns. duration.
- **BZ** - The bunch zero clock has a duration of 19 ns. and occurs once every revolution of the beam in the ring or at almost a 21 microsecond period. This clock is active high.
- **Abort Gap** - The Abort Gap clock has a duration of an integral number of 132 ns. intervals and occurs during the large abort gaps in the Tevatron bunch structure. This signal will provide a measure of flexibility if the bunch structure changes from that expected for Run 2. This clock is active high.

The MC/TSI adapter board clock signals will be based on an oscillator on the GSTM board. The SRC has an internal oscillator and phase lock loop for clock synchronization. This circuitry has a center frequency of 53.103 MHz and a range of plus or minus 100 PPM or about 5 kHz. This requires that the GSTM clock be stable at a frequency between 53.098 and 53.108 MHz. The SRC also has a memory that will allow it to generate the multiphase clocks that describe the timing of the bunch structure within the Tevetron.

1.2.2 Trigger Supervisor Section Functions

The Trigger Supervisor is the master of the readout controllers within the data acquisition system. It issues commands and analyzes the status of all the readout controllers and makes system level decisions. The Trigger Supervisor section of the MC/TSI adapter will transmit control frames to the SRC using an AMD TAXI (Transparent Asynchronous Xmitter-Receiver Interface) protocol. The TAXI chip output will drive a fiber optic transmitter. The TSI commands will be stored on and read from the GSTM motherboard and sent out the TAXI link to the SRC. The MC/TSI adapter will generate a 15.15 MHz clock that will be the timing basis for the TAXI control frames transmitted from the MC/TSI board under test stand conditions. This timing will allow two command frames to be sent over the command link every **SYNC** period of 132 ns.

The TSI section must also receive four status signals returned from the SRC and buffer these signals to the GSTM. These signals will be LVDS protocol. These status signals are:

•DONE - LVDS active high output - indicates a level 2 accepted buffer transfer has completed.

•Wait - LVDS active high output - indicates the SRC cannot accept any more accepts because it is out of scan buffers in the VRB.

•ERROR - LVDS active high output - indicates a fatal error condition in or sensed by the SRC.

•L1_DONE - LVDS active high output - indicates return of a L1 accepted cell to the pipeline.

1.3 Description of Component Requirements

The MC/TSI adapter module must mount to the GSTM mother board and comply with the mechanical restrictions in the specifications for daughter cards[3]. The MC/TSI adapter module must transmit or receive signals such that it simulates the presence of two other SVX system modules. In most cases, the MC/TSI module is a signal level translator rather than being concerned with signal content. Power is supplied through the 40 pin GSTM daughter board power connectors. The following component descriptions are grouped by functional section as above.

Component requirements for Master Clock Section.

The five Master Clock signals described above must be generated based on the GSTM SYS-CLK clock. This clock comes from a crystal oscillator on the GSTM board through the port connector. The MC/TSI adapter must divide this signal twice to generate the TAXI clock and the **SYNC** clock signal. A version of the **SYNC** clock will go back to the GSTM logic for timing information. The GSTM clock will also be used to register the active edges of the four clock outputs to the SRC board. There will be variable delay circuitry in the TAXI clock and output signal latch clock in order to adjust the relative phase of these signals to meet the requirements of the SRC board or specific test requirements. The **BZ, BX,** and **Abort Gap** signals are generated as bit streams from the TX1-FIFO on the GSTM and latched on the MC/TSI card at the same time as the **SYNC** signal. The clock output levels from the MC/TSI card are LVDS. If the signal has less than 50% duty cycle, the active level is the high output from the receiver.

Component requirements for Trigger Supervisor Section.

The Trigger Supervisor section of the MC/TSI adapter will implement a fiber optic command link using an AMD Am7968 TAXI transmitter chip and an AMP 269049 Fiber Optic Transmitter. The data for the TAXI chip will come from the GSTM T[1,2]1-FIFO and the control will come from the port controller. The command link is loosely synchronous with the **SYNC** clock signal and a sample of this signal is input to the port controller. The timing of the transfer of commands words and the **BZ, BX,** and **Abort Gap** clocks will be controlled by the port controller. These signals will be synchronized with **SYNC** and the **CDF clock** on the MC/TSI board.

There are four status signals from the SRC that will be received, buffered and passed to the GSTM R[1,2]2-FIFO. The timing of the reception of these signals is controlled by the GSTM port control logic.

[3] "General System Test Module Daughter Card Design Specifications", Greg Deuerling, Fermilab Document #ESE-XXX-960311.

2 THEORY OF OPERATION AND OPERATING MODES

2.1 Basic Features & Operation

The MC/TSI adapter board is a component of the test stand required to test Silicon Readout Controller (SRC) boards for the SVX II upgrade. When an SRC is used to test other SVX hardware, an MC/TSI adapter board may also be necessary. The MC/TSI adapter board mounts on and is controlled by a GSTM board. The GSTM can contain up to four adapter cards, two defined as transmitters and two as receivers. The MC/TSI occupies two adjacent adapter positions, one transmitter, and one receiver. All data flow between the GSTM and MC/TSI adapter uses the transmitter port connection. The two paths in this connector are the DAT-T path with 27 signals out of the GSTM and the DATA-I/O path with 9 signals that, in this case are data from the MC/TSI adapter into the GSTM. Both paths have associated FIFO buffers on the GSTM board.

The SRC test stand requires more modules than a GSTM and a MC/TSI adapter card but these are the main modules that determine the design specifications for the MC/TSI module. The MC/TSI module provides signals to the SRC module under test that simulate the operational signals to and from the CDF Master Clock System and the Trigger Supervisor Interface. The GSTM to MC/TSI Adapter to SRC module relationships are represented in Fig.1. The signals are described in detail in the next sections.

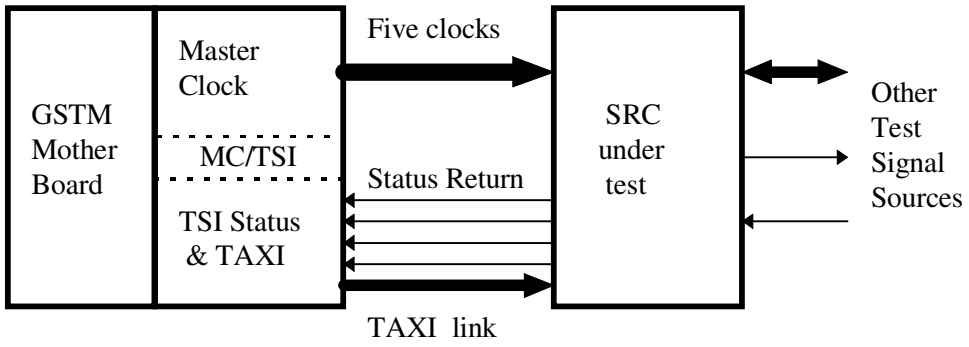


Fig.1 MC/TSI adapter connections to SRC under test

2.1.1 The Master Clock Section.

The Master Clock section of the MC/TSI module generates the five signals that are used by the SRC to provide synchronization between the Tevetron accelerator and the SVX data acquisition system. The five signals are : **CDF clock**, **SYNC**, **BZ, BX,** and **Abort Gap**. The generation of these signals is shown in the block diagram in figure 2. The signals will be LVDS outputs driven into a pair of multi-conductor twisted-pair cables through connectors on the front edge of the adapter board.

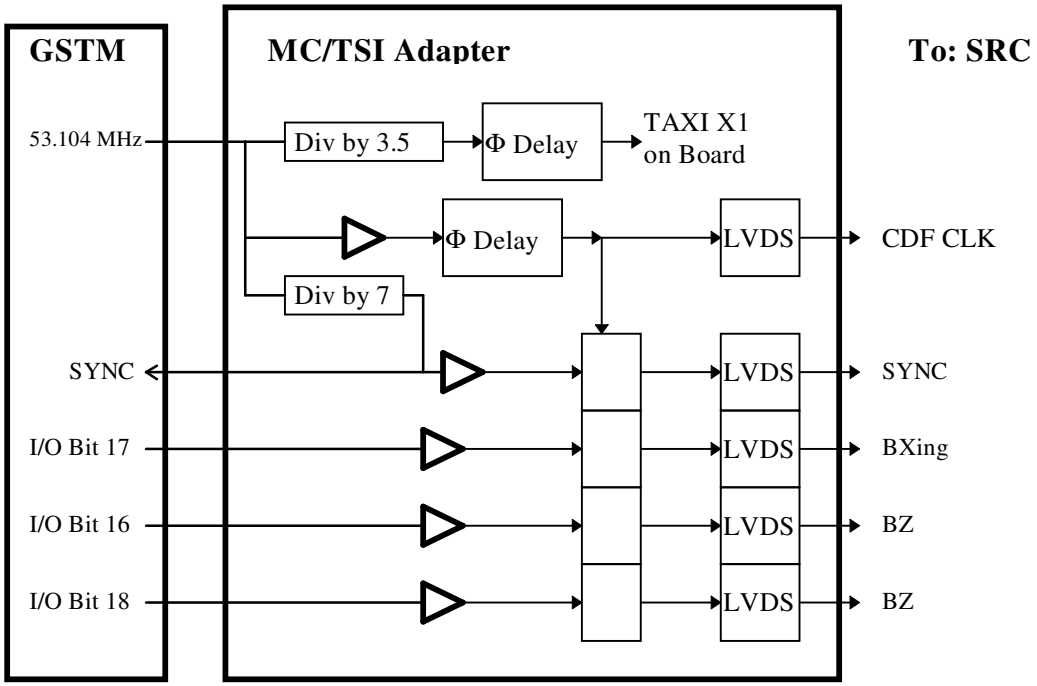


Fig. 2 Master Clock signals

- The CDF Master CLK is a very stable approximately 53.104 MHz clock upon which all the data acquisition timing is based. The MC/TSI board will phase delay the GSTM system clock to generate this signal and provide LVDS buffers to drive the SRC **CDF Clock** input. The duty cycle is 50% +- some small %.
- The **SYNC** clock will be generated by an PECL divider in the phase lock circuit creating the TAXI clock from the GSTM system clock. The divider is followed by a latch and LVDS buffers. The **SYNC** clock will also be routed back to the GSTM board to implement synchronization within the GSTM logic. **SYNC** and the **CDF Clock** will run continuously and will not be able to be disabled on the adapter card.
- The **BZ, BX,** and **Abort Gap** clocks are based on data loaded into the GSTM DAT-T FIFO which will allow a lot of flexibility in the testing of the SRC. Three of the 27 bits in the FIFO will be the data stream for these clocks. The data pattern will be loaded by the operator and buffered on the adapter card to LVDS outputs. This setup can change easily to test many different bunch structures. The DAT-T bits will also provide the command stream for the TSI TAXI link. Both of these streams are, to the first approximation, synchronous with **SYNC** and the **CDF Clock** so this is a valid constraint on the test stand. **SYNC, BZ, BX,** and **Abort Gap** are latched to be synchronous with the rising edge of **CDF Clock**.

2.1.2 The Trigger Supervisor Interface Section.

The Trigger Supervisor Interface issues commands to all the different readout control systems. The SRC board is the readout controller for the Silicon Vertex detector. The transport mechanism for this command stream is the AMD TAXI chip. It is meant to appear as a pseudo-parallel register. The TSI board generates a command stream and the TAXI hardware make it appear at the SRC. The MC/TSI adapter card TSI section must emulate a source of this stream of commands. The TSI command protocol is described in a CDF document[4]. The operation specifies two TAXI words of 9 bits every **SYNC** period or 132ns. The first word is optional and contains one of the commands, either Start Event Scan, Calibration Enable or Control. The second word is always present and contains Level 1 trigger information. This is emulated on the GSTM as bits[8:0] in the DAT-T FIFO. These words are presented to the TAXI chip MC/TSI adapter card and transmitted by a transition on one of the control lines from the GSTM. Then the next FIFO word is clocked out and the process repeated until the test is over.

The TAXI link hardware design will replicate the design on the TSI module as much as possible. Figure 3 shows the block diagram of this design. The GSTM provides twelve parallel data bits to the AMD Am7968 TAXI transmitter chip. The extra bits can change modes on the TAXI chip and will allow testing of the control link mode of the TAXI chip. An output from the port controller, P-Cntrl0, strobes the data when it is valid and an acknowledgment returns when the TAXI chip has latched the data. The TAXI chip is operating in the synchronous mode with **DSTRB** and TAXI Clock, **X1**, loosely synchronized. The details of this synchronization is described in appendix A. If there is no first word in a particular time frame, the TAXI clock still toggles without the **DSTRB** and a special frame, called a sync frame, is sent over the fiber link. Within the GSTM, the DATA-OUT-FIFO bit 25 will control the presence or absence of the **DSTRB** signal. Occasional sync frames are valuable for keeping the TAXI receiver synchronized at the byte level. The MC/TSI TAXI chip PECL outputs feed an AMP 269049 Fiber Optic Transmitter which is a self contained module including an optical launcher and ST connector for the optical fiber.

[4] "Trigger Supervisor Protocols for Run II", CDF group, Yale University, FNALD::CDF$ROOT4:[UPGRADE.RUNII_SPEC]TSI_PROTOCOLS.PS

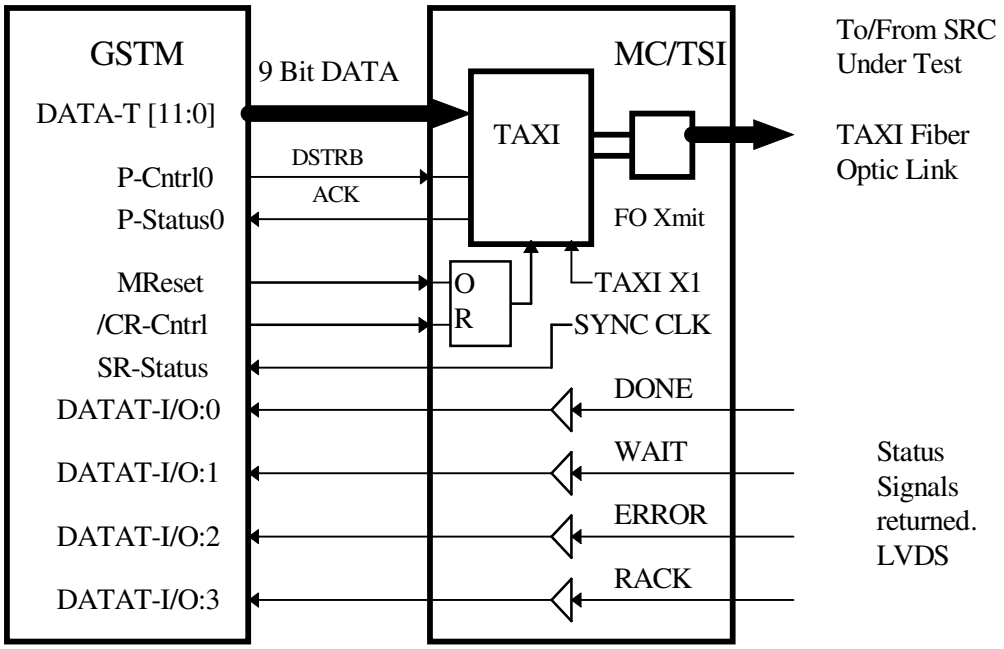


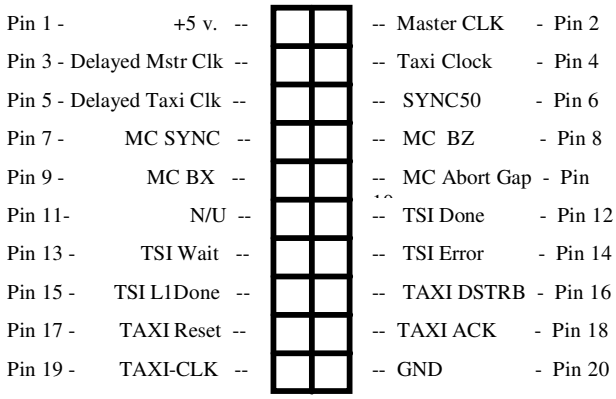
Fig. 3. Trigger Supervisor Interface Signals

The SRC also returns four status signals at LVDS levels to the TSI module. These signals will be received by the MC/TSI module and provided to the GSTM on four of the DATA-I/O lines that have been initialized as receivers. These are shown in figure 3. These four signals enter the MC/TSI adapter through a third connector on the front panel.

2.2 Diagnostic Features

Normal operation of the MC/TSI module can be generally determined by observation of the front edge LEDs. They will indicate activity on the TAXI link and three of the Master Clock signals when the GSTM is running. There is no specific diagnostic circuitry on the MC/TSI module because of the simplicity of the circuitry. The Master Clock circuitry can be tested by observing the clock outputs and creating and sending **BZ, BX,** and **Abort Gap** data from the GSTM through the MC/TSI buffers. The TSI circuitry for the status bits can also be tested by observing the input and output signals. The TAXI data link requires another GSTM daughter board with a TAXI receiver. With the second module, data can be passed through the link and compared with a copy of the source data. The MC/TSI adapter has a diagnostic connector accessible just inside the front panel on the board. Signals on the connector are diagrammed below. The connector pinout matches a standard Hewlett Packard logic analyzer pod connector.

List of diagnostic connector signals (up to 18) : **CDF Clock** and its delayed version, **SYNC19** and **SYNC50**, **TAXI CLOCK**, taxi **DSTRB**, taxi **ACK**, taxi **SYNC,** taxi **RESET, BZ, BX, Abort Gap**, TSI **DONE**, TSI **WAIT**, TSI **ERROR**, and TSI **L1DONE**.



MC/TSI Diagnostic Connector.

3 DIAGNOSTIC/DEVELOPMENT SOFTWARE

The diagnostic software for this board can be divided into two sections that depend on whether the board itself is being tested or the board is being used to test other boards. Note. The GSTM specifications describe the port connections in several ways. The following specifications will use the GSTM port connector pin assignment labels in describing the connections between the MC/TSI adapter and the GSTM. The summary of these labels is: DAT-T[0:26] are the connections to the T11 and T21 FIFO on the T1 and T2 ports. DAT-R[0:26] are the connections to the R11 nd R21 FIFO. DATA-I/O[0:8] can be configured as input or output connections on the GSTM. They can connect to GSTM FIFO buffers as follows. Port T1 : T12-FIFO-1 or R12-FIFO-1. Port R1 : T12-FIFO-2 or R12-FIFO-2. Port T2 : T22-FIFO-1 or R22-FIFO-1. Port R2 : T22-FIFO-2 or R22-FIFO-2.

3.1 Diagnostic Software to test this board.

There are three sections of the MC/TSI board to test. They are the Master Clock section, the TSI status section, and the TSI TAXI section. They are best tested separately.

3.1.1 Master Clock section.

The five clock output signals need to be verified to test this section. A data stream is created for the DAT-T FIFO containing bit stream patterns in bits 16 through 18 that correspond to the desired patterns in the **BZ, BX,** and **Abort Gap** clock outputs. The patterns are loaded into the FIFO and transferred to the MC/TSI card under the control of the GSTM port control logic. The patterns can be observed on an oscilloscope or logic analyzer using the diagnostic connector just inside the front panel. Also the **SYNC**, **BZ, BX,** and **Abort Gap** signals will be put back into the DATA-I/O FIFO inputs bits four through seven to allow self testing of just the daughter card on the GSTM.

3.1.2 TSI TAXI section.

Testing this TAXI transmitter requires a TAXI receiver. A data stream is created for the DAT-T FIFO containing bit stream patterns in bits 0 through 11 that correspond to the desired patterns to be sent. The patterns are loaded into the DAT-T FIFO and transferred to the MC/TSI card under the control of the GSTM port control logic. That sent data is compared to the data received. The TAXI port can be configured for 8 bits of data and 4 of control or nine bits of data and three of control. If the receiver can be configured similarly, these modes can be tested. The transmission of control codes should also be tested.

3.1.3 TSI status section.

This section of the MC/TSI adapter can be tested with a special external connection by using DAT-T FIFO bits that generate Master Clock signals **SYNC**, **BZ, BX,** and **Abort Gap** to supply signals to the status bits. The special cable will connect the Master Clock #2 output connector to the TSI status input connector. The pattern of the recorded status signals in the DATA-I/O FIFO is compared to the clock signal patterns loaded into the DAT-T FIFO.

3.2 Diagnostic software when this board is testing other boards.

The MC/TSI adapter functions can be divided into two categories when the board is used in a test stand and connected to other boards. These functions are input and output.

3.2.1 Input functions.

The four status inputs from the SRC are the only input data taken into the MC/TSI adapter. They are received, level translated and passed to the GSTM board. There the DATA-I/O FIFO lines should have been set-up as inputs and the incoming status bits are recorded as a stream of bits over time. The software to execute this test and analyze the recorded data will be part of the GSTM software package.

3.2.1 Output functions

The TAXI command outputs and the Master Clock outputs can be combined because the source of both is the DAT-T FIFO and both must be timed from the same time base. The **SYNC** signal from the MC/TSI adapter to the GSTM is used to establish timing for these transfers. The software to do this will be part of the GSTM software package and will include the tool to generate bit patterns in the DAT-T FIFO. An example of expected clock signals is shown in Appendix B.

4 INTERFACE SPECIFICATIONS

The MC/TSI adapter card occupies the site of two daughter boards on the GSTM (one transmitter and one receiver) and the card can be functionally be divided into two sections. One section, generates command signals to simulate commands from the Trigger Supervisor Interface to the SRC and receives status signals back. The second section generates the Master Clock signals that would normally come from the Master Clock system. The two electrical sections are combined on one printed circuit board that is designed to the two sites on the GSTM board. The adapter board has three main signal ports besides the power connector. The first is the connection to the motherboard at the transmitter site, through which the daughter card is controlled. This connection contains paths for data and control signals and is implemented by a 60 pin board-to-board interconnect. The second port is the connection to the Master clock. The five signals in this connection simulate synchronization to the accelerator beam. This port is implemented by two eight pin SDL connectors on the card front panel The third port contains the TSI signals, the fiber optic command link and the wired status returns. This port is implemented by an ST fiber optic connector and a third SDL connector for status returns. Signal directions described below are relative to the MC/TSI card.

4.1 GSTM Daughterboard Interface

The MC/TSI daughter card communicates with the GSTM mother board through a 60 pin port connector. The block diagram, figure 4, defines the interface between the GSTM mother board and the MC/TSI daughter card. The numbers shown next to the signals are the number of bits for each signal. A second smaller (40 pin) connector is used to provide the power supplies for the daughter card. The MC/TSI module may use the power connectors for both GSTM sites that it covers. This will allow a better power connections and more mechanical stability.

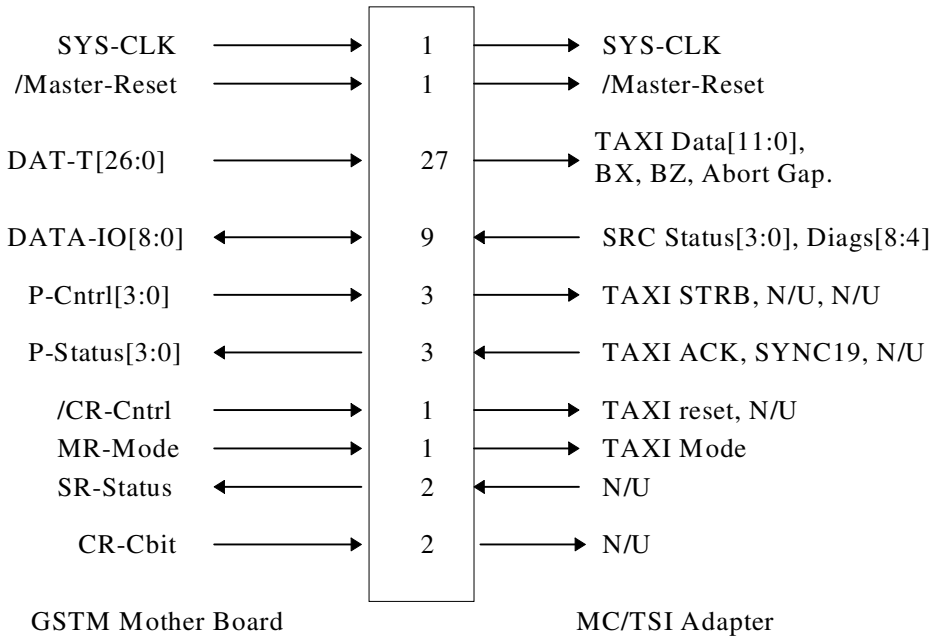


Fig. 4 Daughter Card Signals

4.1.1 Daughter Card Transmit Port Connector

The connector is a 60 pin AMP AMPMODU System 50 connector, part number 104068-2. It is a female style to mate with the male style on the GSTM card transmitter port. The receive ports have female data connectors to prevent incompatible connections. Note that this interface connector only contains pins that tie to the GND or pins that carry signals. Additional details and specifications for the signals can be found in the GSTM and GSTM daughter card specifications. The signals are marked as inputs or outputs relative to the adapter card. Input signals come from the GSTM board to the adapter.

4.1.1.2 Daughter Card Data Connector Pin Configuration

		GND	1 31	GND		
TAXI data0	I	DAT-T 0	2 32	DATA-IO-0	O	SRC DONE
TAXI data1	I	DAT-T 1	3 33	DATA-IO-1	O	SRC WAIT
TAXI data2	I	DAT-T 2	4 34	DATA-IO-2	O	SRC Error
TAXI data3	I	DAT-T 3	5 35	DATA-IO-3	O	SRC L1_Done
TAXI data4	I	DAT-T 4	6 36	DATA-IO-4	O	Diag Taxi Clk
TAXI data5	I	DAT-T 5	7 37	DATA-IO-5	O	Diag Sync19
		GND	8 38	GND		
TAXI data6	I	DAT-T 6	9 39	DATA-IO-6	O	Diag BX
TAXI data7	I	DAT-T 7	10 40	DATA-IO-7	O	Diag BZ
TAXI data8	I	DAT-T 8	11 41	DATA-IO-8	O	Diag Abrt Gap
TAXI data9	I	DAT-T 9	12 42	P-Status-0	O	TAXI ACK
TAXI data10	I	DAT-T 10	13 43	P-Status-1	O	SYNC50
TAXI data11	I	DAT-T 11	14 44	P-Status-2	O	N/U
		GND	15 45	GND		
N/U	I	DAT-T 12	16 46	SR-Status-0	O	N/U
N/U	I	DAT-T 13	17 47	SR-Status-1	O	N/U
N/U	I	DAT-T 14	18 48	/CR-Cntrl	I	TAXI reset
N/U	I	DAT-T 15	19 49	MR-Mode	I	TAXI Mode
BX	I	DAT-T 16	20 50	P-Cntrl-0	I	TAXI STRB
BZ	I	DAT-T 17	21 51	P-Cntrl-1	I	N/U
		GND	22 52	GND		
AbortGap	I	DAT-T 18	23 53	P-Cntrl-2	I	N/U
N/U	I	DAT-T 19	24 54	CR-Cbit0	I	TAXI reset
N/U	I	DAT-T 20	25 55	CR-Cbit1	I	N/U
N/U	I	DAT-T 21	26 56	SYS-CLK	I	SYS-CLK
N/U	I	DAT-T 22	27 57	/Master-Reset	I	/Master-Reset
N/U	I	DAT-T 23	28 58	DAT-T 26	I	N/U
N/U	I	DAT-T 24	29 59	DAT-T 25	I	N/U
		GND	30 60	GND		

Daughter Card Data Connector

4.1.1.1 Daughter Card Data Connector Signal Descriptions

All of the connections are discussed here, either with a description of the signal or by identifying it connection as not used. The signal directions are relative to the daughter board

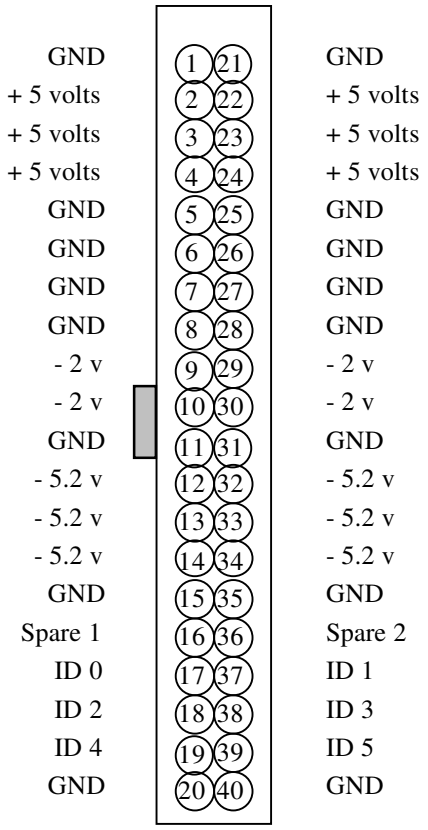
- DAT-T [11:0] in - TTL positive logic - Command and data words to TAXI link will occupy these bits. There are enough bits to utilize any protocol the TAXI chip will generate.

- DAT-T [18:16] in - TTL positive logic - These will create the bunch clock streams **BZ, BX,** and **Abort Gap**.
- DAT-T [15:12] [26:19] in - TTL - These are not used.
- DATA-I/O bits [3:0] outputs - TTL positive logic - These will be the status lines from the SRC.
- DATA-I/O bits [8:4] outputs - TTL positive logic - These will be samples of signals on the daughter boards to be used as diagnostic signals back to the mother board. The sampled signals are **BZ, BX, Abort Gap**, **SYNC,** and the TAXI clock outputs.
- SYS-CLK in - TTL - System clock 53.104 MHz from motherboard, 50% duty cycle.
- /Master Reset in - TTL active low - Reset signal to all the resetable circuitry on the board.
- P-Cntrl-0 in - TTL active high - Is the **DSTRB** signal to the TAXI chip when the GSTM DAT-T [11:0] bits are valid. The rising edge latches the TAXI latch. When there is no command in the command time slot this control signal will be missing and that will cause the TAXI transmitter to send a synchronization packet. DAT-T-FIFO [25] will be the basis for this signal but this bit 25 will not be present on the MC/TSI adapter.
- P-Cntrl-1 and 2 in - TTL active high - These signals are not used.
- P-Status-0 out - TTL active high - This will be the **ACK** signal back from the TAXI chip after a DSTRB indicating that the input latch is available for data. **DSTRB** must remain asserted until **ACK** is asserted.
- P-Status-1 out -TTL active high - Will be a sample of the **SYNC** clock from the clock divider to provide the GSTM port logic with synchronization information.
- P-Status-2 out -TTL - This signal is not used.
- SR-Status-0 and -1 out -TTL - This signal is not used.
- MR-Mode in - TTL active high - Will connect to the DMS pin on the TAXI chip and switch the data mode. Low sets the mode to eight bits of data plus four bits of command. High (normal) sets nine bits of data plus three bits of command. If this line is not asserted but left high impedance, it will select a third unused mode. This line must be either asserted high or low.
- CR-Cbit0 in - TTL active low - can directly reset the TAXI chip. The TAXI reset is the logical OR of this line with /Master Reset.
- CR-Cntrl, and CR-Cbit1 are unused.

4.1.2 Daughter Card Power Connector

The connector is a 40 pin AMP AMPMODU System 50 connector, part number 104078-2. It is a female style to mate with the male style on the GSTM card. The daughter card will be equipped with power connectors for both daughter card sites to allow better grounding and mechanical strength. The power connector on the receiver site will only have ground connections. Additional details and specifications on the power connections can be found in the GSTM and GSTM daughter card specifications.

4.1.2.1 Daughter Card Power Connector Pin Configuration



4.1.2.2 Daughter Card Power Connector Signal Descriptions

The power available to daughter cards from the GSTM mother board through the power connector are:

- + 5 volts. Digital supply voltage.
- - 5.2 volts ECL digital logic supply. Limited to 7 watts.

The total power dissipation on the MC/TSI card is limited to 20 watts.

The GSTM also expects to read an identification word on the six ID pins. The ID value is unique for each GSTM daughter card. The MC/TSI ID value is 000010 or 0x02 and the ID bits will be hard wired to this code.

4.2 Front Panel Area I/O -- Master Clock

The bottom half of the front panel area will contain the two master clock connectors for the clock signals to the SRC and four LEDs as shown in figure 5. The LEDs will indicate activity on the **SYNC**, **BZ, BX,** and **Abort Gap** Master Clock signal lines.

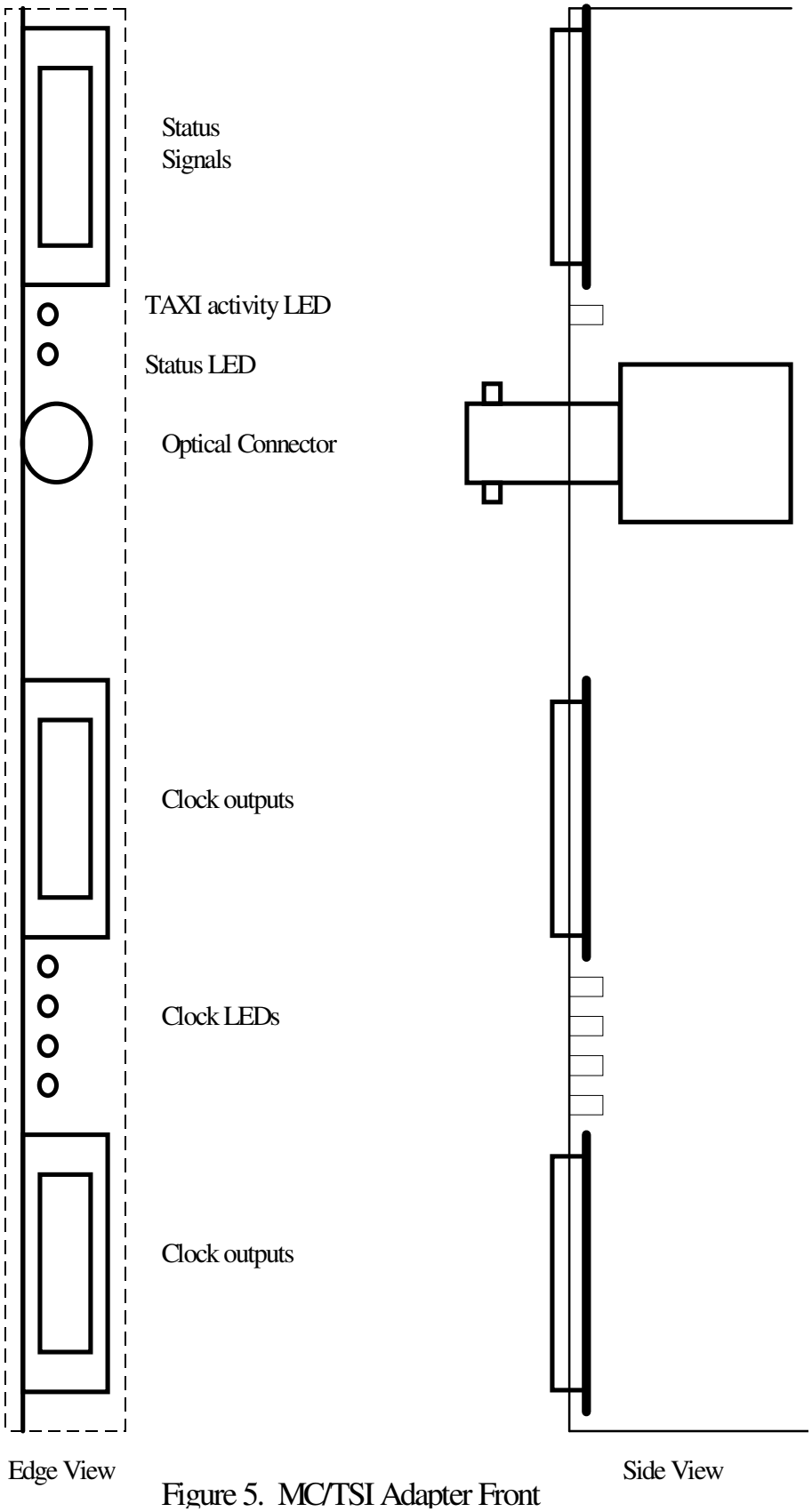


Figure 5. MC/TSI Adapter Front

4.2.1 Master Clock Connector

The Master Clock outputs will two connectors. They will be 8 pin shrouded right-angle style connectors that are mounted to the adapter card and accessible through the front panel. The part is an AMP SDL PN 1-520459-3 with C and E keys to prevent misconnection to the other connectors..

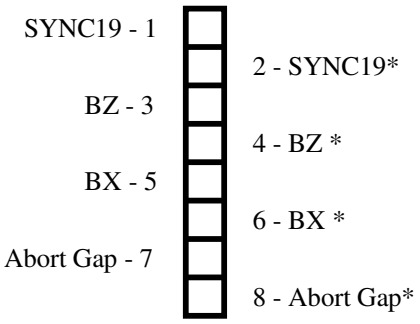
4.2.1.1 Signal Descriptions - Both Connectors

These will be outputs from the MC/TSI board that will simulate a connection to the CDF Master Clock. All clock signals are high for 19 ns. with variable periods at ground level.

- **CDF Clock** output - LVDS - Master clock at 53.104 MHz 50% duty cycle.
- **SYNC** output - LVDS active high output - Indicates bunch crossing positions possibly containing particles. Duration of 19 ns. Master clock divided by seven. Almost 7.6 MHz.
- **BZ** output - LVDS active high output - First bunch of one revolution of 1113 bunch positions in the accelerator ring.
- **BX** output - LVDS active high output - Bunch crossings that really contain particles. The pattern is under discussion but should include gaps that will allow calibration and abort recovery.
- **Abort Gap** - The Abort Gap clock has an expected duration of eleven bunch periods of 132 ns. and occurs with a pattern defined in the Tevatron bunch structure. This clock is active high.

4.2.1.2 Master Clock Connector #1 Pin Configuration

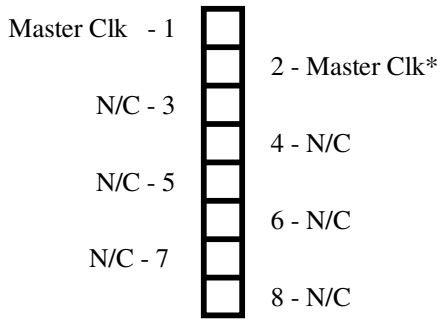
The signals are differential pairs. The starred pins are the inverted output. This connector has a ‘C’ key.



MC/TSI Master Clock Connector.

4.2.1.3 Master Clock Connector #2 Pin Configuration

The signals are differential pairs. The starred pins are the inverted output.. This connector has an ‘E’ key.



MC/TSI Master Clock Connector #1

4.3 Front Panel Area I/O -- TSI TAXI link and Status returns.

The upper half of the front panel area will be the TSI I/O area and will contain two connectors and one LED as shown in figure 5 above. There will be one fiber optic connector and one return status connector. The LED will indicate activity on the DSTRB line into the TAXI chip.

4.3.1 Fiber Optic connector

The fiber optic connector will be part of the AMP 269049-1 fiber optic transmitter module. The module will be mounted on the adapter board so that the connector is easily accessible from the front. The connector is a standard ST female fiber optic connector. There are no pin configurations and the signal is described in the technical section.

4.3.1.1 Signal Description

TAXI link output - Fiber optic - Command path from TSI to SRC. The word size is nine bits. The link can transfer two words per **SYNC** period (132 ns.)

4.3.1.1 Connector Pin Configuration

The connector is a standard ST style fiber optic connector.

4.3.2 Status Return Connector.

The Status connector will be a 8 pin shrouded right-angle style connector that is mounted to the adapter card and accessible from the front similar to the master clock connector above. The part is an AMP SDL PN 1-520459-3 with an A key to prevent misconnection to the clock signals

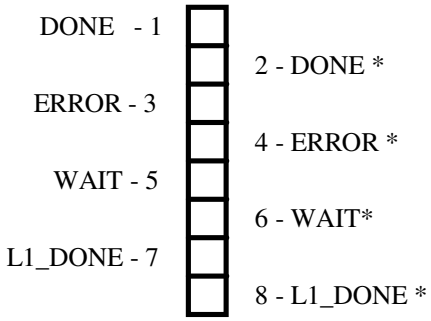
4.3.2.1 Status Signal Descriptions

- DONE input - LVDS active high output - Status from SRC to TSI indicating level 2 accepted buffer transfer has completed.

- ERROR input - LVDS active high output- Status from SRC to TSI indicating a catastrophic error condition in or sensed by the SRC.
- WAIT input - LVDS active high output - Status from SRC to TSI indicating the SRC cannot accept any more accepts because it is out of scan buffers in the VRB.
- L1_DONE input - LVDS active high output - Status from SRC to TSI indicating acknowledgment of a level 1 accept/reject.

4.3.2.2 Status Connector Pin Configuration

The signals are differential pairs. The stared pins are the inverted output. *The definition of this connector and its pin out is currently under discussion.*



MC/TSI Status Connector.

5 ELECTRICAL, MECHANICAL and SAFETY SPECIFICATIONS

5.1 Packaging & Physical Size

The board is a daughter board that plugs into the General System Test Module (GSTM). The dimensions of the MC/TSI adapter card are 6.6 inches wide and 8 inches long. The specifications of daughter boards referred to above allow three lengths for the cards. Either 6, 8, or 13 inches. The board is attached to the mother board with NUMBER 4-40 machine screws after the electrical connections are mated. The electrical connections to the GSTM mother board are 40 pin and 60 pin AMPMODU style connectors. Connections to interface cables are right-angle mounted on the MC/TSI adapter and accessible when the board is inserted into a chassis.

5.2 PC Board Construction

PC board construction techniques for high speed logic should be used on this board. The fiber transmitter to TAXI chip connections should be as short as possible. All chip power connections should be filtered and sufficient bulk filter capacitors distributed around the board.

5.3 Power Requirements

The MC/TSI daughter board requires +5 volts at approximately one amp. It will not use any -5.2 volt power.

5.4 Cooling Requirements

The cooling requirements will be supplied by the VME chassis within which the board will normally operate.

5.5 Connector Requirements

The fiber optic transmitter must be mounted on the adapter board such that a cable connector can be easily mated to the transmitter connector when the adapter is mounted on a GSTM board and while the GSTM is inserted into a VME rack. The connector must project beyond the front edge of the board so that there is no mechanical interference to this connection. The clock and status cable connectors specified have locking screws to secure the cable connector from vibration.

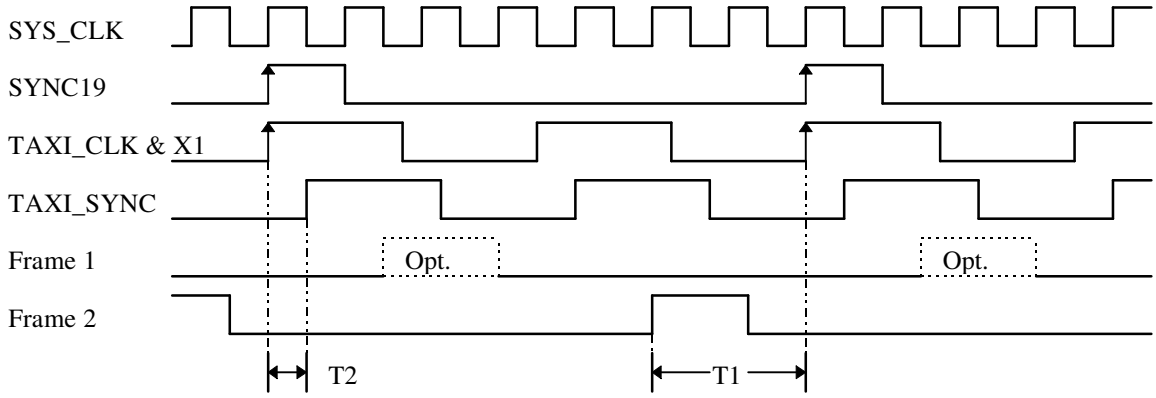
5.6 Module Fusing & Transient Suppression

The +5 volt ‘VCC’ power supply connection will be fused near the mother board power connector. On the daughter board, the power supply line is protected with transorb-diode style transient protection close to the fuse. Following that there will be a high frequency ferrite in-line filter and the bulk capacitor filter. There will be low ESR filter capacitors at each digital integrated circuit and distributed around the printed circuit board. There are special ground planes for the clock phase lock loop chip, the TAXI chip and the ODL device. They will have special connections to the board ground plane.

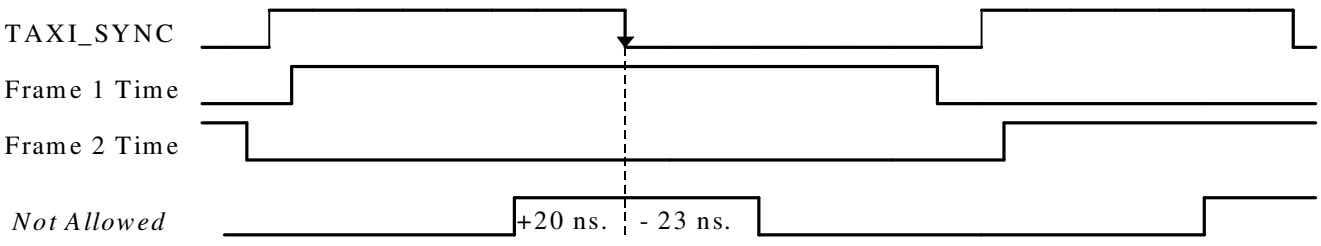
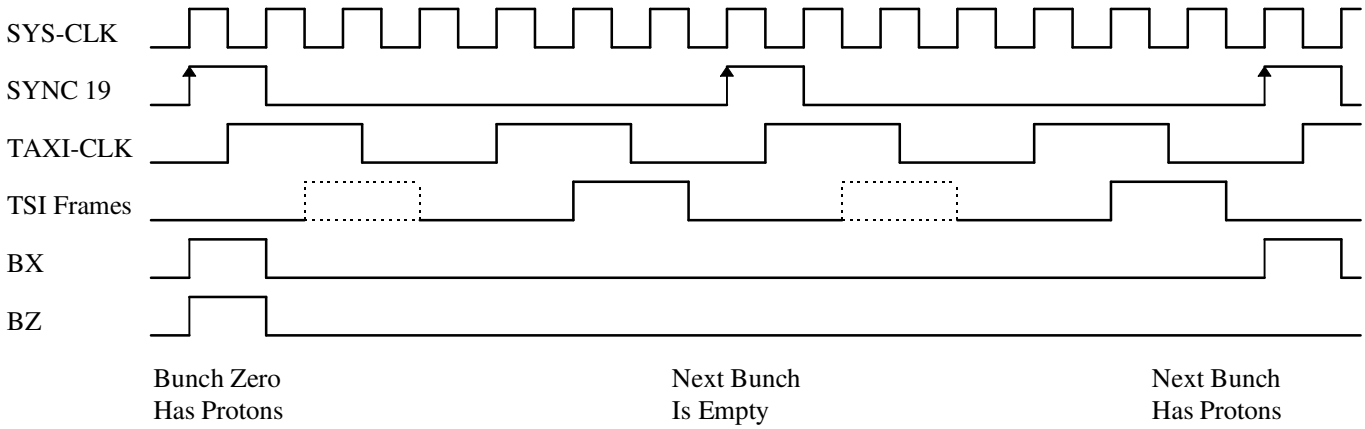
APPENDICES

A. TAXI Synchronization.

The TAXI clock and **SYNC19** are based on the 53 MHz Master Clock (SYS_CLK). **SYNC50** is an internal signal with a 50% duty cycle used to create **SYNC19** which only has a duration of 19 ns. **SYNC19** becomes the **SYNC** output from the master clock section. The TAXI chip clock **X1** must be twice the **SYNC19** rate to provide for two command frames per **SYNC** period (132 ns.). **X1** will be driven by the **TAXI-CLK** signal from the clock divider. The signal **TAXI-SYNC** is an output from the TAXI chip that can be used for synchronization. Frame 1 commands are optional but frame 2 always has level 1 information. **TAXI-CLK** and **SYNC19** may not have coincident rising edges. The SRC specifications require that the range for T1 is: 30 ns. < T1 < 122 ns. TAXI specifications require that T2 be in the range: 0 < T2 < 32 ns.



The TAXI chip transfers data internally on the falling edge of **TAXI_SYNC**. The chip should not be strobed during the *Not Allowed* window or that data may be delayed one whole cycle of **TAXI_SYNC.** *Not Allowed* extends from + 20 ns before the **TAXI_SYNC** falling edge to - 22.5 ns. after it for a **TAXI_CLK** of 15.17 MHz (53.104 MHz / 3.5). **DSTRB** is allowed any other time. **DSTRB** can occur before the rising edge of **TAXI_CLK** as long as it is after the hold time at the **TAXI_CLK** falling edge. **DSTRB** must remain asserted until **ACK** is asserted by the TAXI chip.



B. Example Clock Outputs from MC/TSI Adapter.