THE ALICE TRANSITION RADIATION DETECTOR CONTROL SYSTEM

J. Mercado* for the ALICE TRD Collaboration
Physikalisches Institut der Universität Heidelberg, D-69120 Heidelberg, Germany

Abstract

The ALICE (A Large Ion Collider Experiment) detector at the Large Hadron Collider (LHC) at CERN incorporates a transition radiation detector (TRD) designed to provide electron identification in the central barrel at momenta in excess of 1 GeV/c as well as fast (6 μs) triggering capability for high transverse momentum ($p_T > 3$ GeV/c) charged particles. It consists of 540 gas detectors (total area about 750 square meters) and about 1.2 million electronics read-out channels which are digitised during the 2 μs drift time by the front-end electronics (FEE) designed in full custom for on-detector operation.

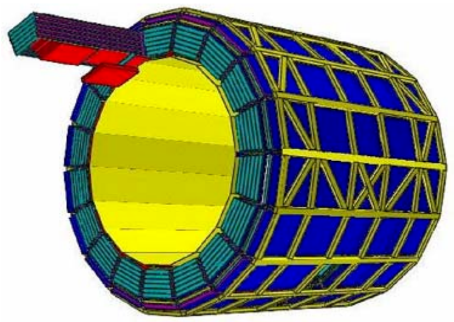

Figure 1: Schematic view of the 18 TRD supermodules showing some of the 540 drift chambers and its relative size. Both, diameter and length of the TRD, are about 7 m.

The TRD detector control system (DCS) back-end is fully implemented as a detector-oriented hierarchy of objects behaving as finite state machines (FSM) allowing for the sequencing and automation of operations. PVSS II is used in the supervisory layer. The front-end part is composed of a 3-layer software architecture with a distributed information management (DIM) server running on an embedded Linux system pool (about 550 servers) and an InterComLayer interfacing the DIM client in PVSS as well as the configuration database. The DCS also monitors and controls several hundreds of low and high voltage channels, among many other parameters.

THE ALICE TRD

The ALICE TRD will cover the kinematic region of $|\eta| \leq 0.9$ in pseudorapidity with a total of 540 individual chambers arranged in 6 radial layers which are subdivided into 18 azimuthal and 5 longitudinal sections (Fig. 1). Each detector consists of a sandwich radiator, a combination of Rohacell© and polypropylene fiber mats of 48 mm thickness; it is followed by a drift chamber with a 30 mm drift gap and a 7 mm amplification gap read out via a segmented cathode pad plane glued to a multi-layer carbon fiber honeycomb backing. The chambers are operated with a $\mathrm{Xe/CO_2}$ (85:15) mixture (total volume about 28 m^3) in order to achieve a high conversion probability for transition radiation photons [1]. The readout electronics of the 1.2 million individual pads is mounted directly on the back of the detectors. The anticipated total radiation length of all six layers of the detectors is approximately 15% X_0.

THE ALICE TRD READOUT ELECTRONICS

Beyond the 1.2 million analog channels which are digitised during the 2 μs drift time, the TRD also implements an on-line trigger which is capable of tracking most of the up to 16,000 expected charged particles within the six detector layers with a very tight time budget of 6 μs for all digitisation and processing [2].

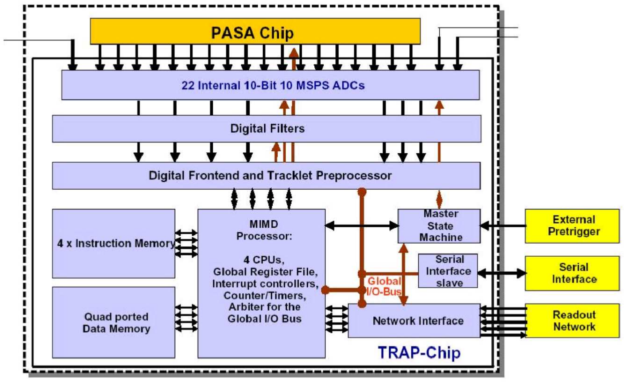

Figure 2: Architecture of the MCM building blocks.

The on-detector pads feed a charge-sensitive preamplifier (PASA) [3] whose noise is determined by its input capacity, therefore requiring its proximity to the pad planes. The preamplifier also implements first-level shaping and tail cancellation functionality. The differential PASA outputs are digitised with a custom 10-bit ADC at 10 MHz [4]. The remainder of the TRD electronics chain implements a short 64-word single event buffer plus a tracklet processor (TRAP) [5], which identifies potential high-p_T track candidates for further processing. Both chips, PASA and TRAP,

* mercado@physi.uni-heidelberg.de

are assembled in Multi-Chip Modules (MCM) which are hosted by Readout Boards (ROB) [6] that integrate power supply, DCS interface boards and optical data links.

The read-out is performed in two stages: first, during the trigger processing, where all tracklet candidates are shipped within 600 ns from the 65664 MCMs (Fig. 2) to the global tracking unit (GTU) using 1080 2.5 GBit optical links for merging of the six detector layers; second, the event buffer is read out in case the event is accepted [7].

THE ALICE TRD CONTROL SYSTEM

The primary task of the DCS is to ensure correct and safe operation of the TRD detector. It provides configuration, remote control and monitoring of all the sub-systems' equipment from a single workplace in an efficient way. In order to operate the TRD, the integration and synchronization of various sub-systems is required: low voltage (LV), high voltage (HV), front-end electronics (FEE), power control units (PCU), cooling and gas systems, among others. Some of these are briefly described in this section.

Low voltage system

Low voltage power is required by the TRD supermodule electronics (ROBs), DCS boards, PCU, GTU and pretrigger system. All together, in normal running conditions, it would amount an electrical power of more than 65 kW. For this to be accomplished, 89 water-cooled Wiener PL512/M [8] low voltage power supplies provide 224 individual channels.

These power supplies use OPC (OLE for Process Control) via ethernet as communication protocol with the supervisory layer. Each single LV channel implements more than 30 OPC items among settings, read-back values, limits and status. These are often doubled when implementing alarms and archiving schemes in the DCS.

High voltage system

The TRD readout chambers (ROC) require a potential of -2.1 kV to generate the necessary drift field and about $+1.7$ kV in order to reach sufficient gas gain. This leads to a total of 1080 HV channels needed to operate the entire detector. The specifications for each channel are demanding. For instance, the relative stability is required better than 0.1% over 24 hours while the ripple per channel is required to be smaller than 50 mV peak-to-peak.

Currently, the TRD HV system is foreseen to be operated with 32-channel Iseg EDS series modules [9] for both, drift and anodes. OPC via CAN bus is used as interface with the supervisory layer. Similar to the LV system, the amount of parameters to be controlled and monitored per HV channel by the DCS exceeds 50 when alarms and archiving is implemented.

Front-end electronics slow control

The TRD front-end electronics needs complex initialization after powering up as well as a special procedure to optimize all parameters. The TRAP chips on the detector are connected in groups of about 35 on two ROBs in redundant daisy chained networks, the slow control serial networks (SCSN). A highly universal and compact board (DCS board) was developed, incorporating an FPGA with an embedded processor capable of running Linux operating system using ethernet as network interface [10]. It serves as SCSN master and is responsible for the configuration of the TRAPs, for distributing system clock and trigger information and for enabling (disabling) the ROBs' voltage regulators.

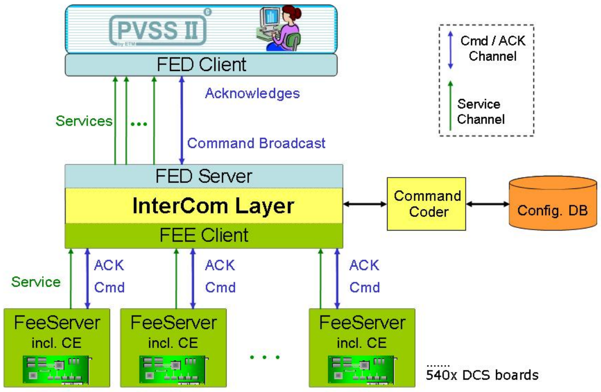

Figure 3: TRD front-end communication chain.

A 3-layer software architecture has been adopted for the FEE communication chain (Fig. 3). In the lowest level, the DCS boards run a Control Engine (CE) and a dedicated FEE server (FeeServer). The CE communicates with the underlying hardware via the SCSN, provides values to the FeeServer and processes the received commands, while the FeeServer itself takes care of the communication path and updates the published values.

The supervisory layer is implemented using the SCADA (Supervisory Control And Data Acquisition) system PVSS, which will be described in more detail later. An intermediate layer between PVSS and the on-detector software called InterComLayer, processes the instructions from PVSS, if necessary, contacts the *command coder* (interface to the actual database) and delivers data further to the FeeServers. This application runs on a dedicated control computer. For all data transfers DIM is used.

DCS IMPLEMENTATION

The TRD DCS requires hierarchical control, distribution, parallelism, partitioning and automation. In order to fulfill these requirements, all the various TRD sub-systems have been modelled as objects behaving as finite state machines using the framework State Management Interface, SMI++ [11]. For device access and description as well as alarm handling, archiving, trending, logging, access control and user interface building, the commercial SCADA system PVSS is used. PVSS is a sophisticated product that offers quite some flexibility and has been adopted as the standard SCADA system at CERN.

The TRD FSM hierarchy

A hierarchical, tree-like, model to represent the structure of the TRD detector, its sub-systems and hardware components has been developed (Fig. 4). This hierarchy allows a high degree of independence between components, for concurrent use during integration, test or commissioning phases, but it also allows integrated control, both automated and user-driven, during physics data-taking.

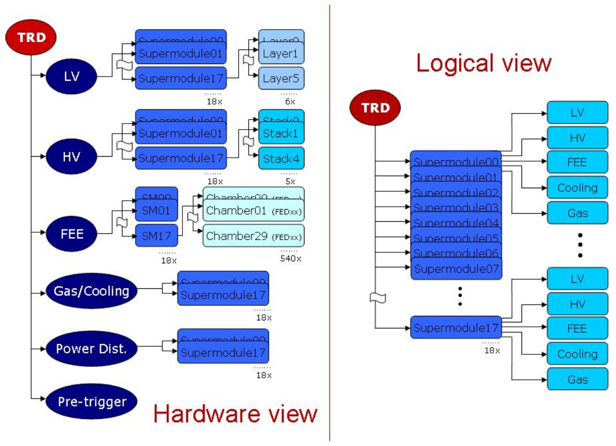

Figure 4: Sketch of the TRD FSM hierarchies (in practice, a detector-oriented hierarchy has been implemented).

The actual implementation was done by creating SMI++ classes and objects that allow for the decomposition of the whole complex TRD into smaller manageable entities. Each entity, or object (e.g. LV, HV, FEE), is described as a finite state machine modelling its behaviour in terms of simple states (off, configured, running, error, etc.) and actions (switch on, standby, recover, etc.).

These objects can be "concrete" or "abstract". Concrete objects interface with physical devices, like power supplies, DCS boards, etc. Abstract objects represent logical entities, like TRD stacks or layers. Logically related objects, for instance, all TRD LV and HV crates, can be grouped inside SMI++ "domains" representig a given subsystem, like, e.g., *Infrastructure*. A user interface can be attached to the different domains in order to view the states of their objects or to send commands to them.

DCS INTEGRATION

The control of the ALICE experiment is based on several independent "on-line systems". Each of them controls operations of a different kind and belongs to a different domain of activities: Data Acquisition (DAQ), Trigger system (TRG), High Level Trigger (HLT) and DCS.

The Experiment Control System (ECS) coordinates the operations controlled by the on-line systems and allows for independent and concurrent activities on part of the experiment by different operators. The current TRD FSM implementation has been recently integrated into ECS.

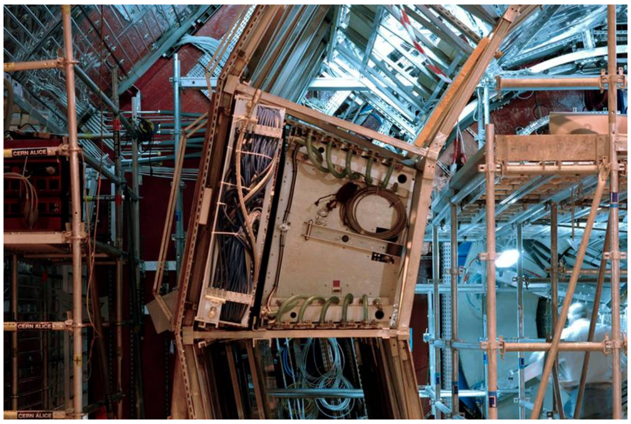

Figure 5: First TRD supermodule installed in ALICE.

SUMMARY AND PRESENT STATUS

A TRD control system based on FSM is being developed. The main FSM logical nodes for supermodules, stacks and layers are nearly finalized. All device units for LV channels, front-end devices (FED) and FeeServers are ready as well as the main FSM hierarchy. The control system is being tested with one fully equipped TRD supermodule.

On 9 October 2006, the first TRD supermodule was lowered into the ALICE cavern for final installation (Fig. 5). This fall, the second supermodule will be installed and by the end of the year, two more are scheduled.

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