Fifteenth Biennial
Single Event Effects Symposium

Final Program

Sunday, April 9

5:00 – 8:00 PM	**Registration/ Reception**	*The Foyer, Long Beach Renaissance*

Monday, April 10

7:00 – 8:30 AM	**Continental Breakfast**	*Rear, Conference Room, Renaissance*

Time	Author	Title
8:30 AM	M. Xapsos	Welcome and Local Arrangements
8:35 AM	D. McMorrow	Intro to Technical Program

INVITED TALK

8:40 AM	A. Clark L.M. Cohn	*DTRA Single Event Effects Program*

Session A: Devices and ICs I

Pascale Gouker (MIT LL) – Chair

9:10 AM	J. Benedetto P. Eaton R. Davis	Examination of Single Event Functional Interrupts (SEFIs) in COTS SDRAMs
9:30 AM	N. Haddad, T. Bach, T. Conway D. Lawson, J. Ross, J. Rodgers A. Tipton, D. Ball K. Warren R. Schrimpf	Eliminating Low LET Sensitivities in Deep Sub-Micrometer SRAM Through Non-Intrusive Technology Features
9:50 AM	C. Poivey, H. Kim, M. Vilchis J. Forney A. Phan, K. LaBel, R. Saigusa R. Finlinson A. Suvkhanov V. Hornback J. Song, J. Tung M. Miragedini	Radiation Characterization of a 0.11 μm Modified Commercial CMOS Process

10:10 AM	P. Fleming B. Bhuva W. Holman L. Massengill A. Witulski	Single-Event Effects in Switched Capacitor Amplifiers
10:30 AM	***Break***	*The Foyer*

Session B: Reconfigurable Devices Fernanda Lima-Kasensmidt – Chair

10:50 AM	M. Berg	***INVITED:*** *FPGA Design Strategies for the Space Radiation Environment*
11:30 PM	S. Rakers	Experimental Study of SEU Mitigation Measures Applied to Xilinx Virtex FPGAs
11:50 AM	***Lunch Break***	*Sicilian*

12:00 PM– 5:00 PM	**Industrial Exhibit Open**	*The Foyer*

Session B (cont'd): Reconfigurable Devices Fernanda Lima-Kasensmidt – Chair

1:00 PM	H. Quinn P. Graham J. Krone M. Caffrey J. George G. Swift	Multi-Bit Upsets in Xilinx FPGAs
1:20 PM	R. Monreal	Initial Heavy Ion Single Event Effect (SEE) Testing of the Xilinx Virtex-II Pro Multi-Gigabit Transceivers (MGT)
1:40 PM	J.J. Wang S. Rezgui N. Charest B. Cronquist J. McCollum	Aerospace Applications and Single Event Effects of Flash-Based Field Programmable Gate Arrays
2:00 PM	C. Hafer, M. Berg, R. Kim, H. Kim, R. Ladbury	High Speed Testing of the Aeroflex RadHard Eclipse FPGA
2:20 PM	G. Swift L. Edmonds	Predicting and Measuring System Error Rates for Designs Incorporating Upset Mitigation based on Triple Modular Redundancy (TMR)
2:40 PM	F. Lima Kastensmidt E. Henes Neto L. Carro G. Wirth	Evaluating SET Resilience with Duplicated Routing in SRAM-based FPGAs
3:00 PM	***Break***	*The Foyer*

Session C: Mechanisms and Modeling Lew Cohn and Anne Clark (DTRA) – Chairs

3:20 PM	V. Ferlet-Cavrois P. Paillet J. Baggio D. Lambert J. Schwank G. Vizkelethy M. Shaneyfelt D. McMorrow J. Melinger A. Campbell O. Faynoe, C. Jahan, L. Tosti	Statistical Analysis of the Charge Collected in SOI and Bulk Devices Under Heavy Ion Irradiation – Comparison with Laser Irradiation
3:40 PM	D. Fulkerson R. Carlson D. Nelson	Engineering Model for Determining Sensitive Volumes and Soft Error Rates in SOI Logic and Memory
4:00 PM	A. Balasubramanian B. Bhuva A. Sternberg S. Kalemeris L. Massengill	The Effect of Random Dopant Fluctuations (RDF) on the Radiation Hardness of Nanoscale CMOS Memory Cells
4:20 PM	E. Montes R. Reed J. Pellish M. Alles R. Schrimpf R. Weller, M. Varadharajaperumal, G. Niu A. Sutton R. Diestelhorst G. Espinel R. Krithivasan J. Comeau J. Cressler P. Marshall G. Vizelethy	Single-Event Effects Modeling in Silicon Germanium HBTs
4:40 PM	J. Pellish R. Reed M. Alles R. Schrimpf, M. Varadharajaperumal, G. Niu A. Sutton R. Diestelhorst G. Espinel R. Krithivasan J. Comeau J. Cressler	Monte Carlo Modeling of Proton Events in Deep Trench Isolation Technologies Using the Combined Capabilities of MRED and TCAD

	G. Vizkelethy P. Marshall R. Weller M. Mendenhall E. Montes	
5:00 PM	W. Chen J. Oder B. Vermeire H. Barnaby	Modeling Single Event Transients (SETs) with Linear Macro-models

6:00 – 10:00 PM	**Reception/Industrial Exhibit** – ***Foyer/Renaissance***

SEE Symposium
Tuesday, April 11

7:00 – 8:30 AM	**Continental Breakfast**	*Rear, Conference Room, Renaissance*

Session D: Testing Raoul Velazco (TIMA) – Chair

8:30 AM	G. Swift	***INVITED:*** *Tales From the Cave Part III: SEE Testing Lessons from Dickens, Scouting, and Oz*
9:00 AM	J. Howard H. Kim, M. Berg K. LaBel S. Stansberry M. Friendlich T. Irwin	Development of a Low-Cost and High-Speed Single Event Effects Tester Based on Reconfigurable Field Programmable Gate Arrays (FPGA)
9:20 AM	B. Randall S. Currie, D. Post M. Daun-Lindberg C. Burfield P. Marshall B. Gilbert E. Daniel	Packaging High Speed Circuits for Single-Event Testing
9:40 AM	M. Carts P. Marshall R. Reed S. Curie K. LaBel	Guidelines for Designing Built-In Self Test (BIST) Circuits for High-Speed IC Technologies
10:00 AM	***Break***	*The Foyer*
10:20 AM	R. Ladbury	Scaling, Packaging, and Testability

10:40 AM	M. Baze, J. Wert A. Witulski D. McMorrow J. Clement M. Hubert	Propagating SET Characterization Technique for Digital CMOS Libraries
11:00 AM	S. Buchner D. McMorrow	Future Challenges Facing Pulsed Laser SEE Testing
11:20 AM	V. Pouget D. Winn A. Douin D. Lewis P. Fouillat	Recent Developments for SEE Testing at the ATLAS Laser Facility
11:40 AM	E. Peterson	Common Problems with SEE Data Acquisition and Analysis
12:00 PM	***Lunch Break***	*Poolside (weather permitting)*

INVITED TALK

1:10 PM	L. Anghel	*Evaluation of SET and SEU Effects at Multiple Abstraction Levels*

Session E: Devices and ICs II Steve Buchner (NASA GSFC) – Chair

1:40 PM	M. Baze, J. Black J. Wert M. Hubert	Heavy Ion Test Results on 13 Shift Registers in a 130 nm Process
2:00 PM	D. Hansen, P. Chu, K. Jobe, R. Lopez-Aguado M. Shoga	Ion-Microbeam Probe of High-Speed SiGe Shift Registers for SEE Analysis
2:20 PM	T. Loveless L. Massengill B. Bhuva W. Holman Y. Boulghassoul	SEE Hardening Options of a RF Digital PLL
2 :40 PM	R. Krithivasan P. Marshall M. Nayeem A. Sutton W. Kuo B. Haugerud L. Najafizadeh J.D. Cressler M.A. Carts C.J. Marshall G. Niu, R. Reed B. Randall C. Burfield B. Gilbert	Recent Results on SEU Hardening of SiGe HBT Logic Circuits
3:00 PM	L. Massengill	***INVITED :*** *Scaling Impact on Traditional SEU Mitigation Techniques*

3:20 PM	K. LaBel M. Berg D. Black W. Robinson T. Jordan	Mystery Talk
3:40 PM	***Break***	*The Foyer*
4:00 PM	**PANEL DISCUSSION**	**SEE Testing Challenges: The Next Generation** *Panelists*: Paul Marshall, *Consultant/NASA GSFC* Robert Reed, *Vanderbilt University* Veronique Ferlet-Cavrois, *CEA* Joe Benedetto, *ATK/Mission Research* Chuck Foster, *Foster Consulting* Steve McClure, *JPL* *Moderators*: Ray Ladbury, *NASA GSFC* Steve Moss, *The Aerospace Corporation*
5:40 PM	***End of Panel Discussion***	

6:00 – 8:30 PM	**Happy Hour –** *Foyer/Renaissance*

SEE Symposium
Wednesday, April 12

7:00 – 8:30 AM	**Continental Breakfast**	*Rear, Conference Room, Renaissance*

INVITED TALK

8:30 AM	R. Reed R. Weller	*RADSAFE Development and Applications Overview*

Session F: Protons and Neutrons Jim Schwank (Sandia) – Chair

9:00 AM	J. Schwank	Single-Event Effects Testing for Proton Environments
9:20 AM	M. Liu, H. Liu E. Vogt H. Hughes P. McMarr A. Thompson	Thermal Neutron Induced Upsets in Hardened SOI SRAM
9:40 AM	J. Tausch D. Sleeter D. Radaelli H. Puchner	Microlatches in Commercial SRAM Caused by Terrestrial Neutrons

10:00 AM	***Break***	*The Foyer*
10:20 AM	M. McMahan	New Neutron Capabilities for Radiation Effects Testing at the 88-Inch Cyclotron
10:30 AM	S. Huston	Mapping the South Atlantic Anomaly

Session G: Single-Event Transients Mark Baze (Boeing) – Chair

10:50 AM	M. Savage G. Dunham J. Seiler	Single-Event Transients in a Dielectrically Isolated Bipolar IC Process
11:10 AM	C. Poivey, H. Kim, K. LaBel J. Karsh, I. Kleyner, R. Katz	Single-Event Transients in Low Voltage Dropout (LVDO) Voltage Regulators
11:30 AM	N. Varanasi W. Chen H. Barnaby	Single Event Transients (SETs) in RF Circuits
11:50 AM	C. Holt, B. Bhuva, W. Holman, L. Massengill	SETs in CMOS Dynamic Logic Circuitry
12:10 PM	D. Mavis M. Turowski P. Eaton A. Raman	Modeling and Simulation of Digital SET Pulse Generation
12:30 PM		**End of Technical Sessions**

2:30 PM ***Special Session: Volleyball by the Pier***