SSP Cable Segment Hybrid Tester

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Abstract

This note describes the design of a circuit to test SSP Cable Segment line drivers (so-called "hybrids"). Some results are presented from an examination of "bad" hybrids, removed from SSP's during past E787/E949 running.

1 Introduction

The most common failure mode on the SSP cable segment is a failure of the cable segment line driver ("hybrids"), a custom device built at KEK for the version used in E787/E949. With the demise of Fastbus throughout the HEP community, E787/E949 probably has the remaining world's supply of these devices, and there has been some concern that this supply would run out. One possibility raised many years ago was to see if we could recycle our "bad" hybrids, removed from SSP's during data-taking; the speculation was that in many of these cases, the hybrid was actually ok, and that the poor hybrid voltage measurement arose from contact problems between the hybrid and its socket or from human error during the chaos of shift-taking.

The hybrid tester described here was designed/debugged by Arnie Stillman and drawn/laid out/built by Henry Diaz. The final tweaking/debugging as well as the documentation were completed after Arnie left the lab. The documentation is based on reverse-engineering the existing board.[1]

2 Tester Design

The two logic states on the Cable Segment are shown in Fig. 1, taken from the Fastbus Spec. In the 0-state, the two legs of the hybrid supply no current, and the current on the cable segment is provided by the ancillary logic. In the 1-state, one leg sources current and the other sinks current such that the overall current across the termination resistor has the same magnitude, but reverses direction. This tester checks the full Fastbus specification for the line drivers:

- 1-state current: I = 4.0 ± 0.2mA
- 0-state current: 40μA maximum
- Current source sink match better than 1%
- Common mode range = $\pm$3.0V, minimum

These specs are tested by sensing the current produced by the hybrid, converting to a voltage and then comparing the voltage to upper/lower thresholds. The basic design is shown in Fig. 2 and 3.

The termination resistors, R, are set by the standard to be around 100Ω. The required current of 4mA (given the termination resistance and the fact that $V_T = -2V$ and $V_{EE} = -5.2V$) then

[1] The schematic that was used to produce the PC board was only partially useful due to many undocumented modifications made to the board after its production.

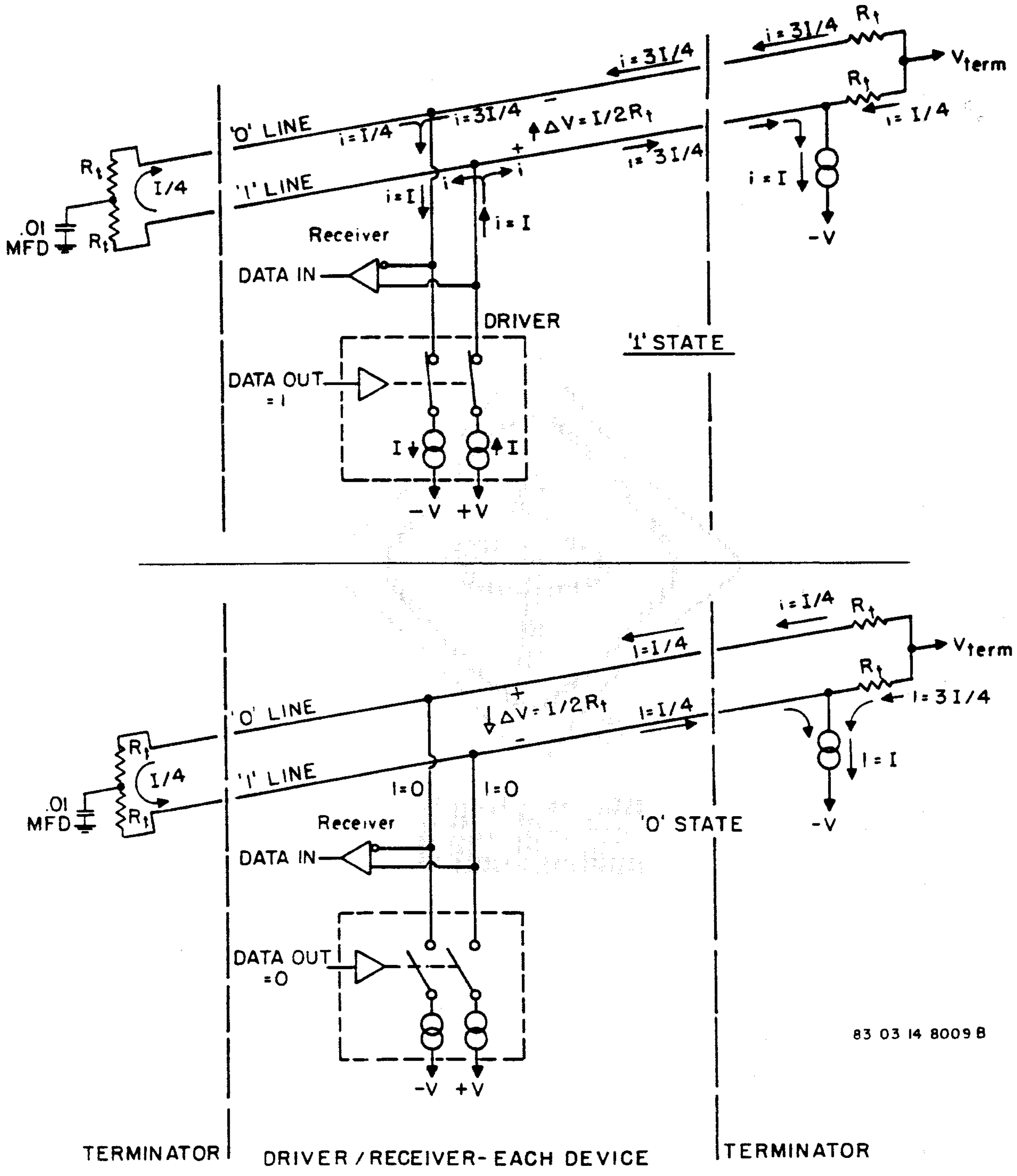

Figure C.
Cable Segment Logic States
(Values of current are based on zero wire resistance.)

Figure 1: The logic states on the Fastbus cable segment, taken from the Fastbus spec

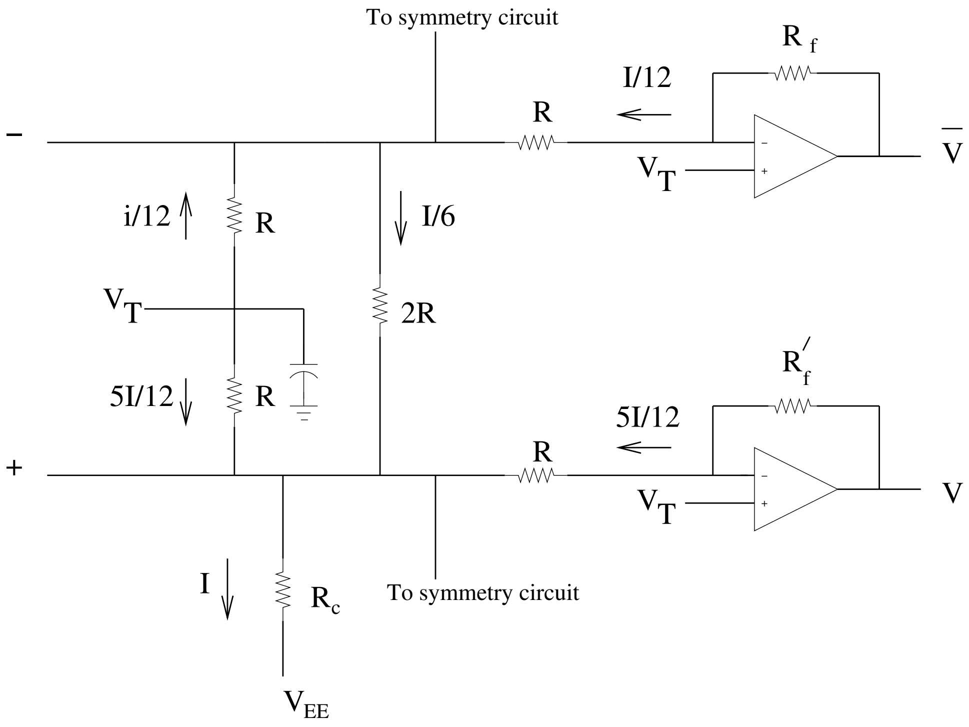

Figure 2: The hybrid test circuit in the 0-state.

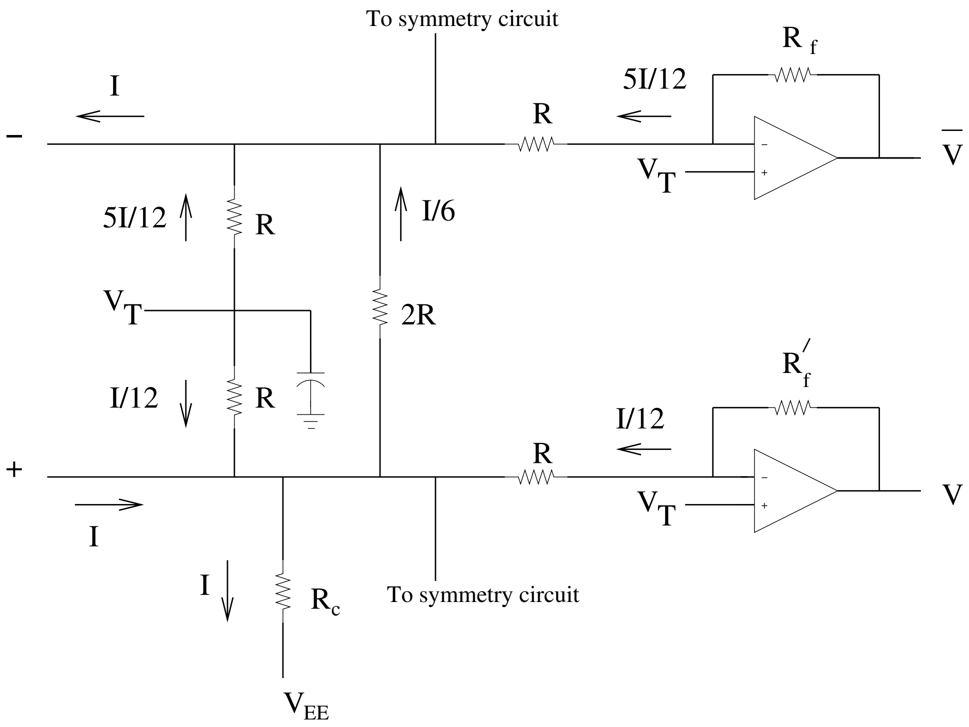

Figure 3: The hybrid test circuit in the 1-state.

channel	$\overline{V}$		V		V_{out}(symmetry)	
	1-state	0-state	1-state	0-state	1-state	0-state
1	-0.953	-0.913	-1.638	-1.697	-4.22	-4.21
2	-0.940	-0.861	-1.663	-1.705	-4.23	-4.22
3	-0.955	-0.942	-1.647	-1.698	-4.22	-4.22
4	-0.962	-0.950	-1.647	-1.701	-4.23	-4.22

Table 1: Typical voltages measured on good hybrids.

$\overline{V}$		V		V_{out}(symmetry)	
upper	lower	upper	lower	upper	lower
-0.834	-1.005	-1.527	-1.746	-4.201	-4.274

Table 2: Upper and lower threshold voltages. Hybrids with voltages between these two thresholds are accepted as "good".

sets the value of R_c. The feedback resistors (R_f and $R_f^{'}$) each have two values and are switched depending on the logic state; this keeps the output voltage from the op-amp approximately constant, and only one set of thresholds is needed for both logic states. The sensitivity to the 0-state current (nominally 0) is set by the feedback resistor; with the 0-state values $R_f \sim 2700\Omega$ and $R_f^{'} \sim 90\Omega$, we find that $\overline{V}$ changes by about 100mV for 40μA of current, while V is insensitive to such small currents.[2] For the 1-state, both R_f and $R_f^{'}$ are set to 510Ω. The symmetry circuit (not shown here; see the proper schematics attached at the end) takes the voltages from the two hybrid legs through $25k\Omega$ resistors into a unity-gain summing op-amp; the typical output voltage is around $-4V$; sensitivity at the 1% level implies being sensitive to voltage changes at the $\pm 40mV$ level.

It turned out to be too difficult to set the threshold values based on pure calculation. Presumably this is due to small differences in resistor values and to op-amp input currents, but I was not able to confirm this with Arnie. We decided instead to calibrate the tester (in the 1-state) using known good hybrids; the 0-state (0 current) is easy since one just removes the hybrid from the tester. The results of the measurements are shown in Table 1. The spread in the voltage readings, sampling a handful of hybrids, was very small, typically a few mV. The 0-state measurements of $\overline{V}$ and V were found to be very close to the values seen with no hybrid in the test circuit, indicating that the typical hybrid 0-state current is very close to 0.

Based on the measurements in Table 1, the thresholds were set as shown in Table 2. The hybrid tester tests all 4 channels at the same time. LED's indicate whether or not the hybrid channel passed the test and if not, a separate set of LED's indicates which test the channel failed.

3 Results

Over the years we have accumulated about 140 bad hybrids. 36 of those were examined with this tester. 29 were found to pass. As a further check, 14 of those 29 were put into an SSP. No problems were found with this SSP when it was subjected to all the standard cable segment tests. This suggests that the tester is working properly. It also suggests that hybrids should be in good supply for future running.

[2] It is not clear to me why $R_f^{'}$ was not chosen to give more sensitivity.

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