



Large Area GTO Thyristor Development

Ranbir Singh
ranbir.singh@genesicsemi.com
GeneSiC Semiconductor Inc.
43670 Trade Center Place
Suite 155, Dulles VA 20166
703-996-8200 (ph)





Outline

- Rationale for Silicon Carbide for Utility Power
- Goals for SBIR Program
- 2D Device Simulations
- Layout Design
- Conclusions & Next Steps

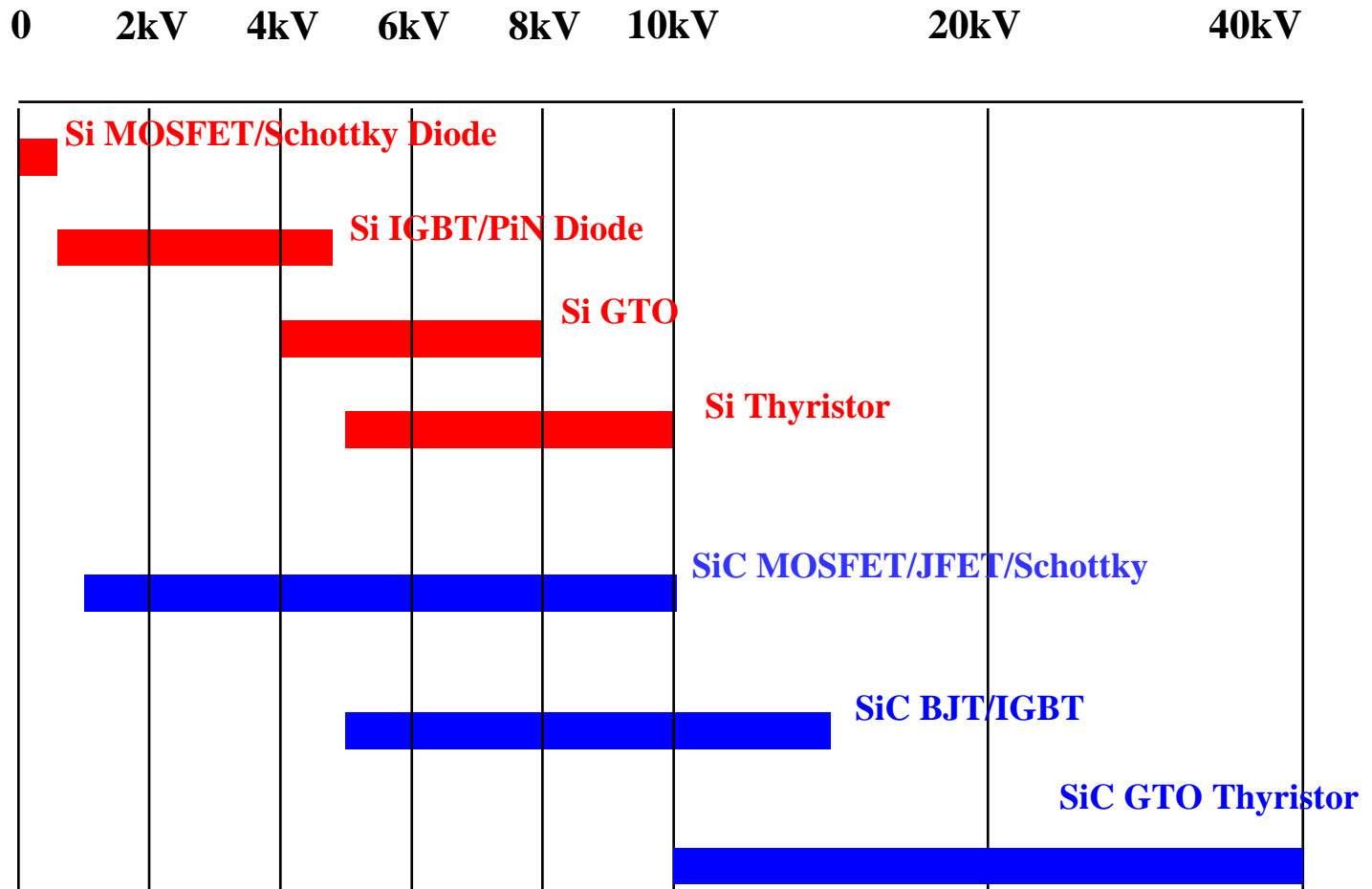


Why Silicon Carbide Power Devices?

- FY07 Phase I SBIR from DoE Started Jul 07
- Design of >10kV, 20 KHz switch

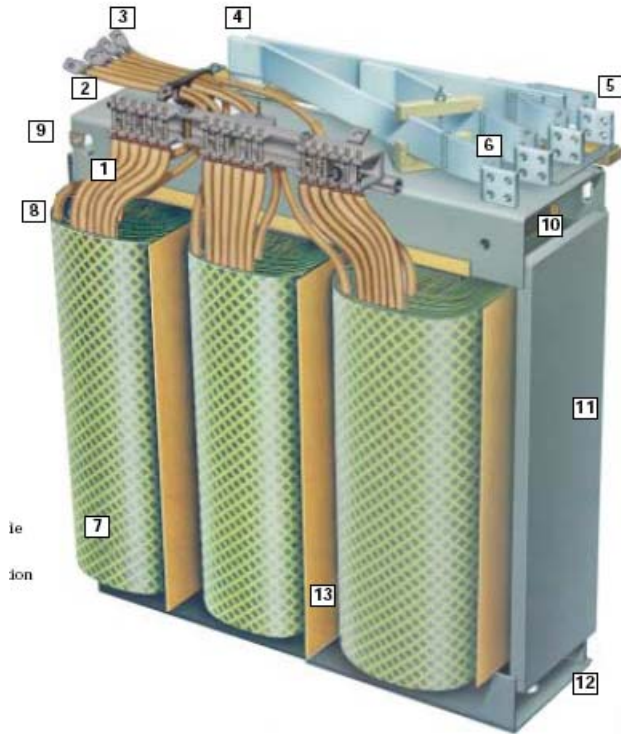
Lower On-state Voltage drop for 5-20 kV Devices (2-3X than Si)	Higher Efficiency of circuits
Faster switching speeds (100-1000X smaller turn-off times)	Smaller inductors, capacitors; Compact circuits
Higher Chip temperatures (250-300°C instead of 125°C)	Smaller packages, Smaller thermal management mass
Higher Thermal Conductivity (3.3-4.5 W/cmK vs 1.5 W/cmK) Widebandgap (10^{16} X smaller n_i)	Higher pulsed power, Higher continuous current densities

Applicability of Power Devices



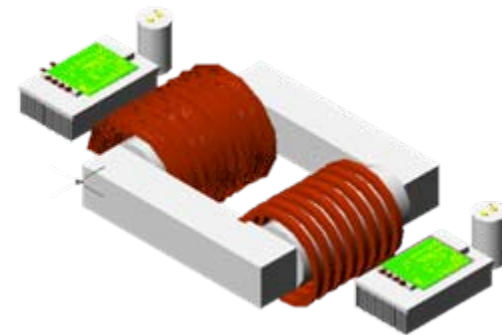
Size and Weight advantages for Naval SST

Conventional 2.7 MVA transformer



Size: 10 m^3

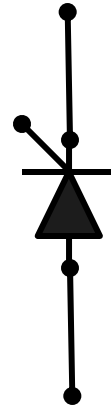
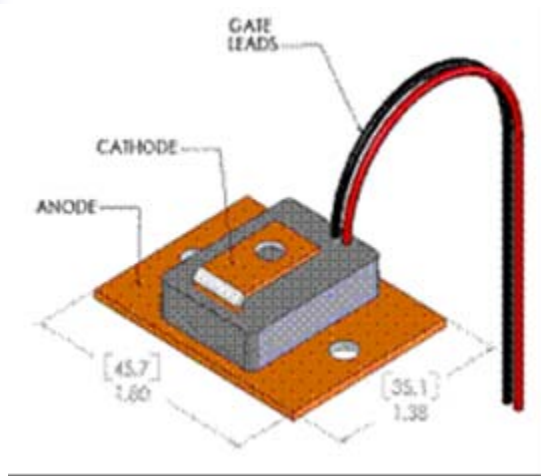
2.7 MVA Solid-state transformer



Estimated Size: 3.4 m^3

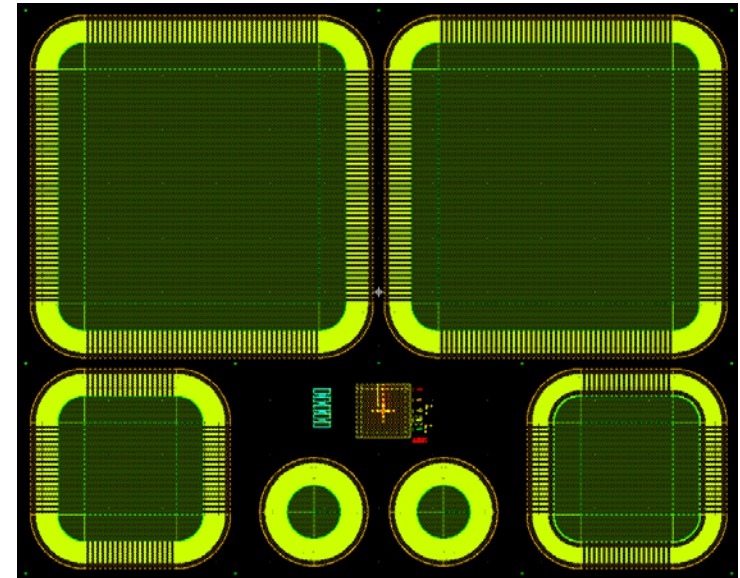
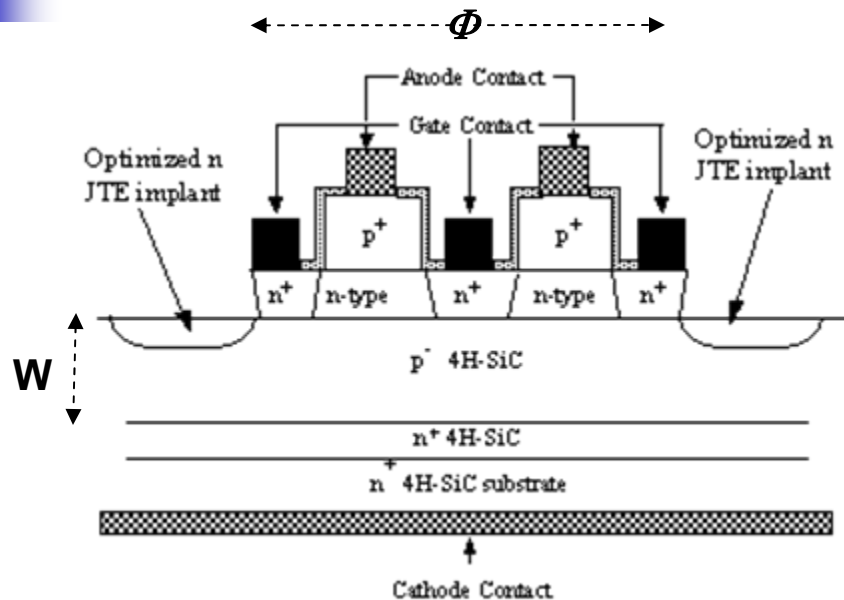
Courtesy: Prof. Alex Huang

Goals: Specifications for Devices/Modules



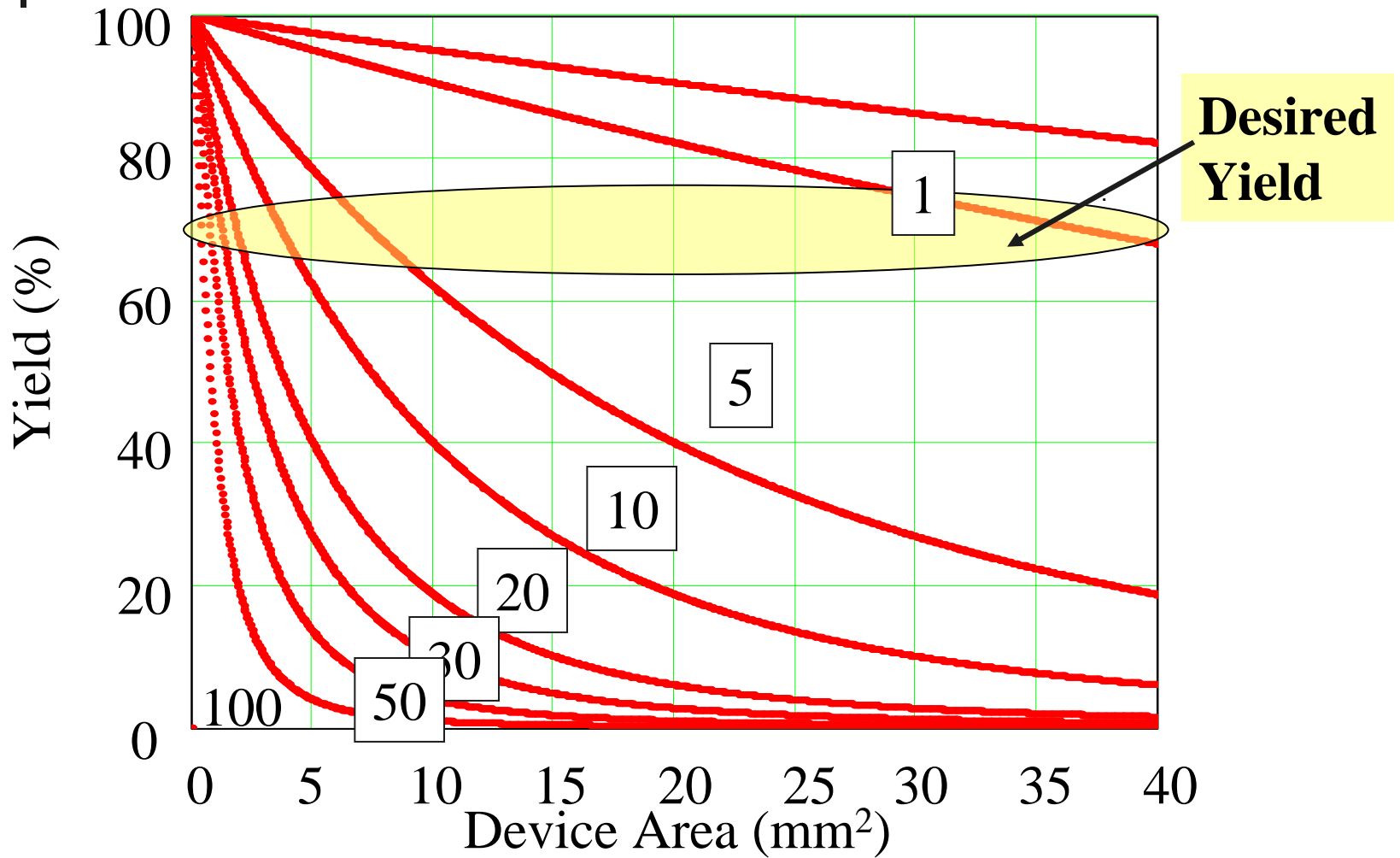
- Voltage 10-16 kV (Phase II Target)
- Current >200 Amp
- Frequency >20 kHz
- Fully Soldered Packaging on all terminals

High Voltage SiC Epitaxial Design

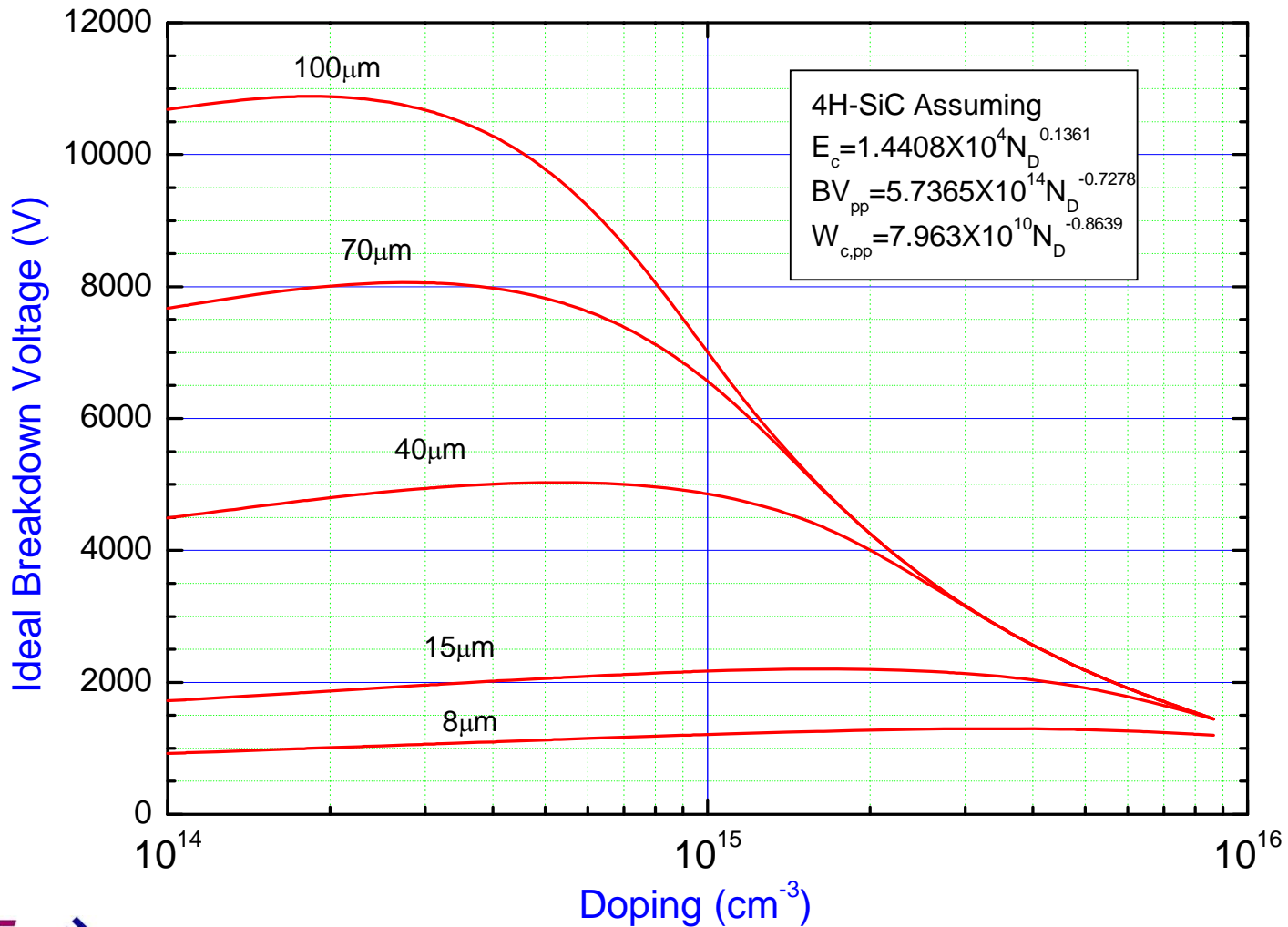


- Epitaxial thickness determines Blocking Voltage
 - Major technical challenge from materials growth standpoint
- Anode Area determines continuous Current rating
 - Material challenge from defect standpoint

Yield vs Defects Curve

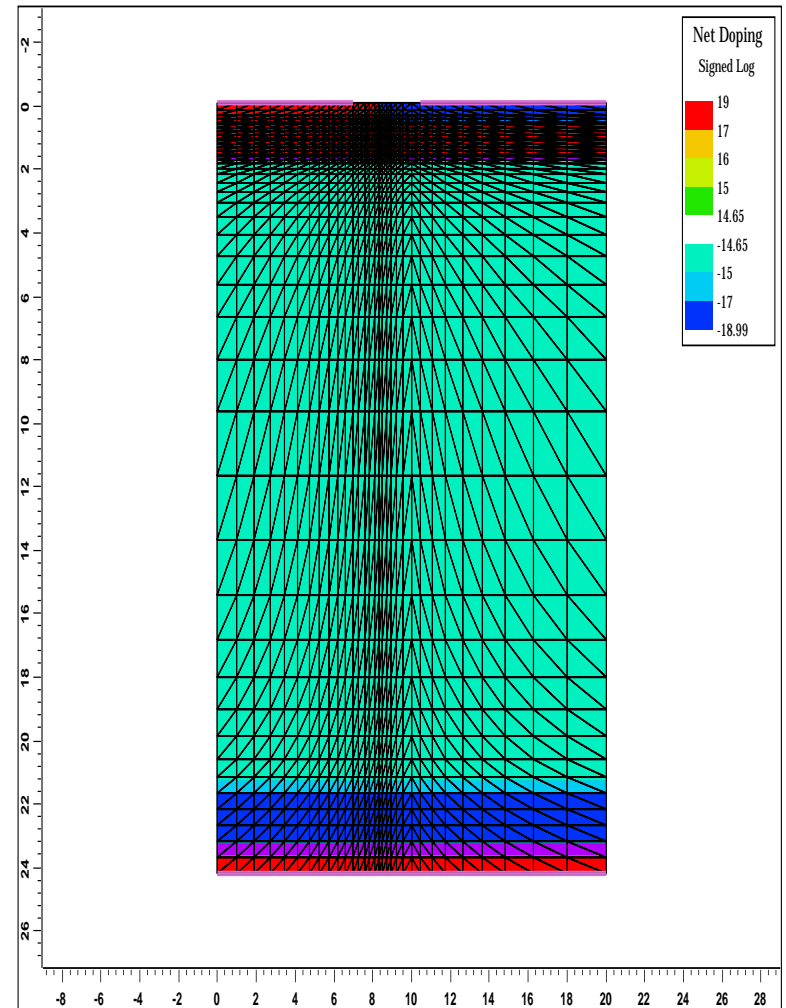


Epitaxial Design Curves



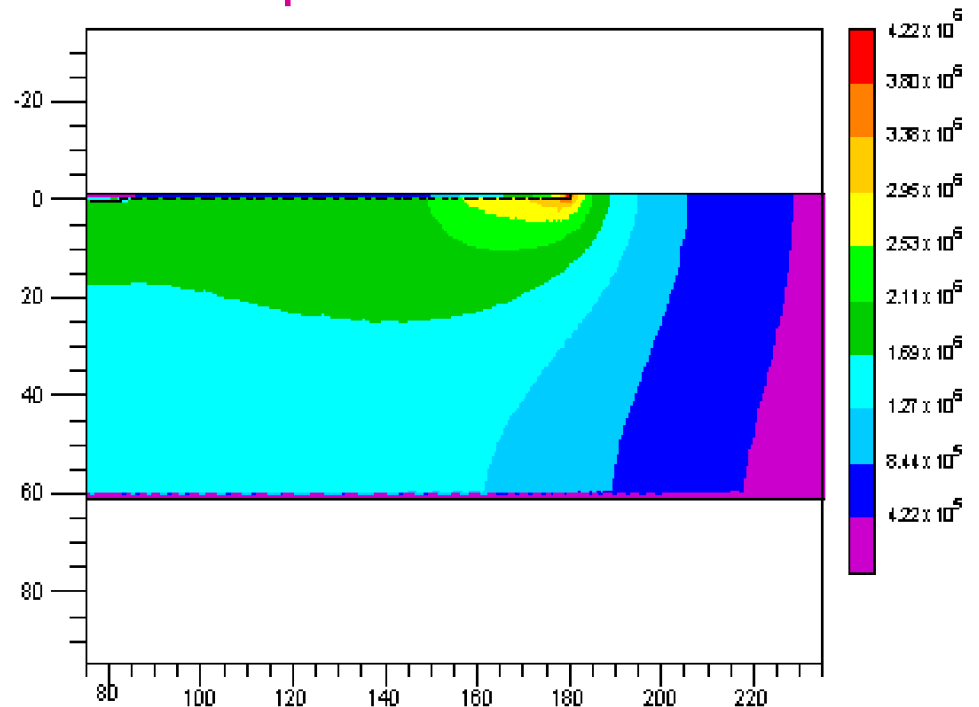
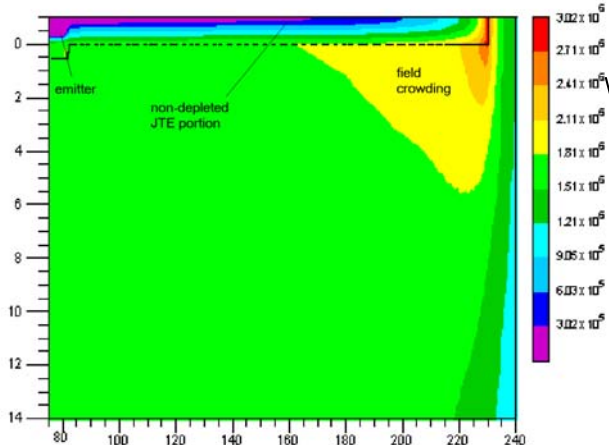
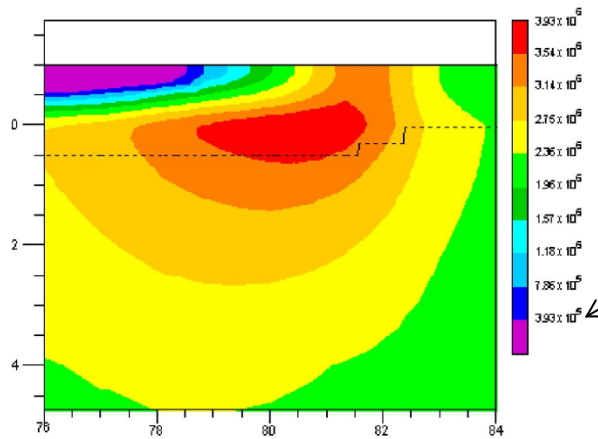
2D Device Simulations for Optimum GTO Thyristor Design

- Accurately predict Blocking Voltage
- Accurately predict Switching characteristics
- Process:
 - Initial Mesh Design
 - SiC modeling parameters
 - Numerical Methods choice
 - Simulation Experiments



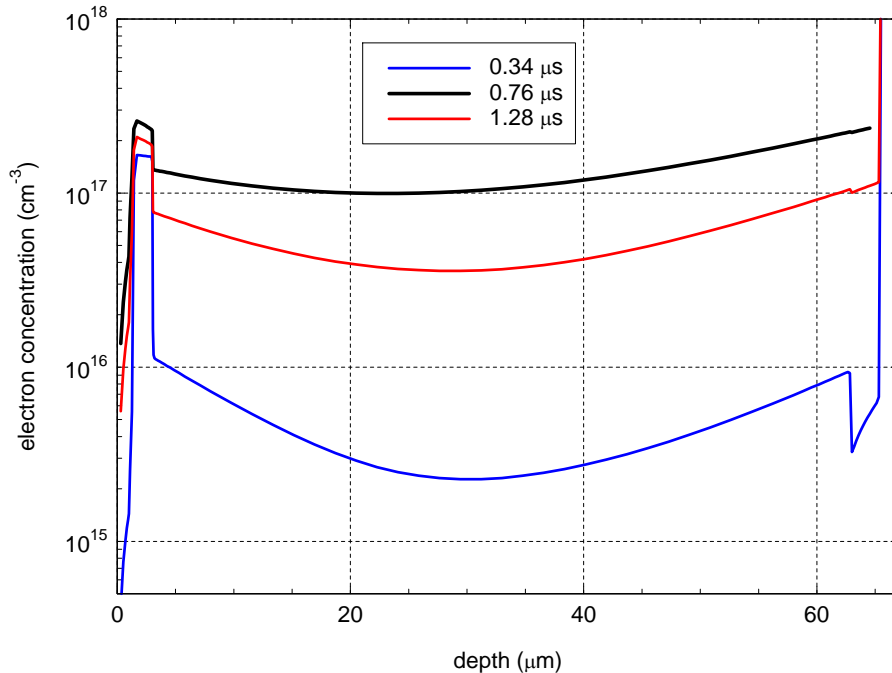
Breakdown Voltage Optimization

- Electric Field crowding determines BV
- BV near junction, or at the edge results in premature BV

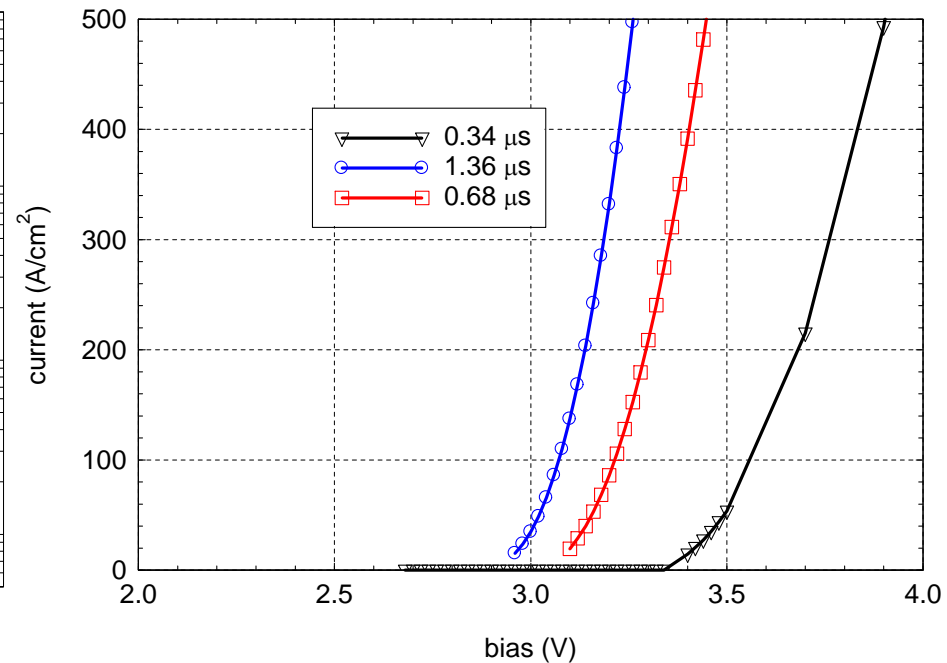


On-State operation of GTO Thyristors

3.5V forward bias

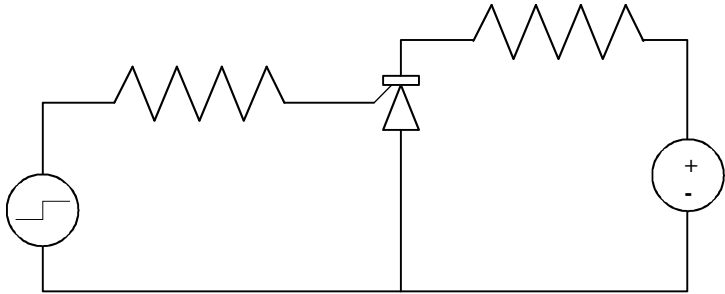


$\tau_{n0} = \tau_{p0} = 1 (0.5, 0.25) \mu\text{s}$

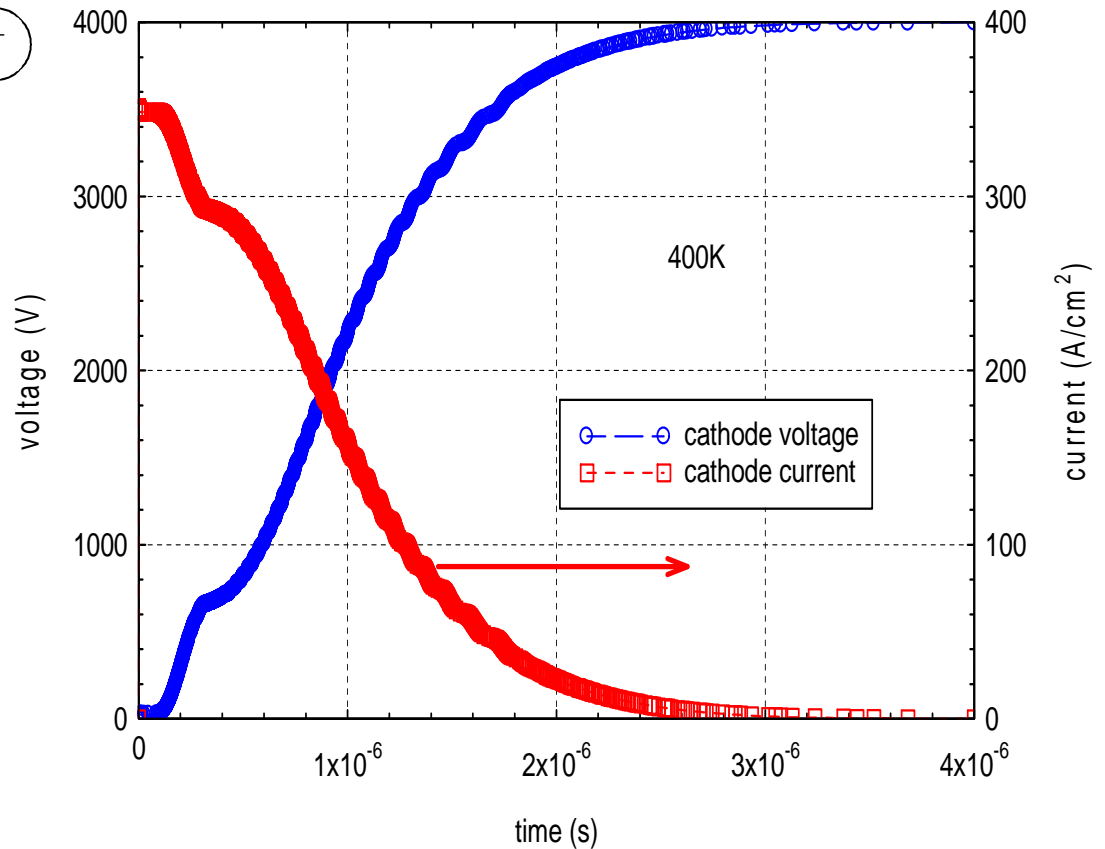


- High Carrier injection results in low on-state drop in GTO Thyristors
- On-State Voltage drop depends on Carrier Lifetime

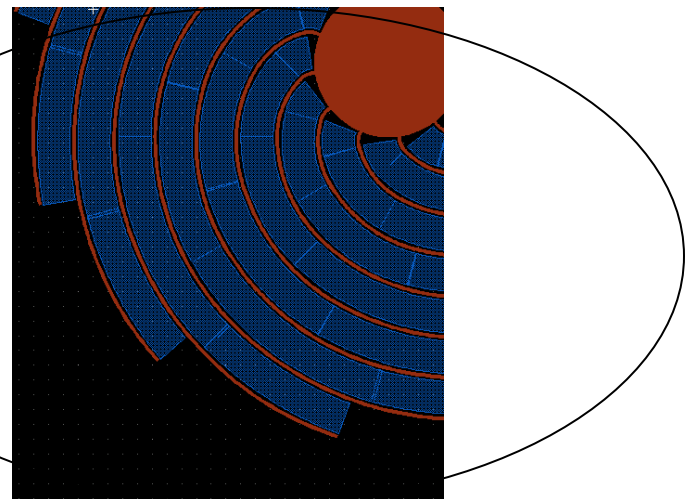
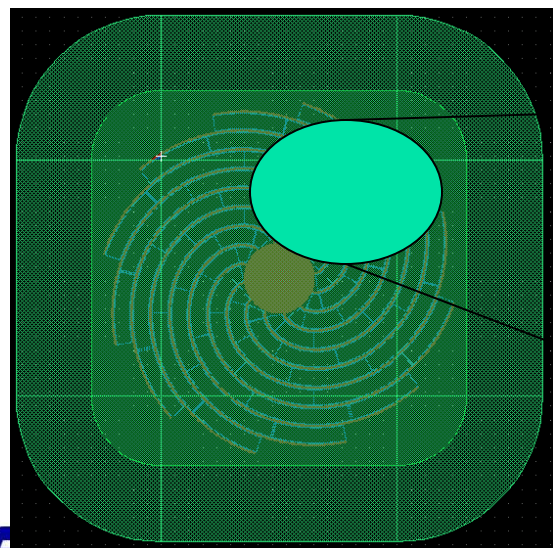
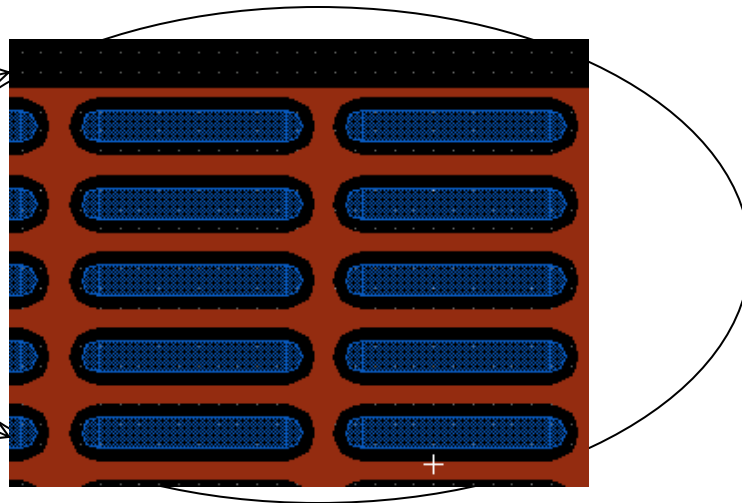
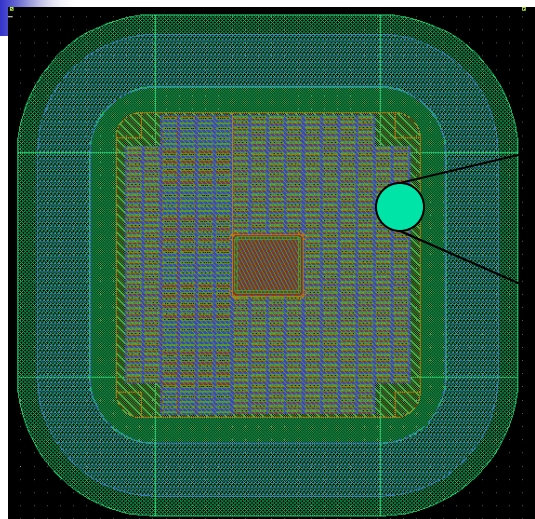
Turn-Off Simulations



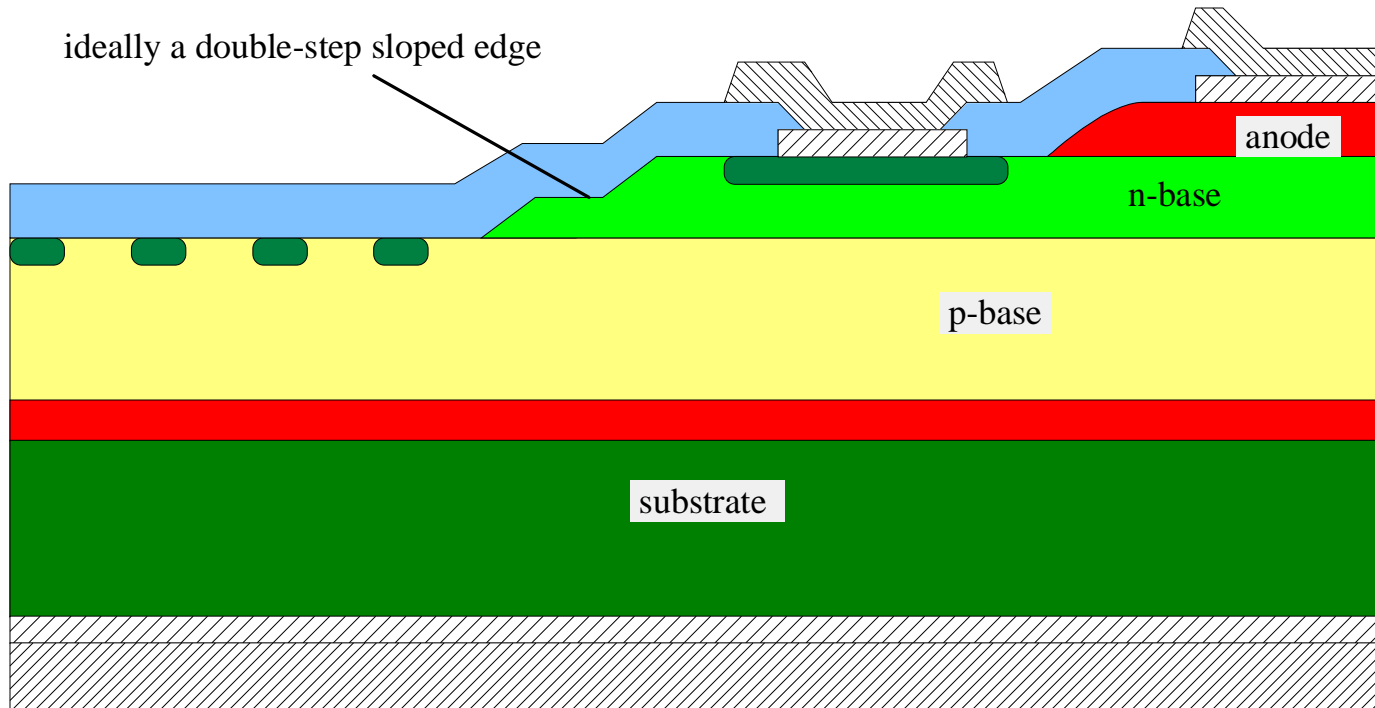
- Turn-Off speed depends on Gate Current
- 1.6 – 2 microseconds typical for Cathode $I = \text{Gate } I$ (pulse)



Cellular and Involute Designs

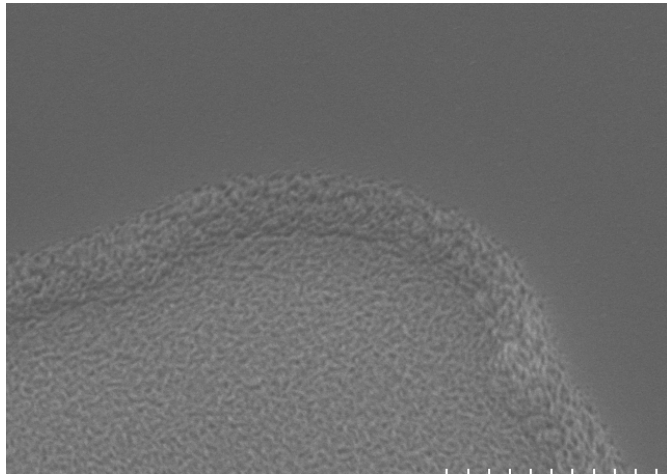


Fabrication Challenges



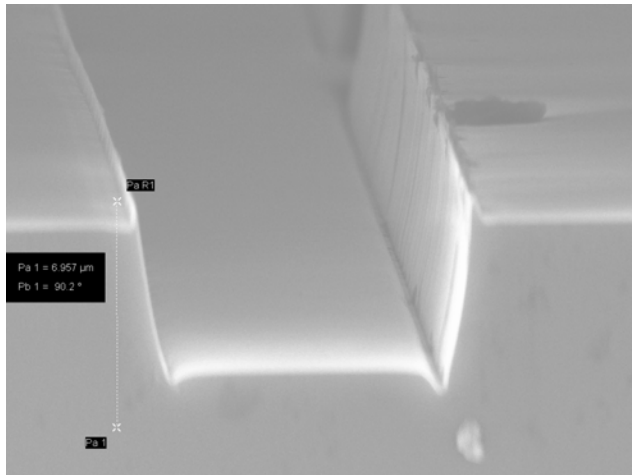
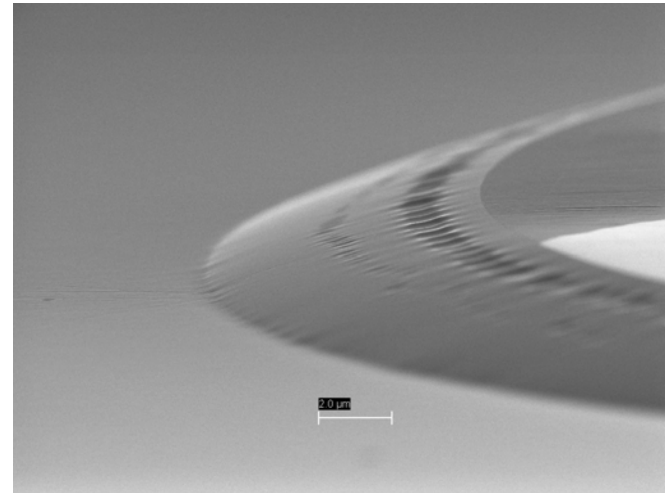
- A major fabrication challenge is achievement of sloped sidewall for high breakdown voltages

SEM Pictures of Dry Etching



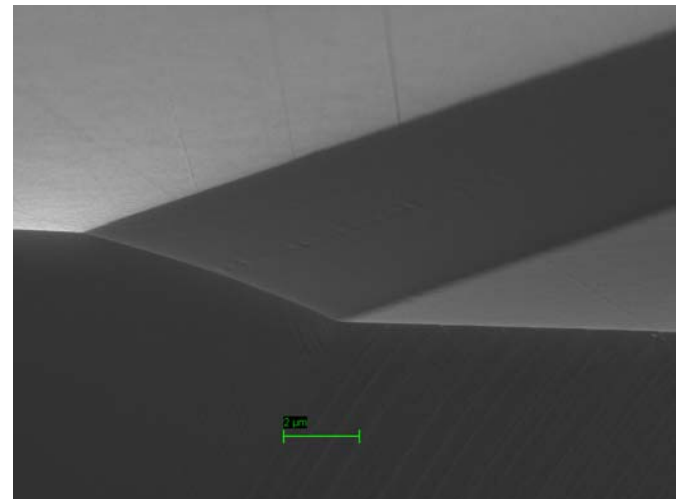
Pitting

"Ideal"
Profile
Achieved



Trenching

12° slope
Measured





Conclusions & Future Work

- Extensive 2D device simulation completed
- Major Experiments on Fabrication completed
- Improved Layouts designed

- Demonstrate GTO devices with good on-state and switching characteristics
- Package largest area chips for highest current per chip