CHEP95 Trigger and DAQ Summary

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Summary

- Present and future DAQ requirements
- DAQ subsystems
- Trigger level-1
- Frontend readout
- Event builder and switches
- Control and software
- Conclusions

C.1 - DAQ and Event Building

Overview and Performance of FNAL KTeV DAQ System
Tsuyoshi Nakaya - Fermilab

A Dead Time Free Data Acquisition System For the NA48 CERN Experiment
Musa Luciano - Instituto Nazionale di Fisica Nucleare

The BaBar Trigger, Readout and Event Gathering System
J. Frederic Kral - LBL

Level 1 DAQ System for the KLOE experiment
Albero Aloisio - Universita' di Napoli

Extending DART to meet the Data Acquisition Needs of Future Experiments at Fermilab
Ruth Pordes - Fermilab

The CMS data acquisition architecture
Sergio Cittolin - CERN

he DAQ and Trigger system of the ATLAS experiement at the LHC
Ralf Spiwoks/RD13 - CERN

The Alice Data Acquisition System
Pierre Vande Vyvre - CERN

A Millemium Approach to Data Acquisition: SCI and PCI
Hans Muller - CERN

Studies on Switch-based Event Building Systems in RD13
R. Spiwoks/RD13 - CERN

Event Building in Future DAQ Architectures Using ATM Networks
David D. Doughty Jr. - Christopher Newport University

Triggering and Event Building Results using the C104 Packet Routing Chip
D. Francis - Boston Universtiy

The US VME-P and Cern VSC Committee

Ruth Pordes - Fermilab

C.2 - Triggers

Design and Simulation for Real-Time distributed processing system
Iosif Legrand - DESY

The implementation of a first-level calorimeter trigger for LHC-type detectors as a special purpose parallel processor using large high-speed ASICs
Christian Bohm - University of Stockholm Sweden

Level-1 Calorimeter Trigger for CMS detector
Sridhara Dasu - University of Wisconsin

The Implementation of the ATLAS Level-1 Muon Trigger in the Barel Region
Emilio Petrolo - INFN Roma

The ATLAS Second Level Trigger
John R. Hansen - Niels Bohr Institute

Concept, Design and first Results of the fast H1 Second Level Trigger using Artificial Neural network
Thomas Kraemerkaemper - Humboldt University

The ZEUS Central Tracking Detector Second Level Trigger
H.A.J.R. Uijterwaal - University of Oxford

Neural Discriminating Analysis for a Second-Level Trigger System
Jose M. Seixas - EE/COPPE/EFRJ

C.3 - On-line Monitoring and Control Systems

The use of the SNMP (Simple Network Management Protocol) implementing Run and Data Flow Controls in the KLOE experiment.
Maria L. Ferrer - Frascati, Italy

The new ZEUS run control system: An exercise in modularity.
Jaroslaw Milewski - Hamburg University

On the Relevancy of Efficient, Integrated Computer and Network Monitoring in HEP Distributed Online Environment
Diego Carvalho - CERN

Interprocess and Interprocessor Data Flow in the KLOE Data Acquisition System
Harry Beker - CERN

A Scalable Data Acquisition System Using Transputers and the Chorus Operating System
D. Francis -

Evaluation of DAQ Performance
Yoshiji Yasu - KEK

Advanced Operating System Technologies
Fabio Riccardi - CERN

Experience on using Databases in the Aleph Data Acquisition and Control System
Pere Mato - CERN

Trigger and DAQ CHEP95 contributions

RUNNING EXPERIMENTS	
Aleph	Databases for DAQ and control systems
Delphi	Online distributed control and monitoring
Zeus	Level-2 central tracking trigger
	New control system.
H1	Level-2 tracking neural net trigger
CPLear	Level-3 Chorus OS for transputer farm
ALMOST RUNNING EXPERIMENTS	
NA48	Frontend readout implementations and performances
KTev	DAQ overview and performances
CLAS	ATM event builder studies
KLOE	DAQ system overview.
	Frontend Readout.
	Distributed processing and control.
	Data flow and software techniques
FUTURE RUNNING EXPERIMENTS	
Babar	DAQ system overview
HERA-B	Distributed RT processing simulation
ALICE	DAQ system overview
ATLAS	DAQ system overview.
	Event Builder tests.
	Level-1 calorimeter trigger.
	Level-1 muon trigger.
	Level-2 C104 based large switch.
	Level-2 ATLAS trigger system.
CMS	DAQ system overview.
	Level-1 calorimeter trigger
GENERIC PROJECT/DEVELOPMENTS	
DART	DAQ extension for future experiments
ATM	Evaluation of ATM based event building
SCI	SCI-PCI DAQ applications
NN	Level-2 trigger using neural nets
OS	Evaluation of DAQ performances
	Advanced OS technologies
VME	VSC committee

ALICE, ATLAS and CMS

ALICE	Rate	
Level-1		
		1500 MB/s
Level-3	50 Hz	10^5 MIPS
Tape	50 Hz	
Event size	**25 MB**	

ATLAS	Rate	
Level-1	40 MHz	
Level-2	**100 kHz**	**6 + 3 GB/s**
Level-3	1 kHz	$\approx 10^6$ MIPS
Tape	10 Hz	
Event size	1.5 MB	

CMS	Rate	
Level-1	40 MHz	
		20 GB/s
Level-3	**100 kHz**	$\approx 5\ 10^6$ MIPS
Tape	10Hz	
Event size	1 MB	

CLAS, NA48, KLOE, Babar

CLAS	Rate	
Level-1		
Level-2		
Level-3		
Tape		
Event size		

NA48	Rate	
Level-1		
Level-2		
Level-3		
Tape		
Event size		

KLOE	Rate	
Level-1		
Level-2		
Level-3		
Tape		
Event size		

Babar	Rate	
Level-1		
Level-2		
Level-3		
Tape		
Event size		

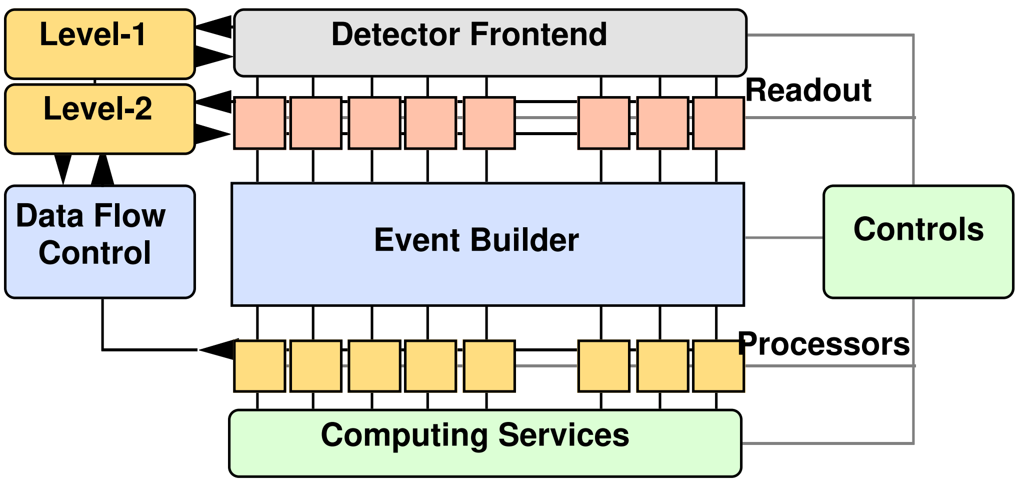
KTeV, ZEUS

KTeV	Rate	
Level-1		
Level-2		
Level-3		
Tape		
Event size		

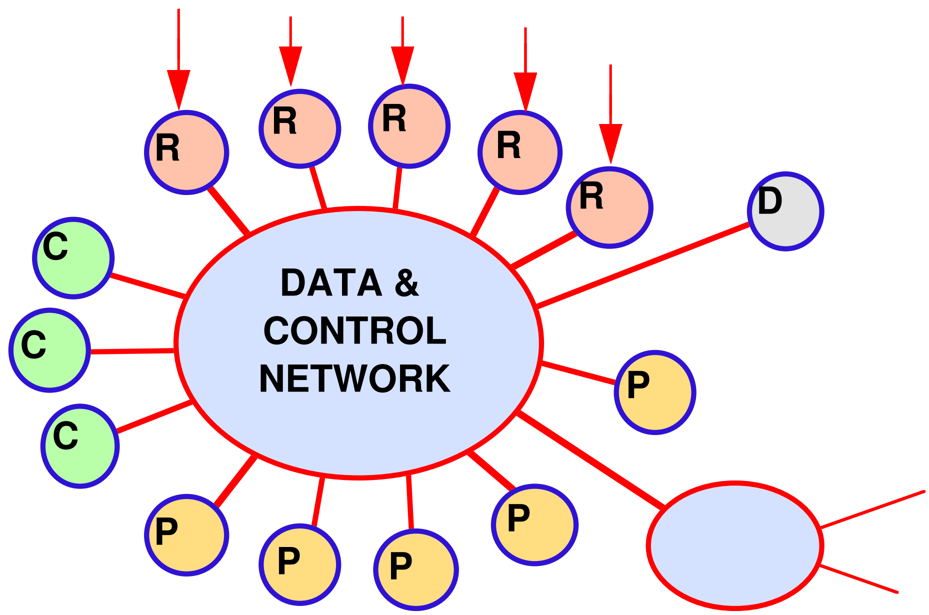
ZEUS	Rate	
Level-1		
Level-2		
Level-3		
Tape		
Event size		

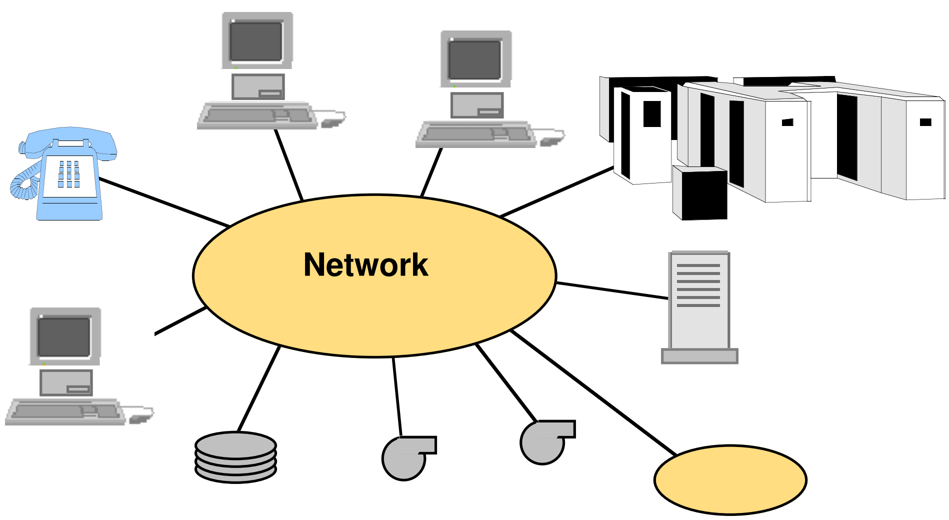
DAQ standard model

- Multi-partition parallel readout
- High speed interconnection systems
- Distributed processing for trigger, control and analysis

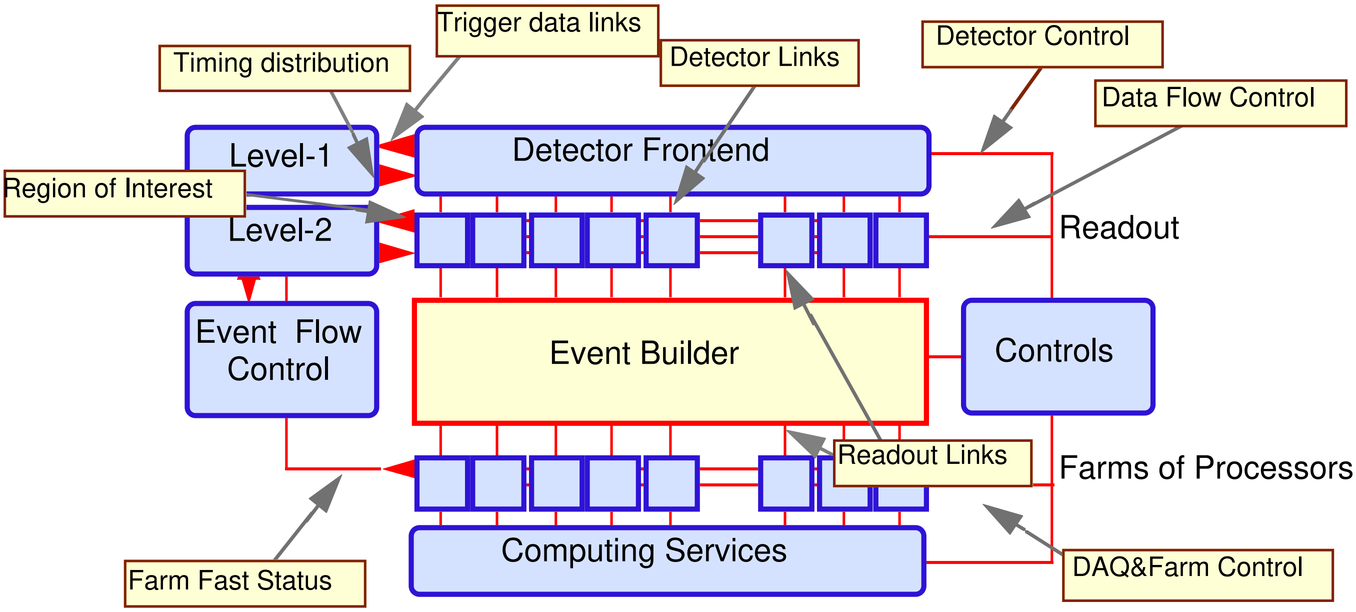


Trigger and DAQ logical structure





Trigger and DAQ computing and communications subsystems



COMPUTING subsystems

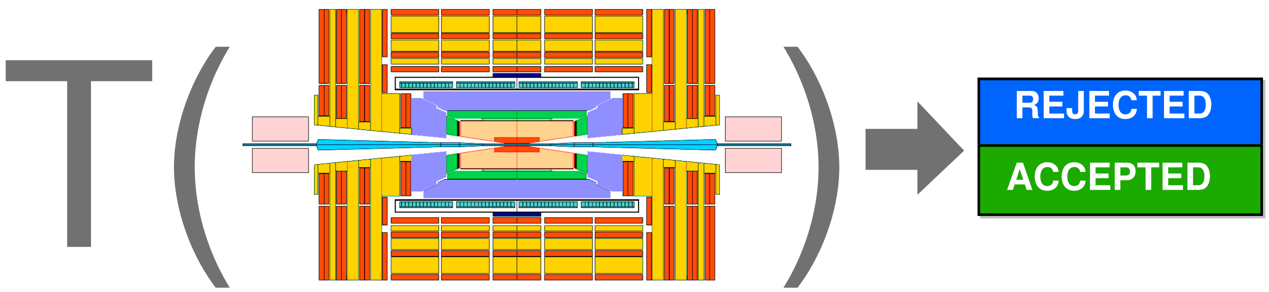
- **Detector frontend.** Shaping/pipelining/digitizing detector electronics
- **Level-1.** Trigger processor based on prompt detector data
- **Level-2.** Trigger processor based on detector full granularity selected data (RoI)
- **Readout unit.** Basic data acquisition unit with multi-event buffering capabilities
- **Event Flow Control.** Event builder data scheduler and high trigger level monitor
- **Event filter.** High trigger levels and analysis by commercial processor farm/desktop array
- **Computing service**. Mass storage and computing infrastructures
- **Controls.** Distributed processor and data bases systems for on-line monitoring

COMMUNICATIONS subsystems

- **Trigger data links.** Fast data link for trigger data readout
- **Region of Interest (RoI).** Selective data readout network
- **Detector links.** Detector analog/digital readout links
- **Timing distribution.** Trigger and DAQ signals distribution system
- **Event Builder.** Readout network (e.g. switch fabric)
- **Readout links.** Point to point connection between (switch,) readout and filter units
- **Control communications.** Multiprocessor/multi-crate interconnection systems
- **Farm status.** Event Manager high level trigger farm status collection
- **Readout Status.** Data flow signals and error messages collection system

The trigger system

The trigger is a function of :



Event data & Apparatus
Physics channels & Parameters

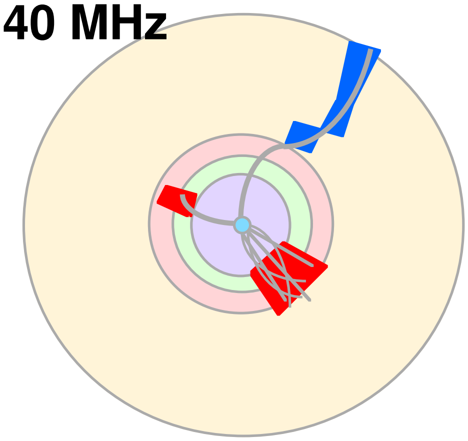
Since the detector data are not all promptly available and the function is highly complex, T(...) is evaluated by successive approximations called :

TRIGGER LEVELS

(possibly with zero dead time)

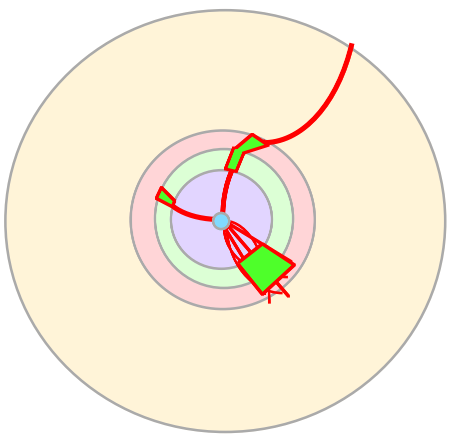
The trigger levels at LHC

40 MHz



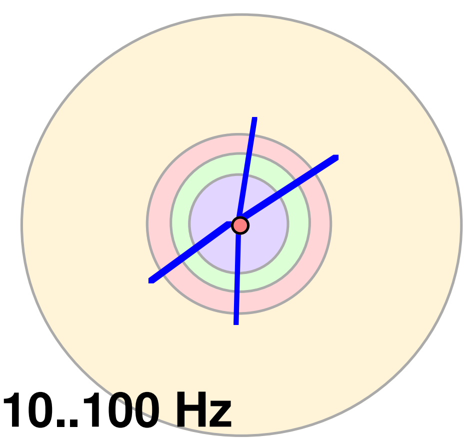
Particle identification
(High pT electron, muon, jets, missing ET)

- Local pattern recognition and energy evaluation on prompt macro-granular information



Clean particle signature (Z, W, ..)

- Finer granularity precise measurement
- Kinematics. Effective mass cuts and event topology
- Track reconstruction and detector matching

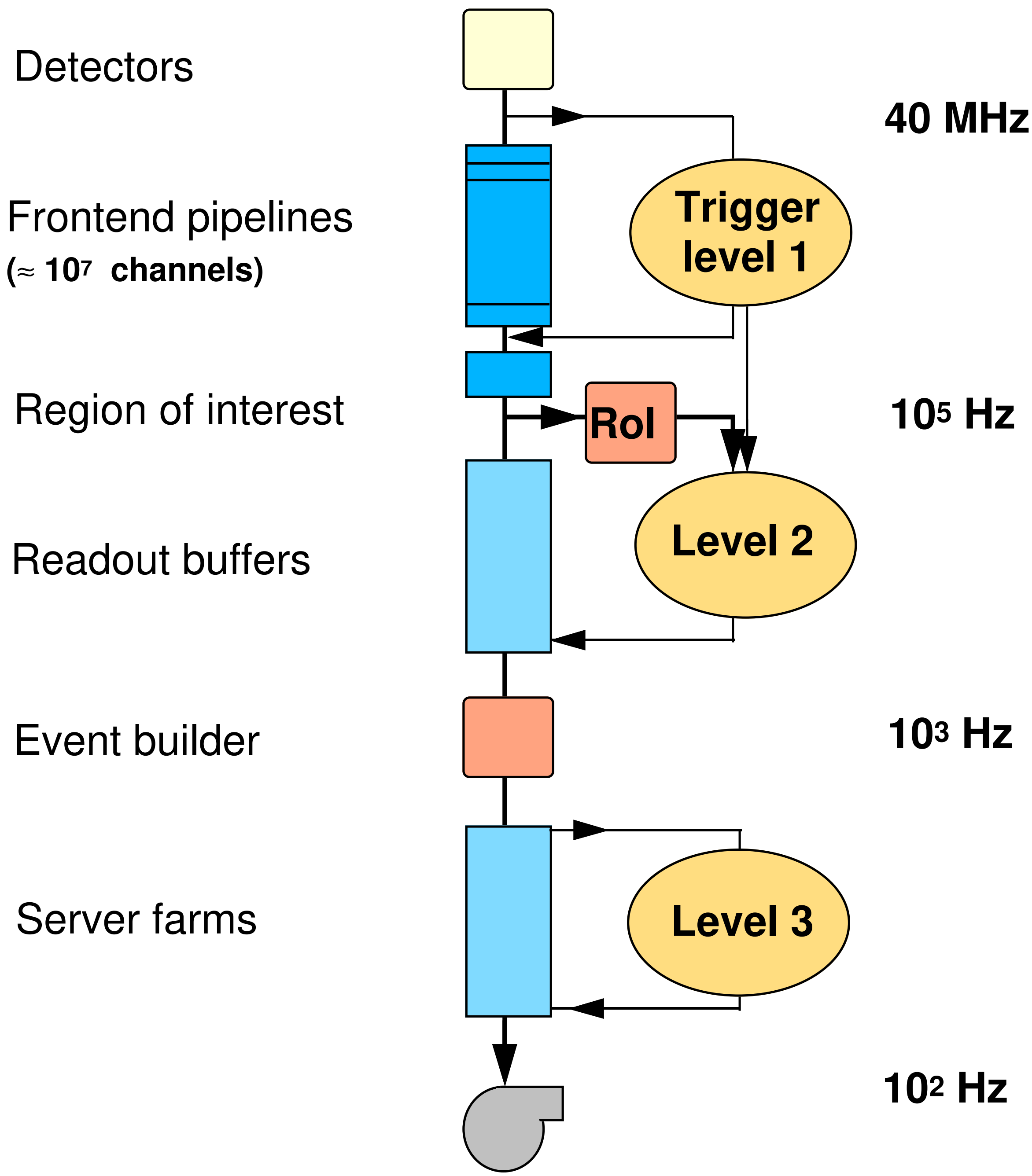


Physics process identification

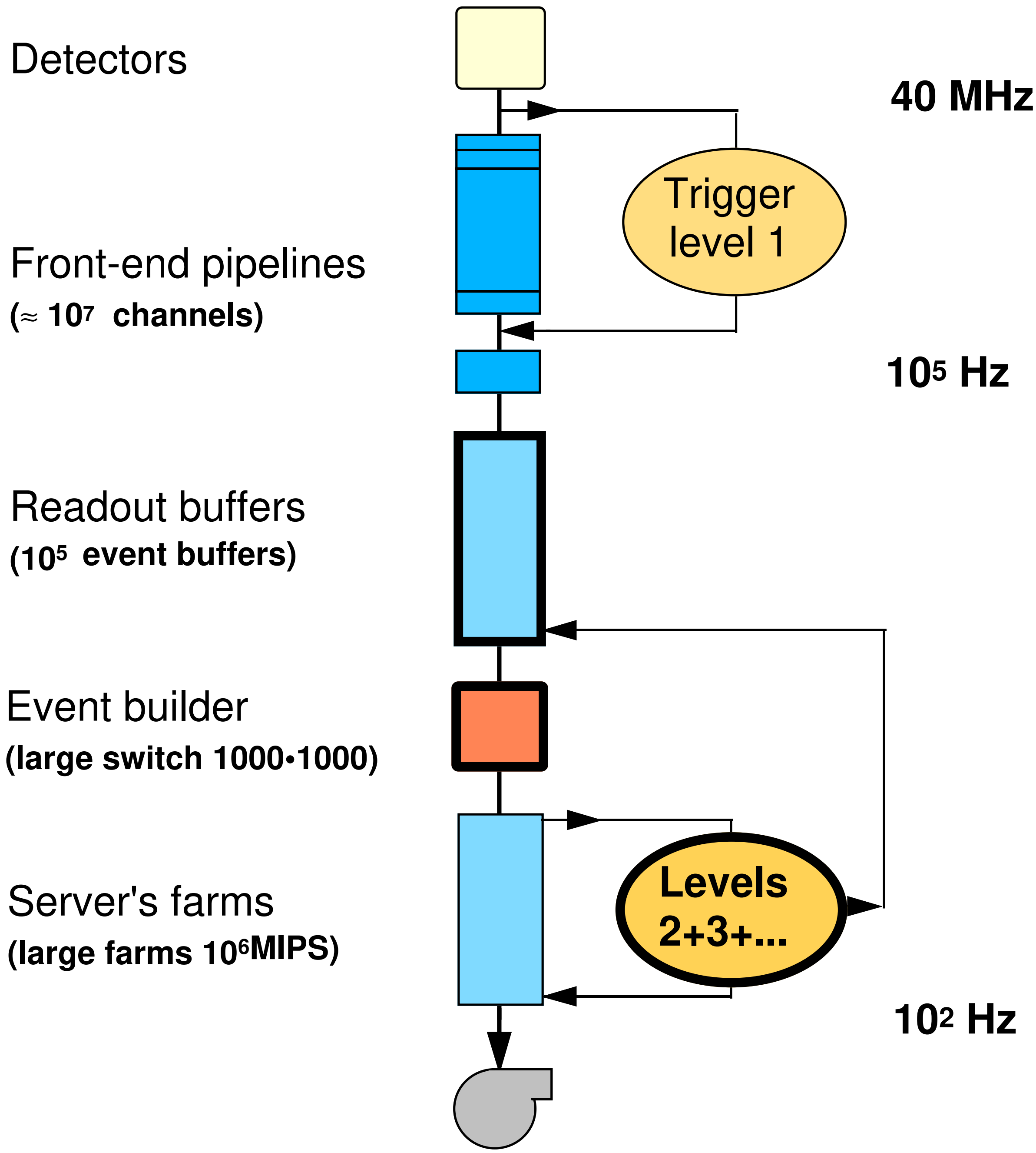
- Event reconstruction and analysis

10..100 Hz

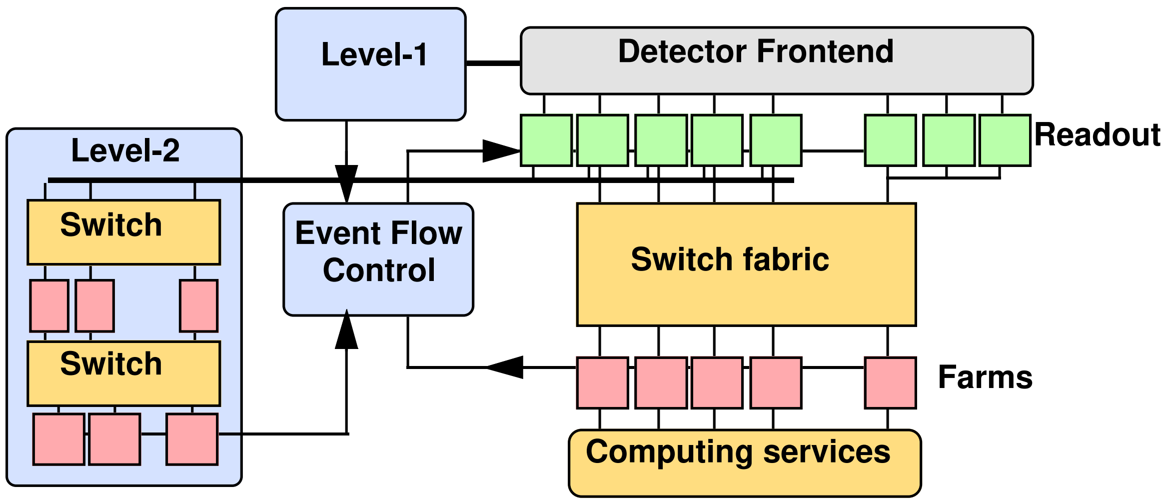
Three physical level DAQ



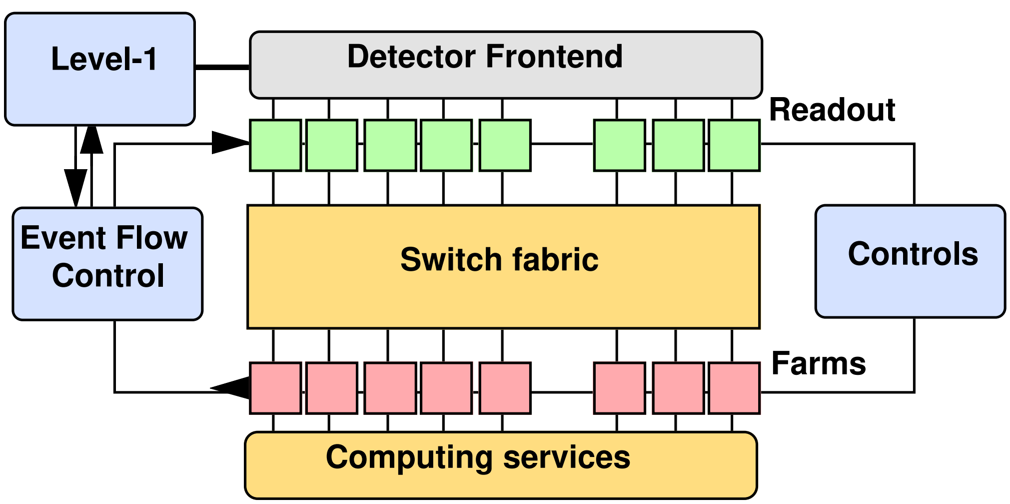
Two physical levels DAQ



ATLAS and CMS DAQ systems



TWO PHYSICAL LEVEL TRIGGERS DATA ACQUISITION SYSTEM

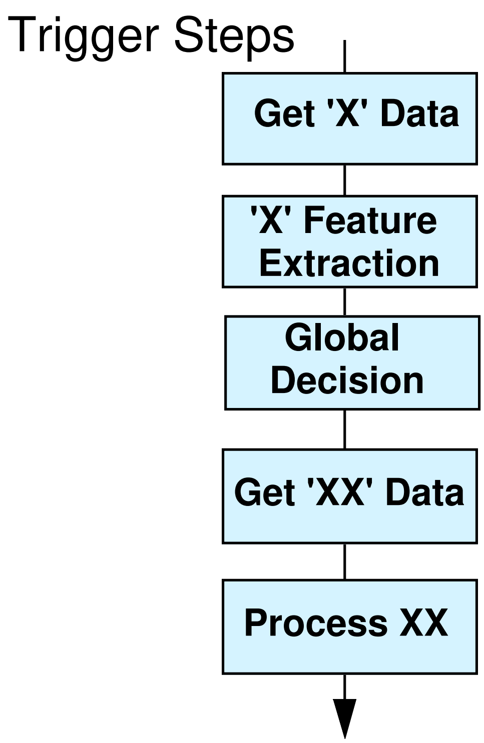


THREE PHYSICAL LEVEL TRIGGERS DATA ACQUISITION SYSTEM

Event selection

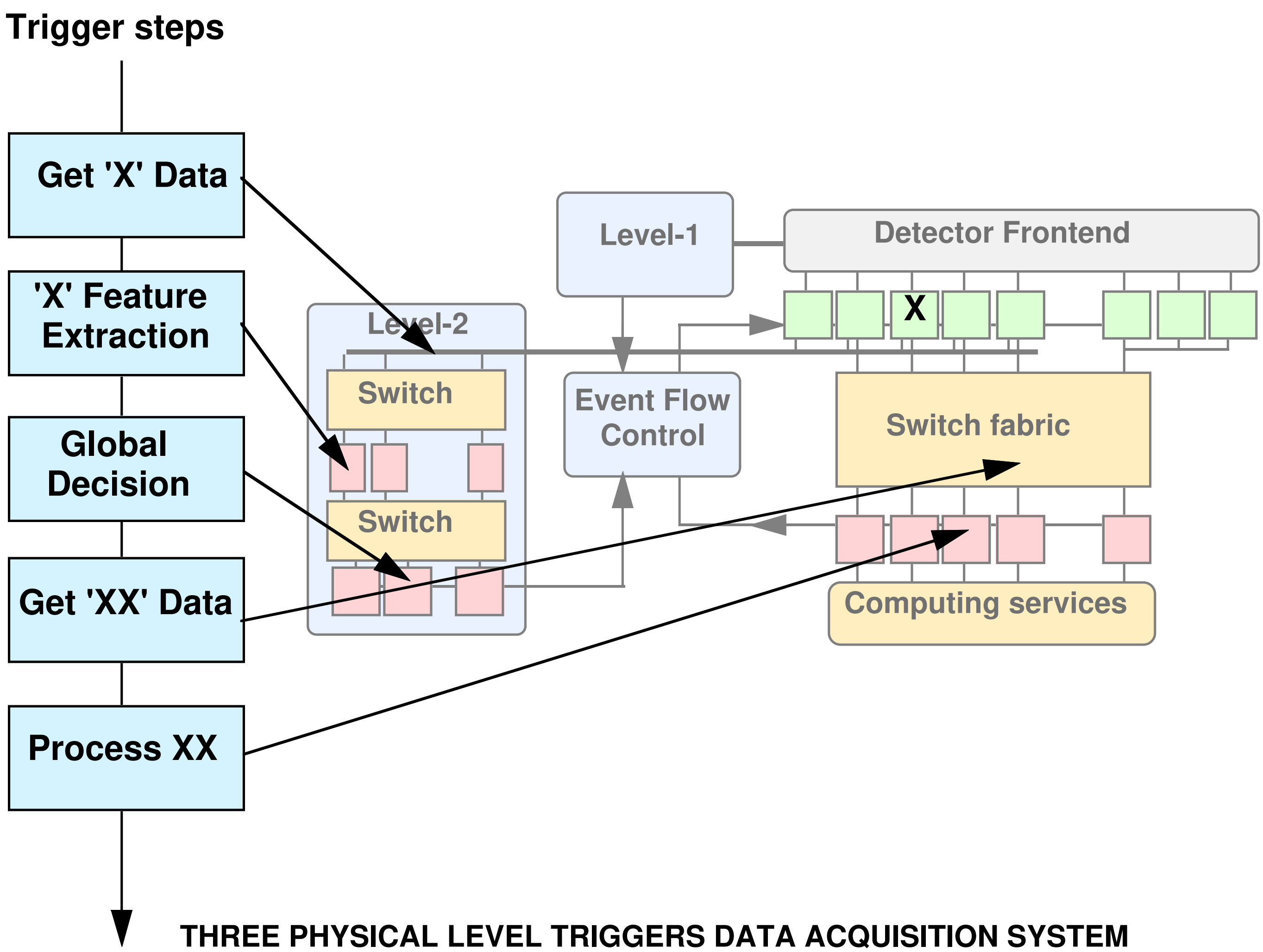
```
Detector data
X, Y, Z
XX, YY, ZZ
.....
```

```
CALL PROCESS (X,,,)
IF (X > T) AND (...) THEN Reject
   ELSE CALL PROCESS1 (XX,,,)
   IF (XX > T) AND (...) THEN Reject
   ELSE ...
```



The DAQ system is mainly determined by the implementation of these two first steps

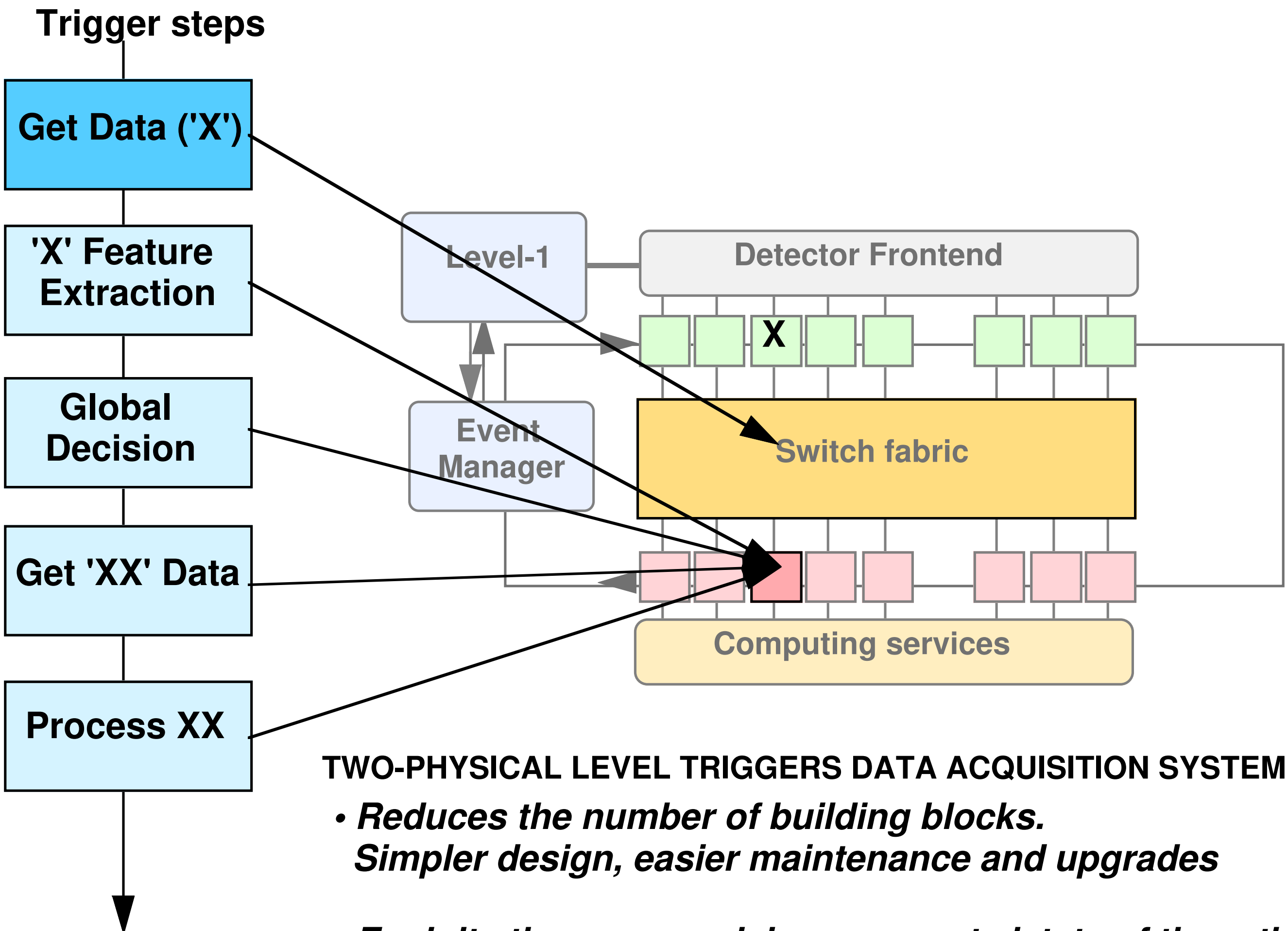
Three physical levels DAQ system



THREE PHYSICAL LEVEL TRIGGERS DATA ACQUISITION SYSTEM

- ***Reduces the demands in the readout network bandwidth***
- ***............***

Two physical levels DAQ system



TWO-PHYSICAL LEVEL TRIGGERS DATA ACQUISITION SYSTEM

- ***Reduces the number of building blocks.***
  Simpler design, easier maintenance and upgrades

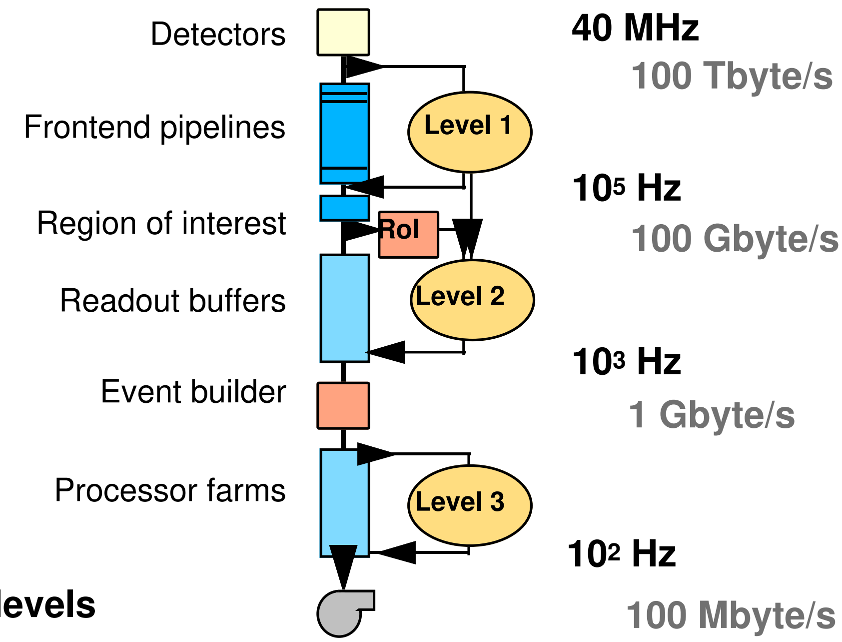
- ***Exploits the commercial components 'state of the art'***
  (memory, switches, CPU)

- ***Upgrades and scales with the machine performances.***
  Flexibility in logical redistribution of resources

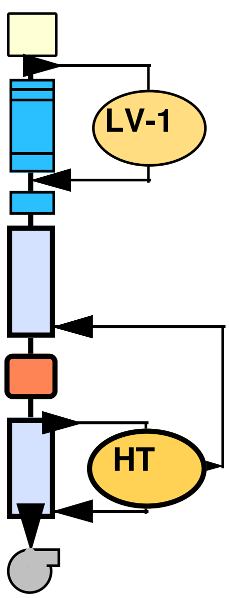
- ***Makes full use of the computing power anyway needed for the off-line analysis***

Rate decimation and trigger levels

Three physical levels



Two physical levels



- Reduces the number of building blocks. Simpler design, easier maintenance and upgrades
- Exploits the commercial components 'state of the art' memory, switch, CPU
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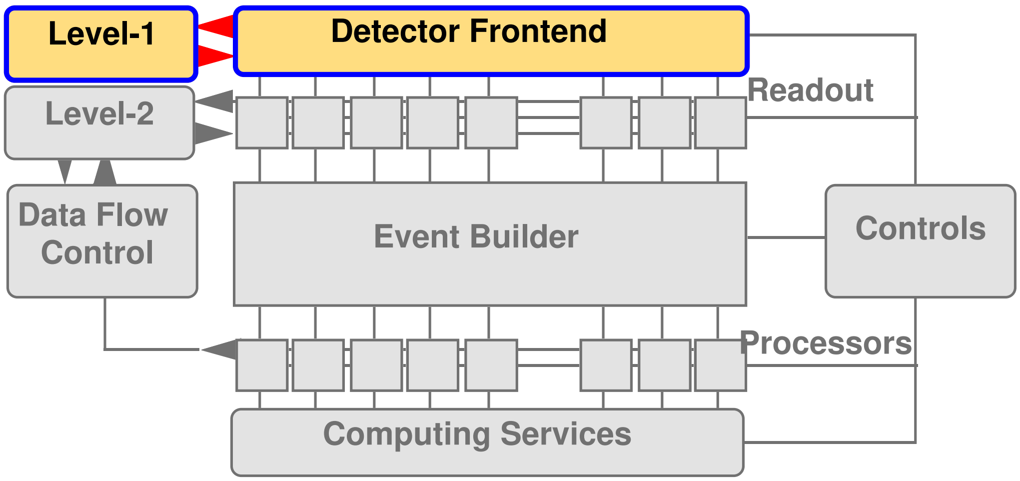
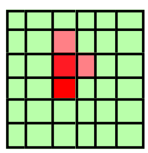
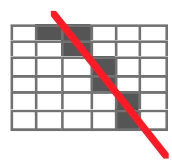
Level-1 trigger



Level-1 trigger COMPUTING AND COMMUNICATIONS SUBSYSTEMS:

- Local data processing and pattern recognition units for :

Cluster finding  Segment finding 

- Local/Global logic to identify :

- **- Objects:** Electron/photon (isolation requirement), Muons, Jets, Missing E_T
- **- Background** (e/γ): High-p_T jets

- Trigger data link. 1 Gbit/s link (to transmit synchronously 21bits/25ns)

- Fast signal and timing distribution. Trigger control signal distribution

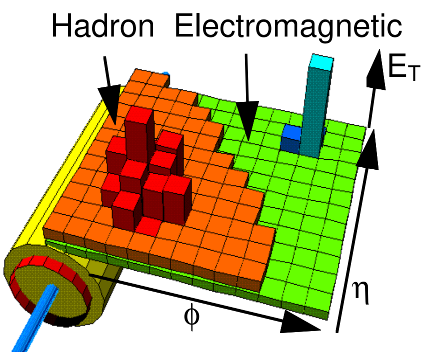
Level-1 Contributions

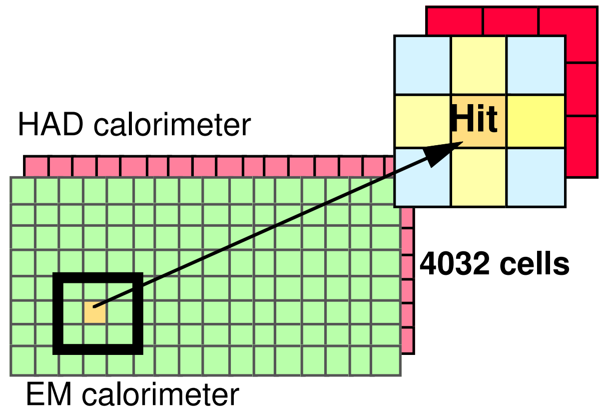
The implementation of a first-level calorimeter trigger for LHC-type detectors as a special purpose parallel processor using large high-speed ASICs
Christian Bohm - University of Stockholm Sweden

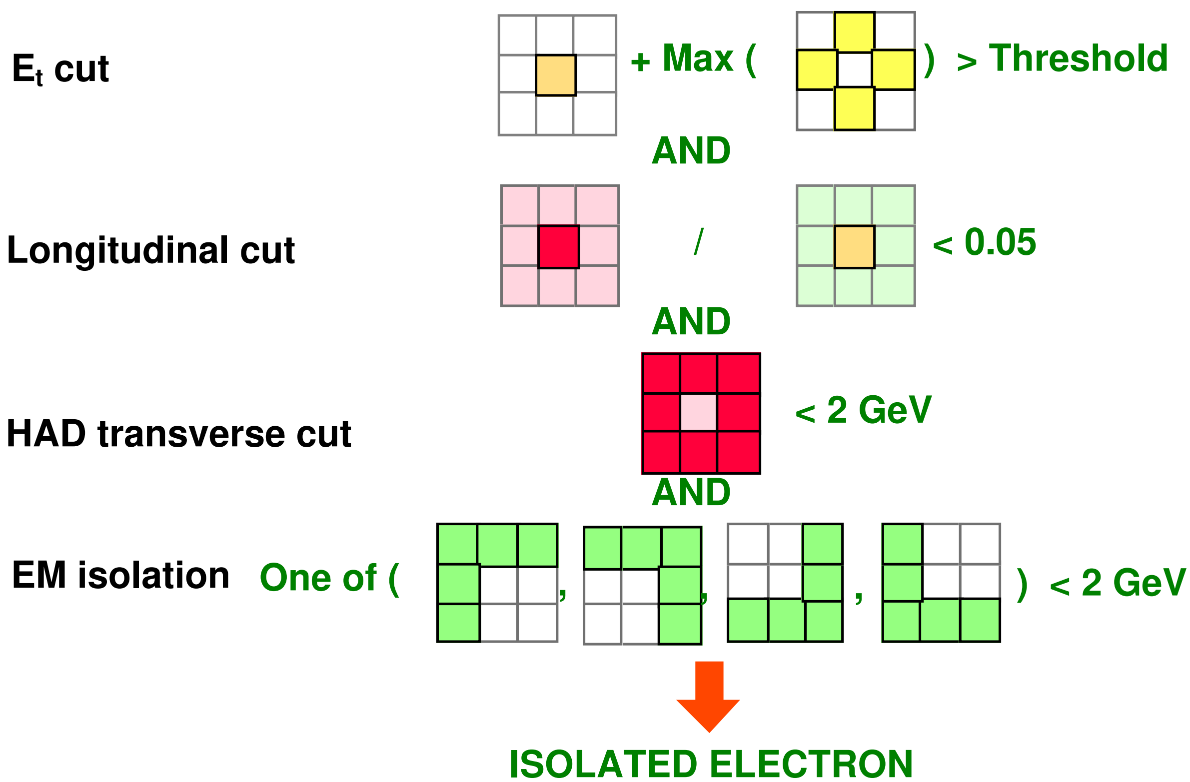
Level-1 Calorimeter Trigger for CMS detector
Sridhara Dasu - University of Wisconsin

The Implementation of the ATLAS Level-1 Muon Trigger in the Barel Region
Emilio Petrolo - INFN Roma

CMS calorimeter level-1. Isolated electron
(sliding window algorithm)

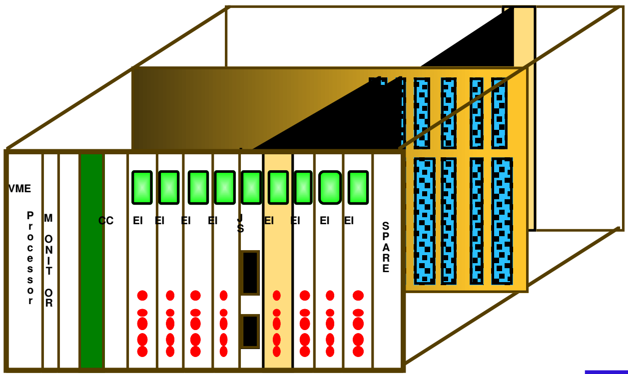




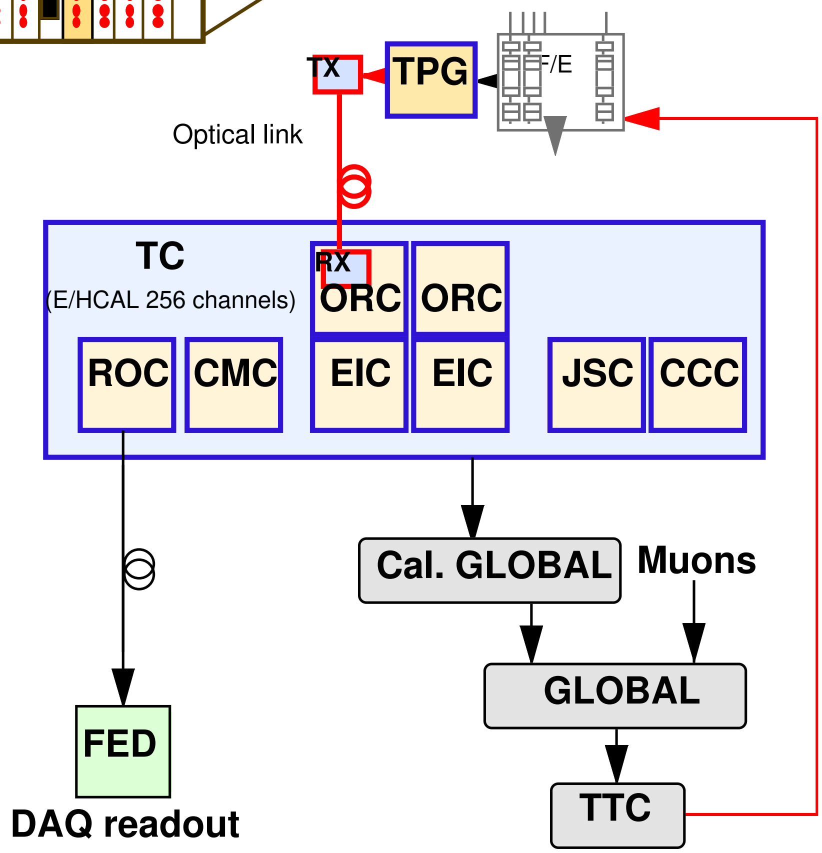


Level-1 Calorimeter Trigger for CMS detector
Sridhara Dasu - University of Wisconsin

CMS level-1 trigger. Calorimeter regional crate

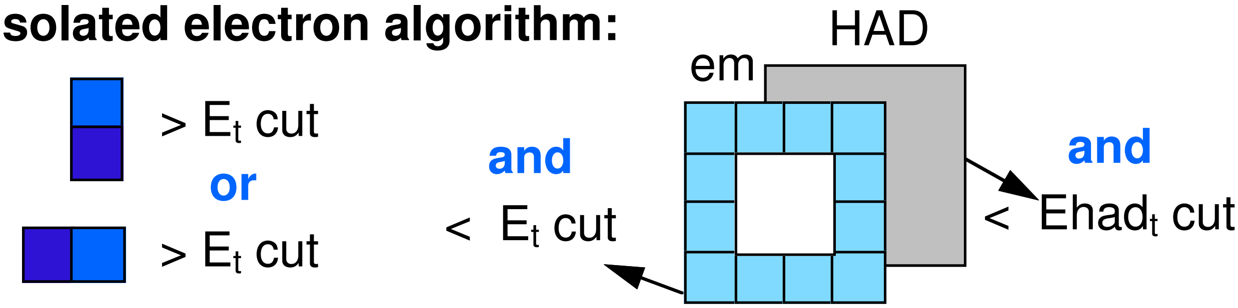


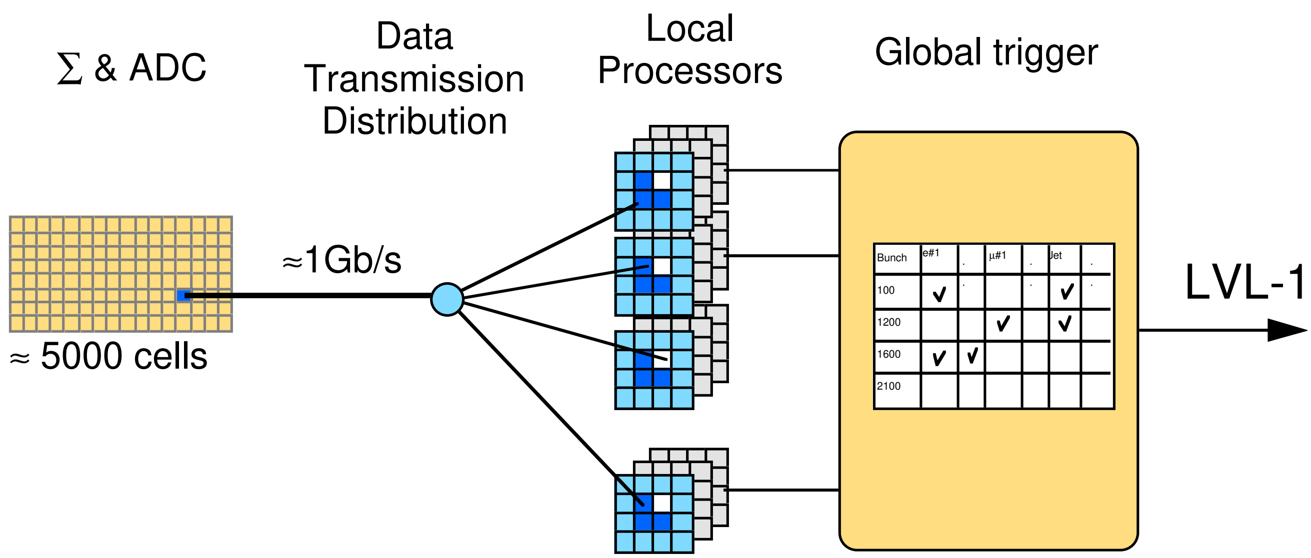
Calorimeter regional crate
256 E/HCAL trigger channels per crate.
Two back to back crates with common backplane connecting the optical receivers and the trigger processing cards.



TC Trigger Crate
ORC Optical Receiver Card
TX Optical transmitter
RX Optical receiver
EIC Electron Isolation Card
JSC Jet Summary Card
CCC Clock and Control Card
ROC Monitor and DAQ processor
CMC Crate Monitor Card
FED Readout FrontEnd Driver
TPG Trigger Primitive Generator

Isolated electron algorithm:

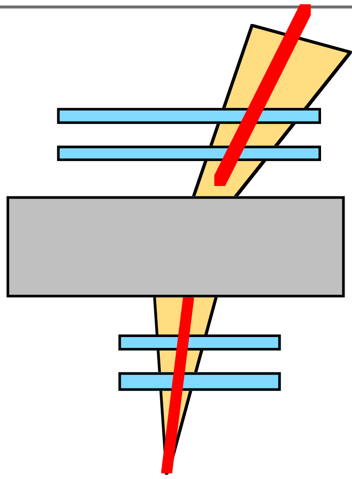




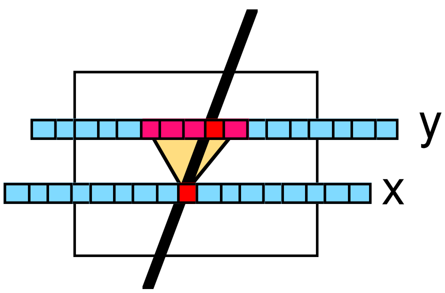
The implementation of a first-level calorimeter trigger for LHC-type detectors as a special purpose parallel processor using large high-speed ASICs

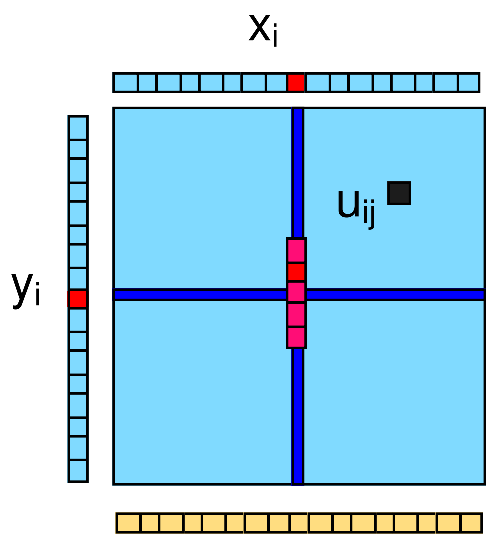
Christian Bohm - University of Stockholm Sweden

ATLAS level-1 muon trigger



Segment identification
within a given angles and
segments combination





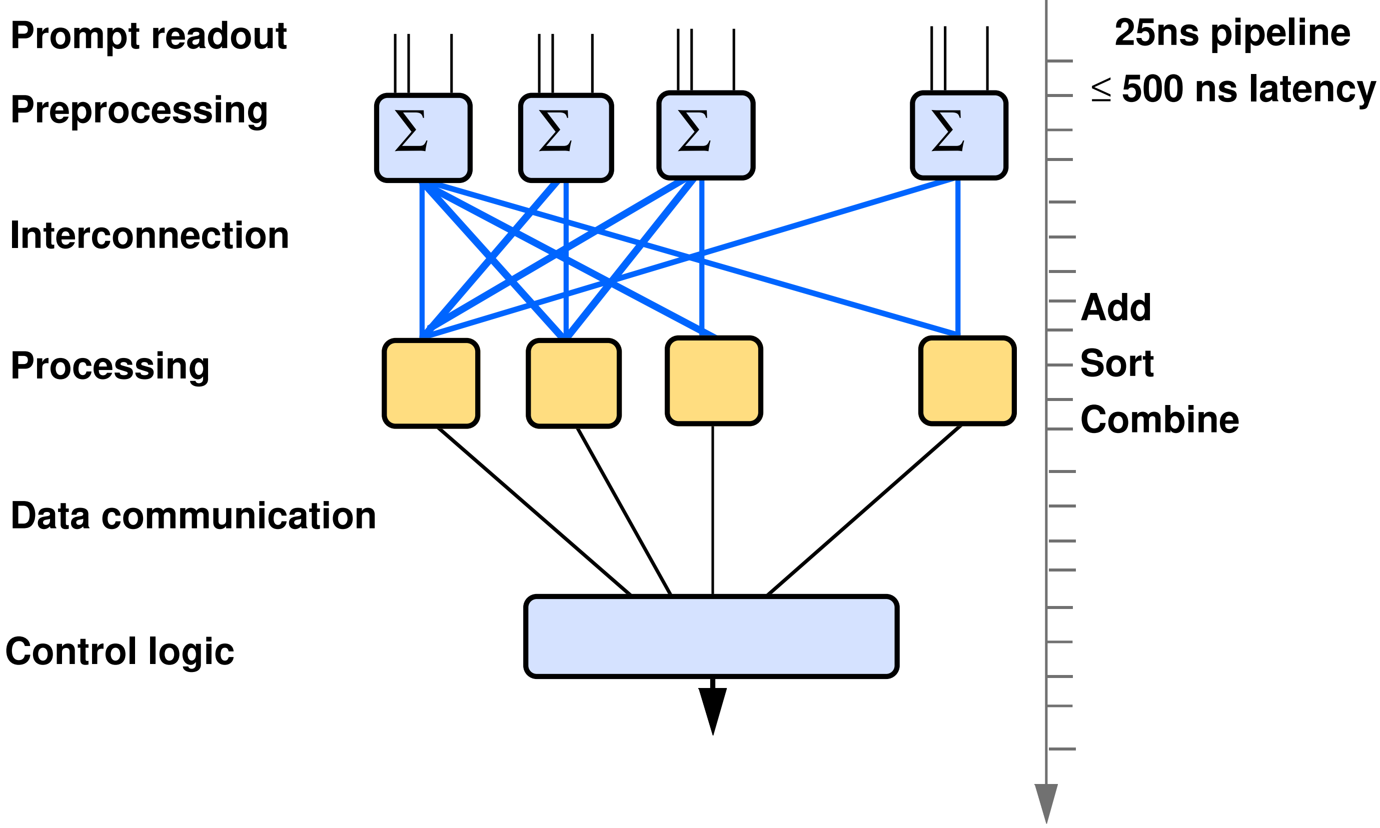
$$z_i = \sum x_j \bullet u_{ij} \bullet y_j$$

- Two planes low occupancy detectors
- Tree logic for more plane/segments (and pipeline)

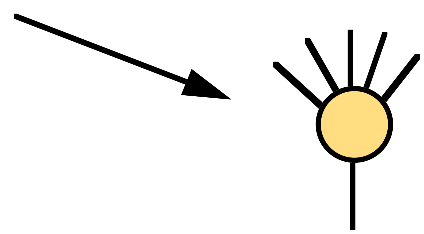
The Implementation of the ATLAS Level-1 Muon Trigger in the Barel Region

Emilio Petrolo - INFN Roma

Level-1 trigger processor main steps

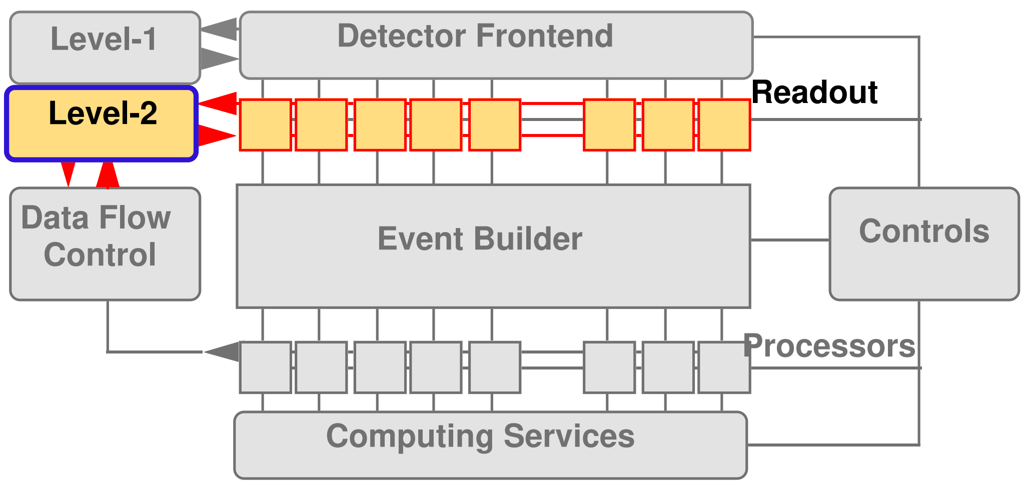


- Fast data link (≈1Gb/s)
- Pipelined processing elements (40,80,160 MHz)
- High speed interconnection network



NN

Level-2 trigger systems



Level-2 trigger COMPUTING AND COMMUNICATIONS SUBSYSTEMS:

- **Feature extraction.** Processor system detector data specialized
- **Local/Global level-2 processors**

- **Region of Interest.** Selective data access system
- **Level-2 data network**. Intercommunication between Level-2 components

Level-2 contributions

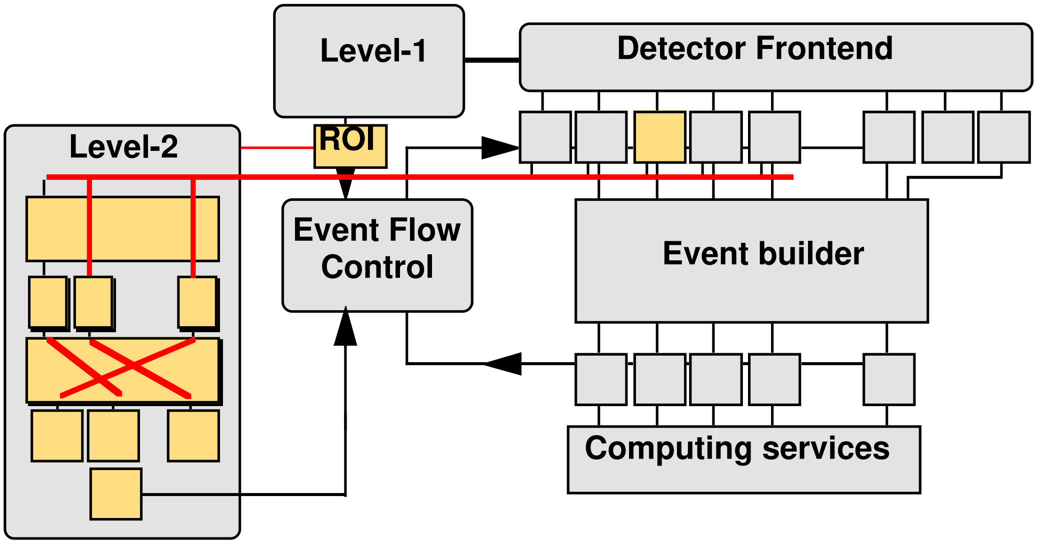
Concept, Design and first Results of the fast H1 Second Level Trigger using Artificial Neural nettwork
Thomas Kraemerkaemper - Humboldt University

Neural Discriminating Analysis for a Second-Level Trigger System
Jose M. Seixas - EE/COPPE/EFRJ

The ATLAS Second Level Trigger
John R. Hansen - Niels Bohr Institute

The ZEUS Central Tracking Detector Second Level Trigger
H.A.J.R. Uijterwaal - University of Oxford

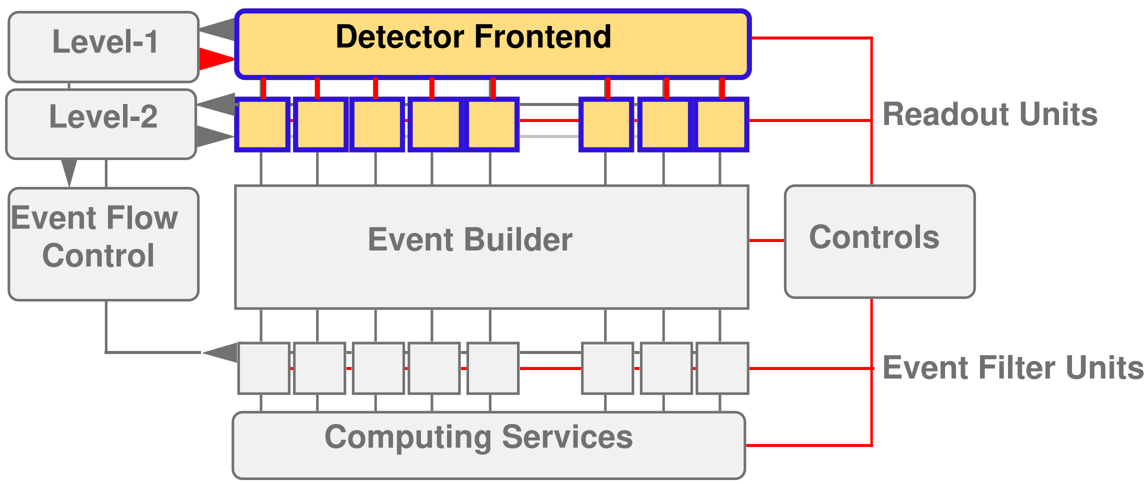
ATLAS level-2



Physical level-2 based on

- Few Regions Of Interest relevant to trigger decisions
- Selected information (ROI) by routers and switches
- Feature extractors (DSP or specialized)
- Staged local and global trigger processors

Detector frontend readout

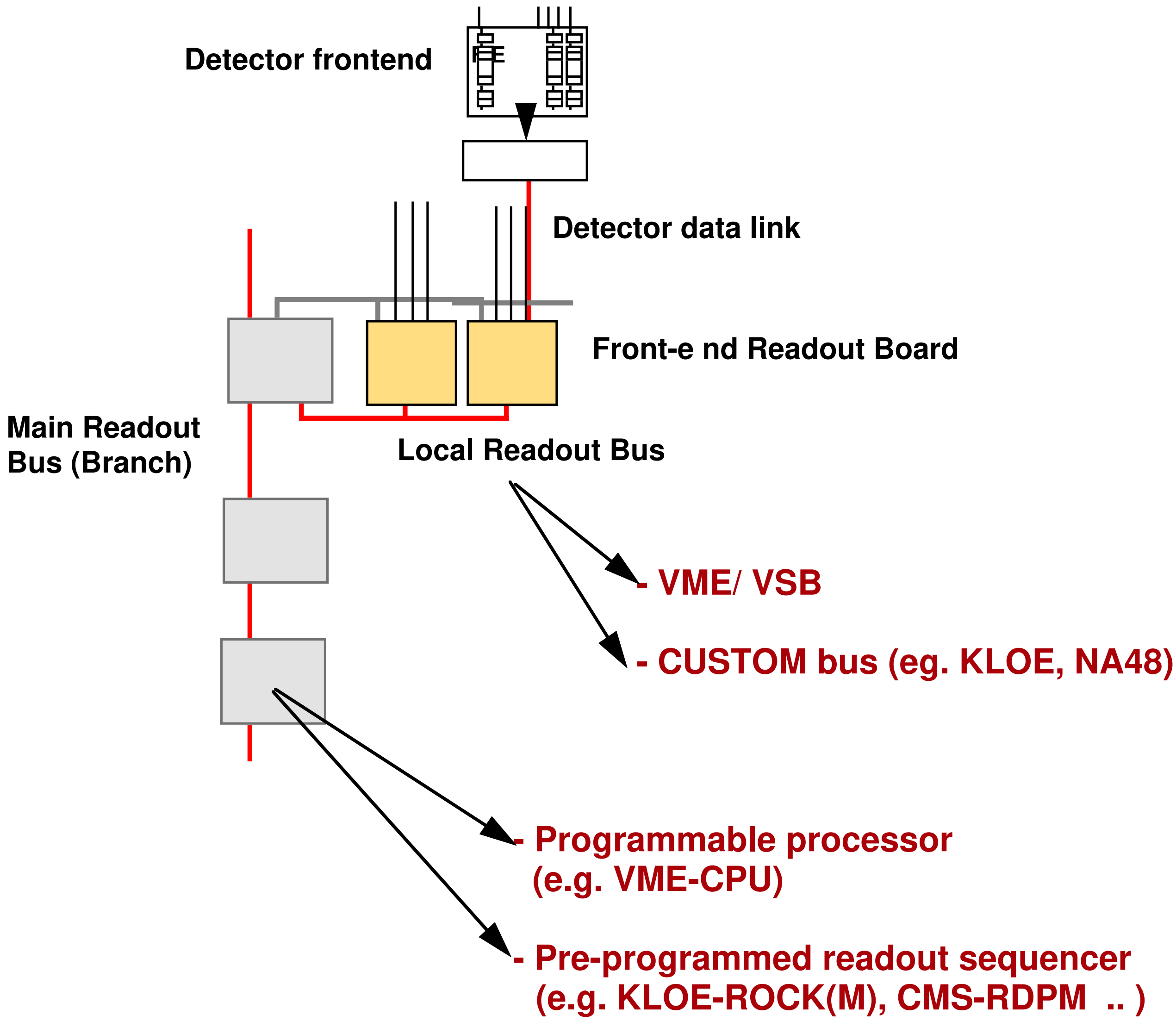


Frontend readout COMPUTING AND COMMUNICATIONS SUBSYSTEMS:

- **Detector frontend electronics.** Preamplifier, shaper, digitizer and the buffers
- **Front-End Readout boad.** Data receiver, processing, formatting boards
- **Readout Crate.** Crate and local control processor system

- **Timing, trigger and control distribution**.
- **Frontend data readout links (analog/digital)**
- **FrontEnd Bus.** Local readout bus (data merging level)
- **Detector control&monitor communication system.**

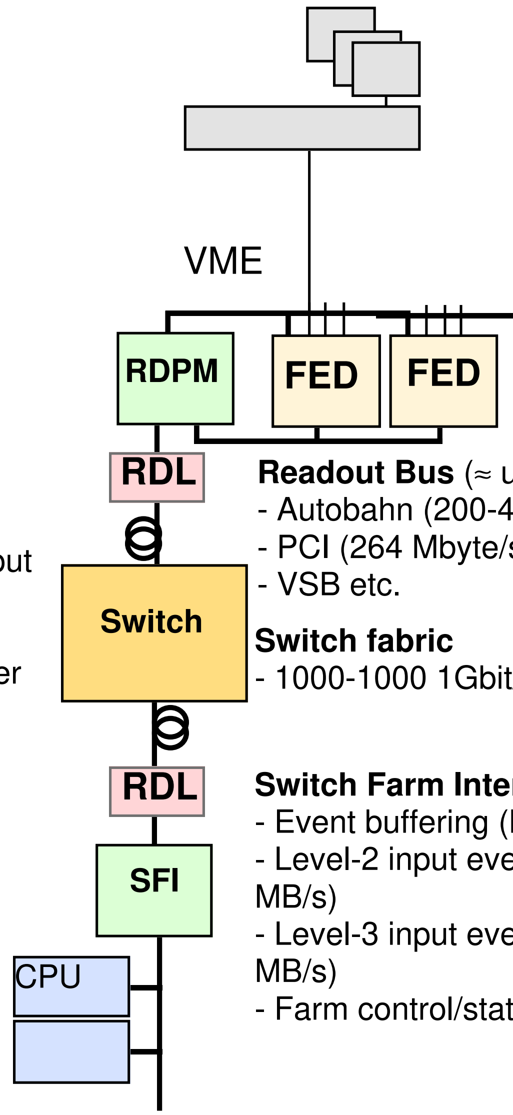
Readout tree and DAQ units



Do we need a standard as in old days ?

The US VME-P and Cern VSC Committee
Ruth Pordes - Fermilab

CMS DAQ basic chain



Detector frontend system

Detector data link
- Digital : 1 Gbit/s
- Analog : 40 MHz

Readout DualPort Memory
- Multi event buffering
- Event builder data source
- (100 MB, 100-400 MB/s)

FrontEnd Driver
- Multi fiber transreceivers
- (Digitizing /processing)
- Event formatting/buffering

Readout Bus (≈ up to 400 Mbyte/s)
- Autobahn (200-400 Mbyte/s)
- PCI (264 Mbyte/s)
- VSB etc.

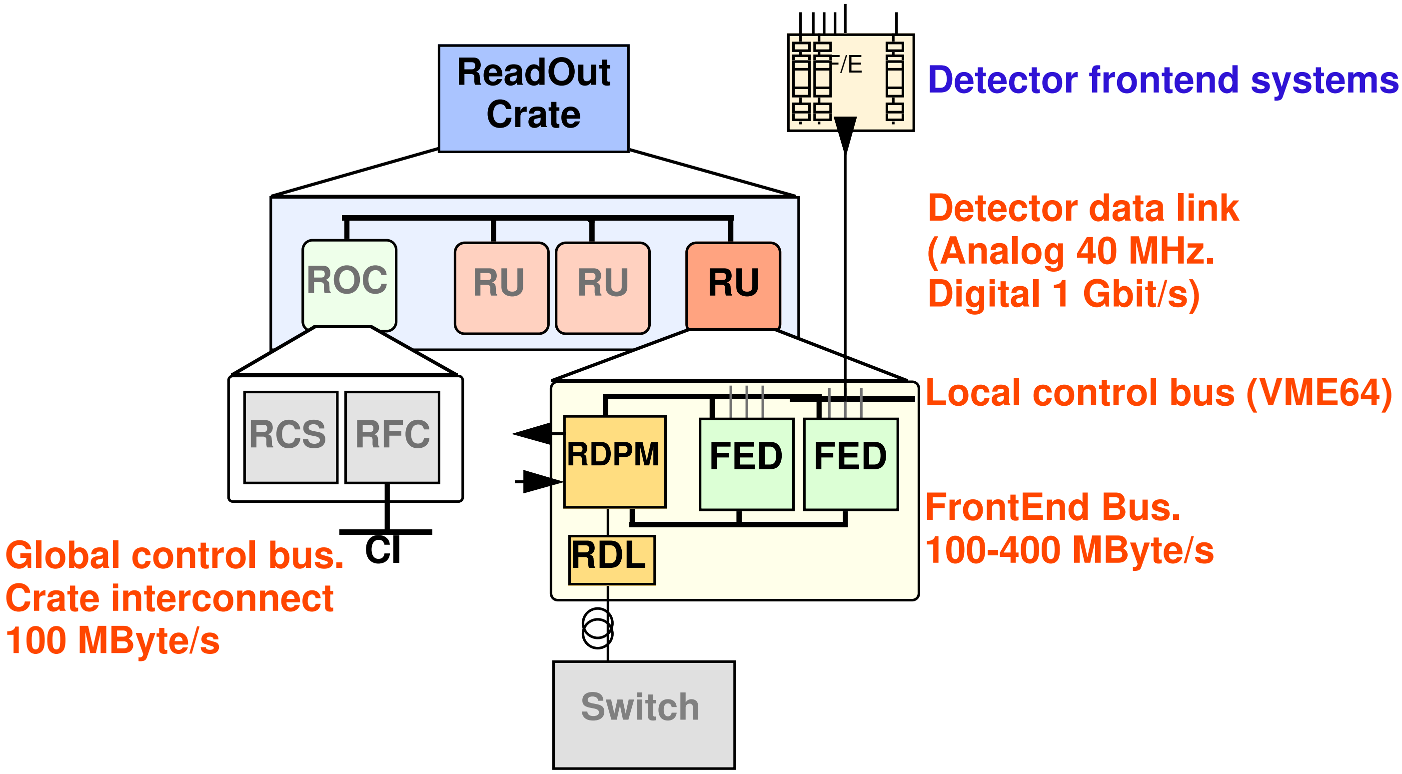
Readout data link
- 500 to 1000 Gbit/s at switch input
- Level-2 RDPM operates at 100 kHz event output rate.
- Level-3 RDPM operates at lower rate (≈1000 to 10000 Hz)

Switch fabric
- 1000-1000 1Gbit/s/port network

Switch Farm Interface
- Event buffering (handling)
- Level-2 input event 100 Hz rate (≈ 20 MB/s)
- Level-3 input event 10 Hz rate (≈ 10 MB/s)
- Farm control/status

Farm
- Multiple CPU workstation (≈ 4000 MIPS)
- Farm output ≈ .1 Hz

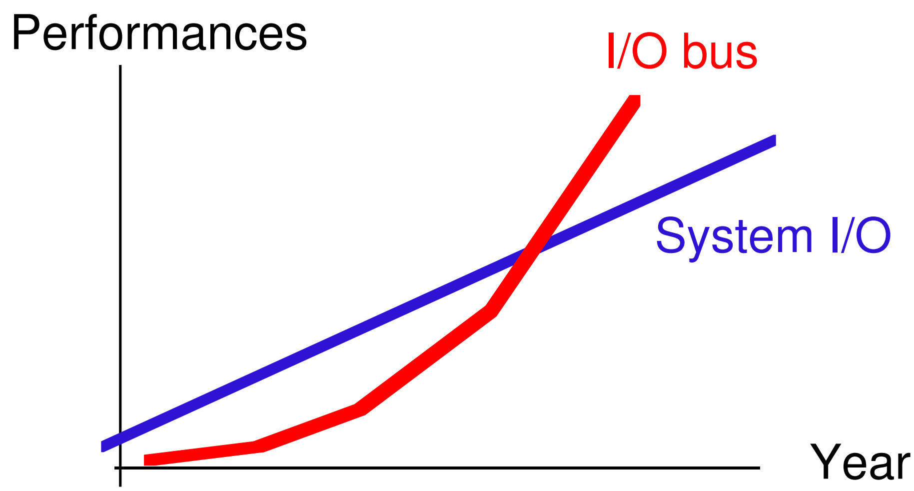
CMS readout crate



ROC Readout Controller
RCS Readout Crate Supervisor
RFC Readout Flow Controller
RU Readout unit
FED FrontEnd Driver
FEB FrontEnd Bus
RDPM Readout Dual Port Memory
RDL Readout Data Link
CI Crate Interconnect

Each RDPM is attached to between one and six FEDs, depending on the local event data sizes and the event builder switch input rate. This system is called Readout Unit (RU). Nearly 2,500 FEDs will be necessary for the readout of all the different subdetectors organized into about 1000 RUs. The standardisation of a common baseline electronics interface at this critical junction will ensure homogeneity throughout the readout architecture, simplifying the tasks of integration and maintenance.

A physical Readout Crate contains several Readout Units and a Readout crate Controller and communication module (ROC). The ROC comprises a Readout Crate Supervisor (RCS) and a Readout Flow Controller (RFC). The specific tasks of the ROC are to ensure the initialisation of the RUs, to monitor their operation during data taking, to handle errors, exceptions and interrupts and also to handle status communication to the central system control.



Software driven protocols are unable to cope with the increased I/O speeds

- Better software ? (Real programmer/Quiche eaters)
- Hardware drivers (KLOE, NA48, CMS...)
    - High level design tools
    -

Frontend readout contributions

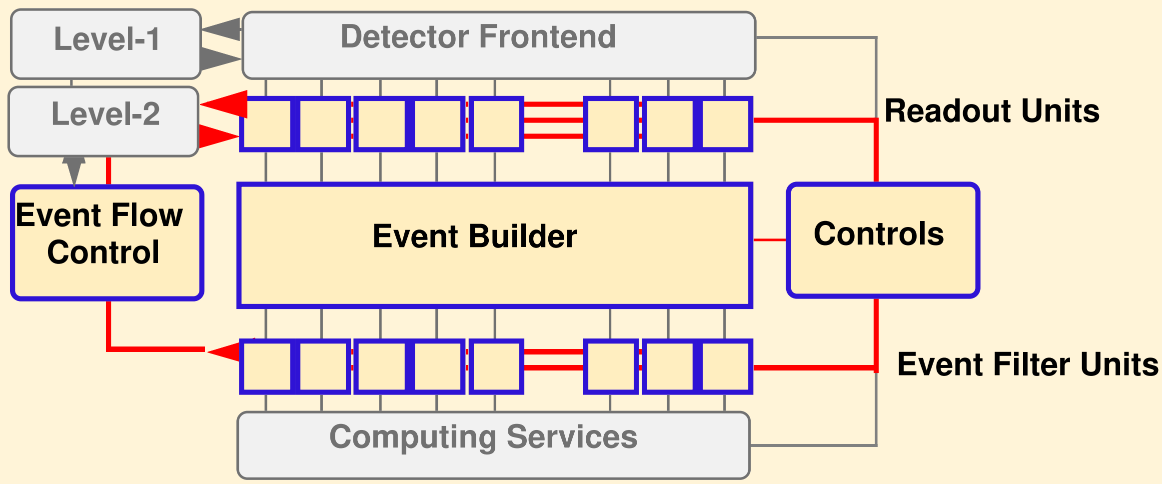
Overview and Performance of FNAL KTeV DAQ System
Tsuyoshi Nakaya - Fermilab

A Dead Time Free Data Acquisition System For the NA48 CERN Experiment
Musa Luciano - Instituto Nazionale di Fisica Nucleare

Level 1 DAQ System for the KLOE experiment
Albero Aloisio - Universita' di Napoli

The US VME-P and Cern VSC Committee
Ruth Pordes - Fermilab

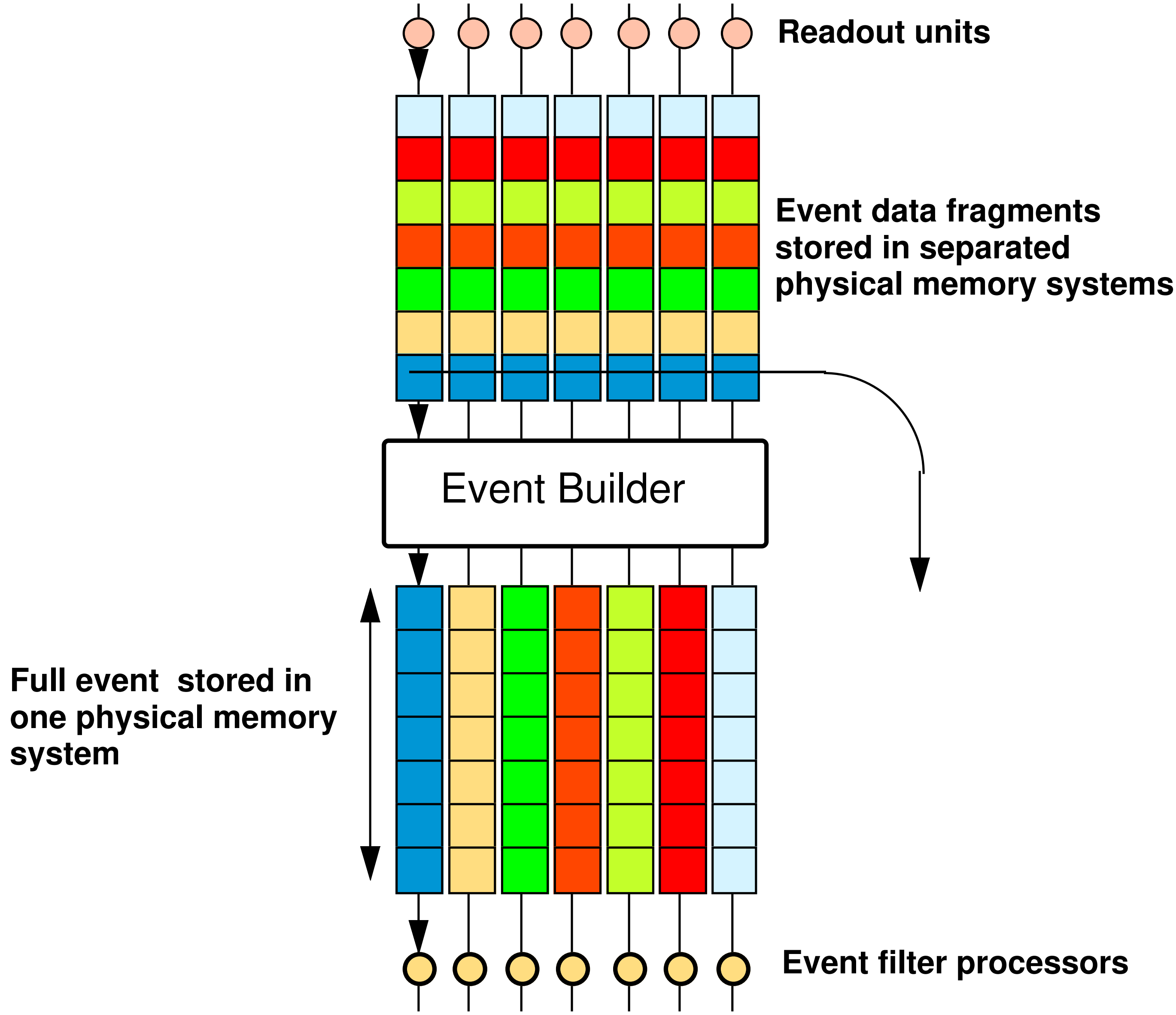
Readout network and event building



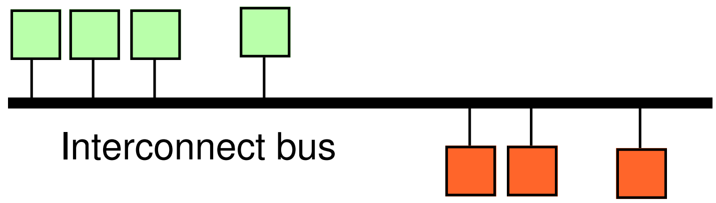
Readout COMPUTING AND COMMUNICATIONS SUBSYSTEMS:

- **Readout unit.** Basic data acquisition subsystem
- **Event filter unit.** High level trigger processing unit (desktop or farm)
- **Event manager.** Event builder scheduler
- **On-line controls.** Initialize, configure, monitor, error handle DAQ

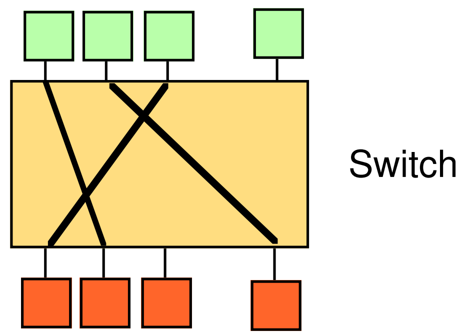
- **Event flow fast controls.** Event manager command distribution to RUs
- **Switch.** N to N port interconnection network
- **Data flow control.** High level DAQ monitoring and error handling
- **Readout fast status.** Back pressure signalling to level-1
- **Farm fast status.** Event building and processing information


Readout units
Event data fragments stored in separated physical memory systems
Event Builder
Full event stored in one physical memory system
Event filter processors

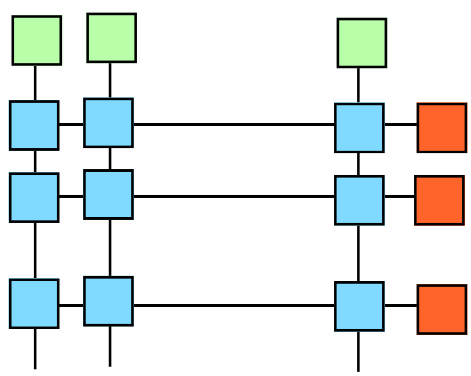
(Parallel) Readout and Sequential event building
(H1, NA48,LEP)



Parallel readout and parallel event building
(KLOE, CLAS, ..)



Parallel readout and parallel sequential event building
KTeV(DART)



Overview and Performance of FNAL KTeV DAQ System
Tsuyoshi Nakaya - Fermilab

Extending DART to meet the Data Acquisition Needs of Future Experiments at Fermilab
Ruth Pordes - Fermilab

Event Building in Future DAQ Architectures Using ATM Networks
David D. Doughty Jr. - Christopher Newport University

Studies on Switch-based Event Building Systems in RD13
R. Spiwoks/RD13 - CERN

A Millemium Approach to Data Acquisition: SCI and PCI
Hans Muller - CERN

Triggering and Event Building Results using the C104 Packet Routing Chip
D. Francis - Boston Universtiy

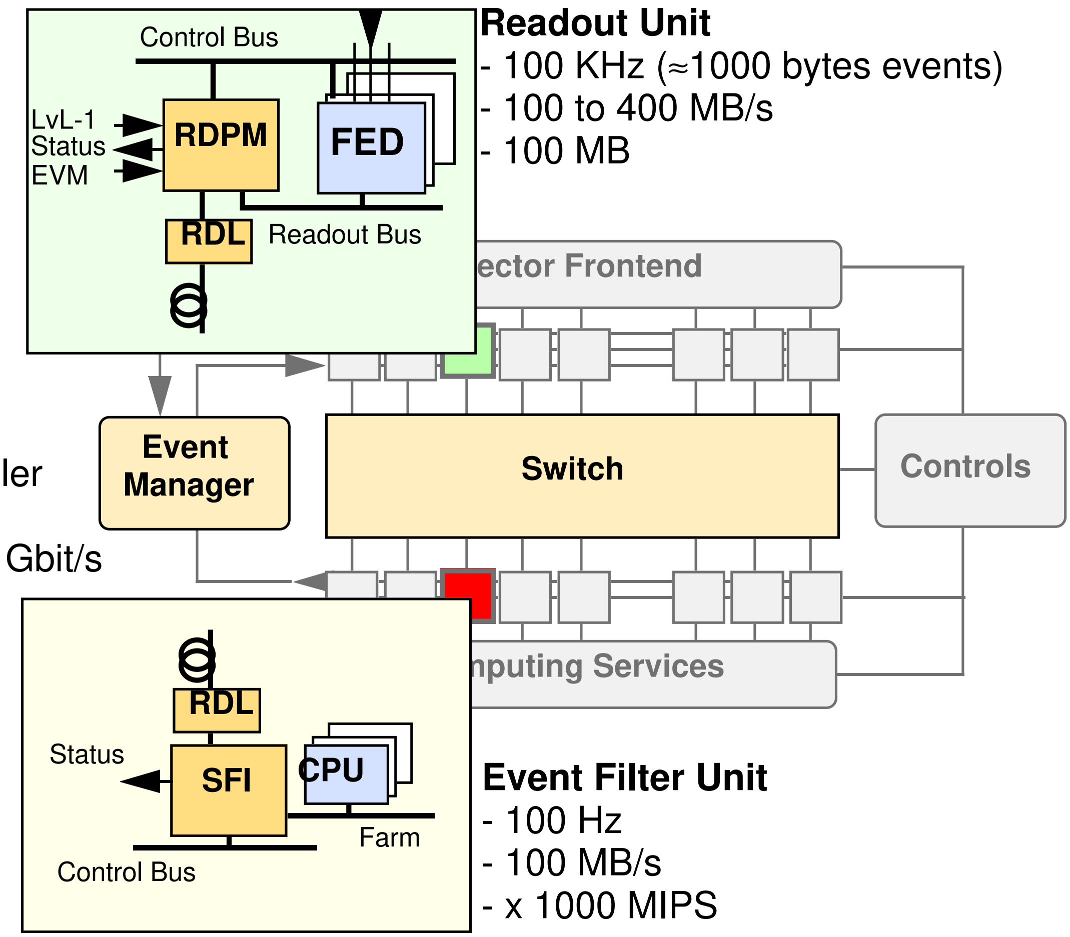
The CMS data acquisition architecture
Sergio Cittolin - CERN

The DAQ and Trigger system of the ATLAS experiement at the LHC
Ralf Spiwoks/RD13 - CERN

The Alice Data Acquisition System
Pierre Vande Vyvre - CERN

KLOE	FDDI.	16•16 100 Mbit/s	50 Mbyte/s
CLAS	ATM.	16•16 155 Mbit/s	50 Mbyte/s
DART	VME matrix, ATM		300 Mbyte/s
ALICE	xxx	32•32	1 Gbyte/s
ATLAS	xxx	200•200	5 Gbyte/s
CMS	xxx	1000•1000	50 Gbyte/s

CMS DAQ basic units

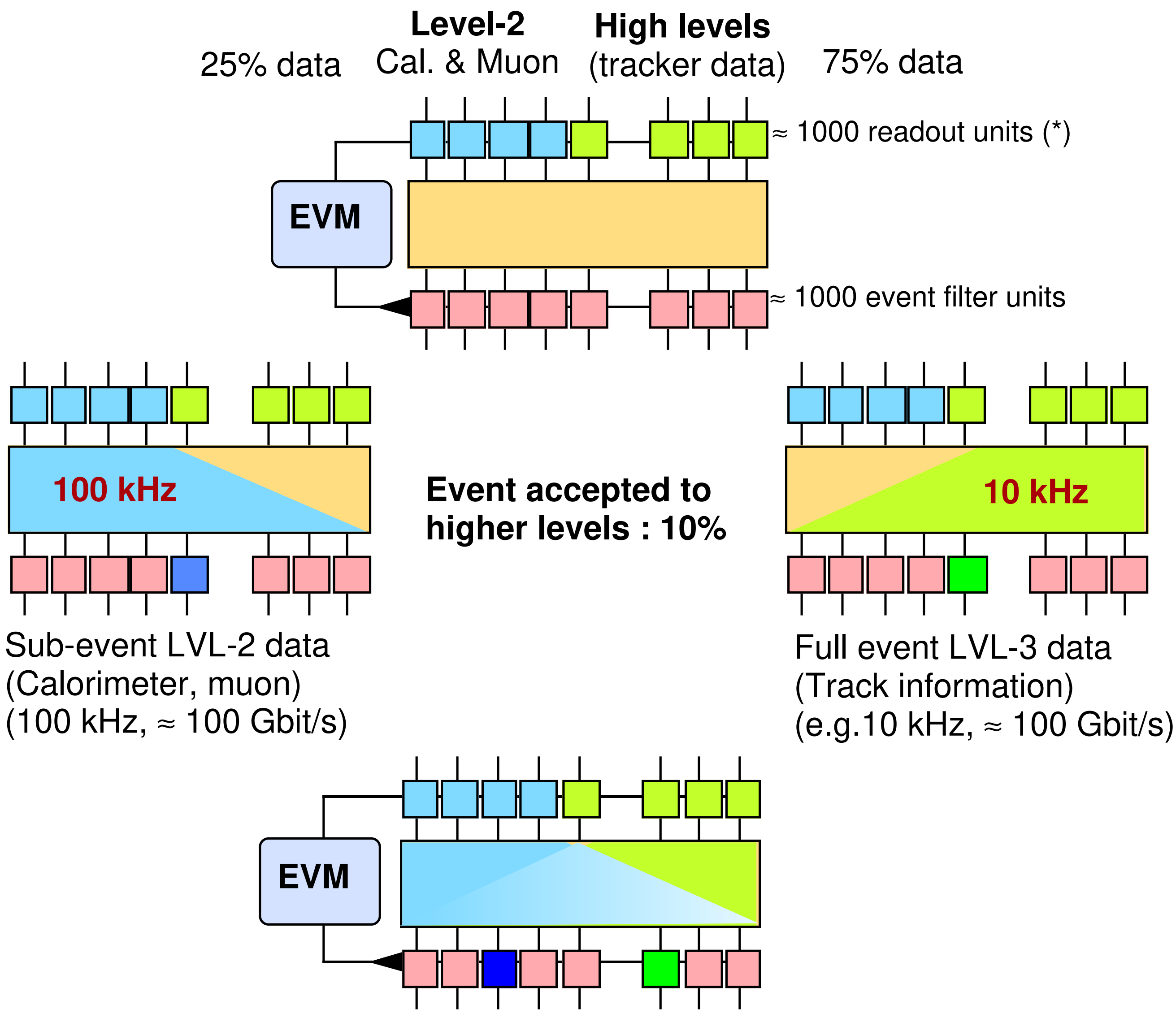


Readout Unit
- 100 KHz (≈1000 bytes events)
- 100 to 400 MB/s
- 100 MB

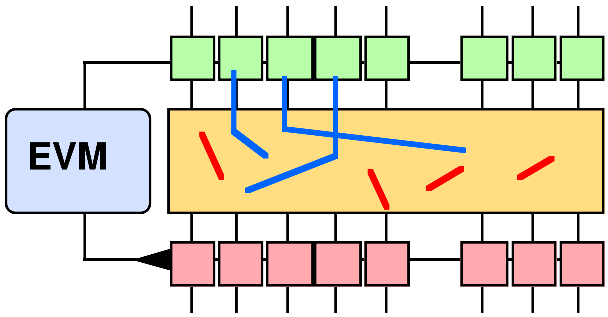
Event Manager
- 100 kHz scheduler

Switch
- 1000-1000. 500 Gbit/s

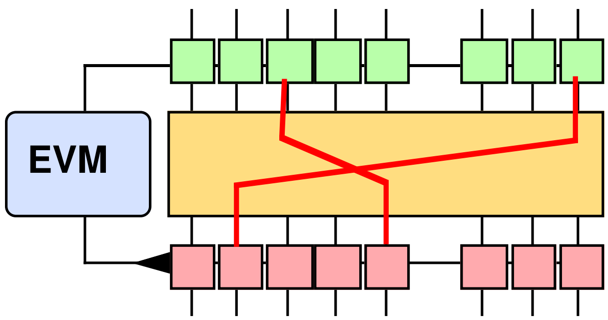
Event Filter Unit
- 100 Hz
- 100 MB/s
- x 1000 MIPS



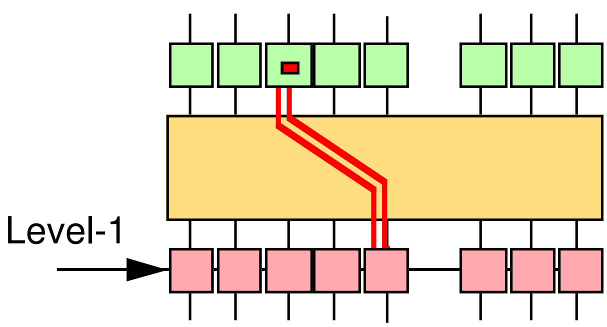
Less aggregate bandwidth, e.g. 100 Gbit/s is needed to handle 100 kHz event rate



Autorouting (PACKET SWITCHING)
- E.g. ATM and FCS (high classes)
- Any size event fragments
- Adapter layer is complex
- Large system performance ? Latency?
- Data congestion controls ?
(traffic shaping, back pressure.)



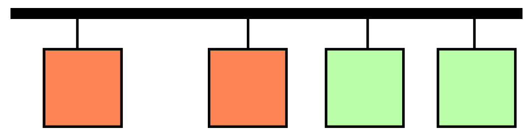
Data channel (CIRCUIT SWITCHING)
- E.g. FCS, HIPPI, custom
- Large size fragments (multi-events)
- Cross bar like switches.
Open connection and send data
- Channel auto selection or from central system
(e.g. barrel switch)
- Large system cross bar ?



Multi-port memory.
- e.g. MPP architecture, SCI
- No event flow control. Move data only when needed

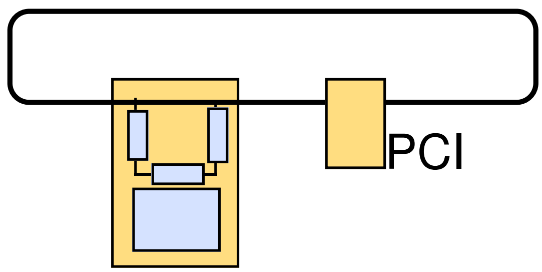
- Large system feasible? Latency?

ORIGINAL SCOPE
- Multi-processor memory bus
- HEP, MPP industry

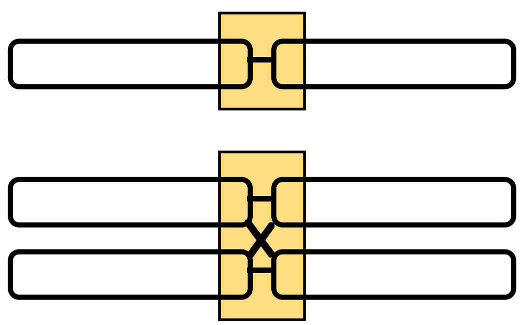


- Read-Write protocol (100 MB/s to 1GB/s)

- Rings and interfaces

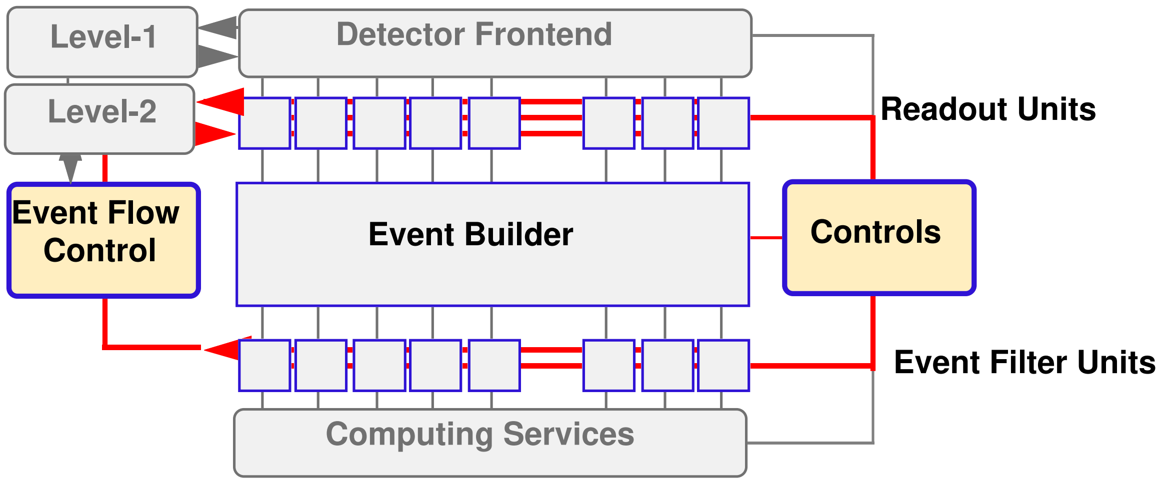


- Bridges & Switches



APPLICATIONs
- Multiprocessor internal bus
- Fast peripheral interconnect
- Crate interconnect

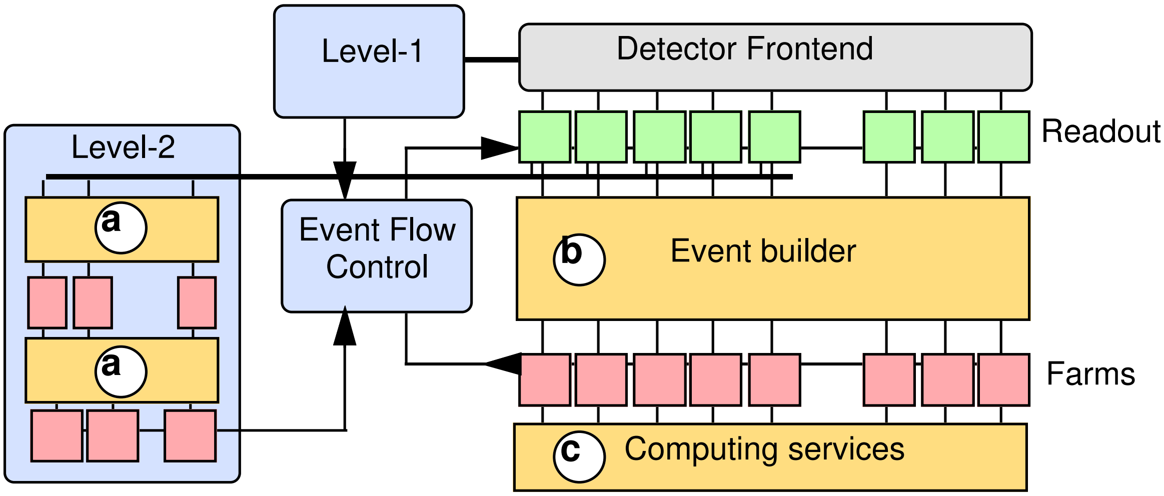
A Millemium Approach to Data Acquisition: SCI and PCI
Hans Muller - CERN



APPLICATIONs

- Multiprocessor internal bus
- Fast peripheral interconnect
- Crate interconnect

Switches in DAQ



a) LEVEL-2 TRIGGER SYSTEMS.
Many-to-few port switches, routers, 'small' switches
- Industry IC components
- Custom systems

b) EVENT BUILDER (and HIGH LEVEL TRIGGERS).
Large switches (traffic shaping, flow control etc.)
- Commercial switches (ATM like and Fiber Channel)
- Custom design **if necessary**

c) COMPUTING SERVICES.
Resource network. Monitoring, mass storage and LAN connections
- Anything will be popular, probably switch based

Level-3/OS contributions

The BaBar Trigger, Readout and Event Gathering System
J. Frederic Kral - LBL

Design and Simulation for Real-Time distributed processing system
Iosif Legrand - DESY

A Scalable Data Acquisition System Using Transputers and the Chorus Operating System
D. Francis -

Advanced Operating System Technologies
Fabio Riccardi - CERN

Software and controls contributions

The use of the SNMP (Simple Network Management Protocol) Implementing Run and Data Flow Controls in the KLOE experiment.
Maria L. Ferrer - Frascati, Italy

The new ZEUS run control system: An exercise in modularity.
Jaroslaw Milewski - Hamburg University

On the Relevancy of Efficient, Integrated Computer and Network Monitoring in HEP Distributed Online Environment
Diego Carvalho - CERN

Interprocess and Interprocessor Data Flow in the KLOE Data Acquisition System
Harry Beker - CERN

Evaluation of DAQ Performance
Yoshiji Yasu - KEK

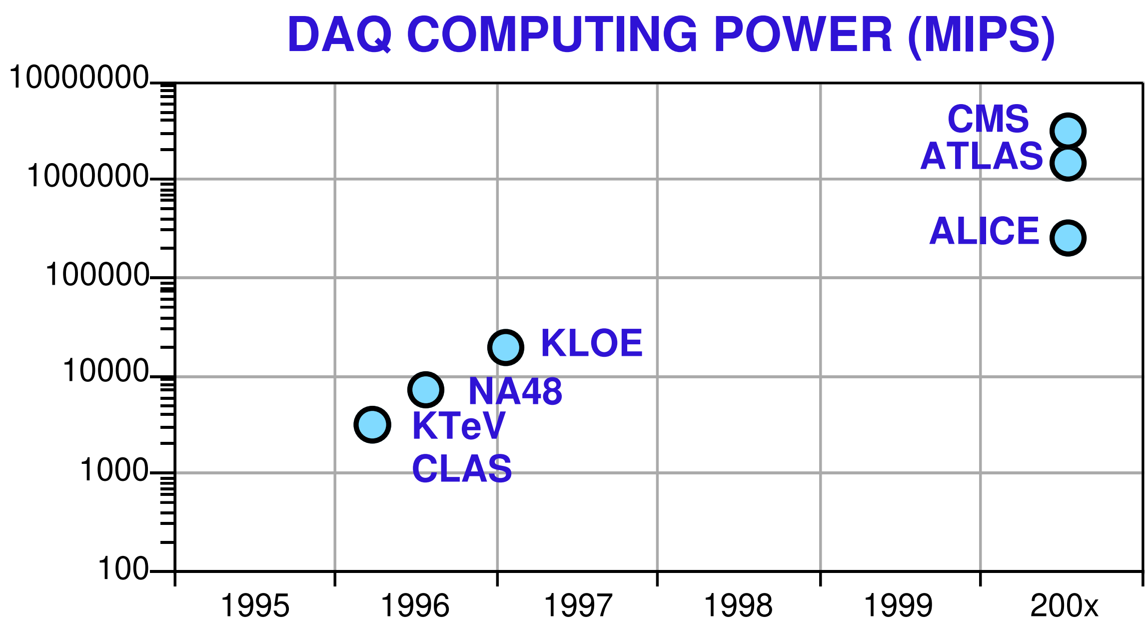
Experience on using Databases in the Aleph Data Acquisition and Control System
Pere Mato - CERN

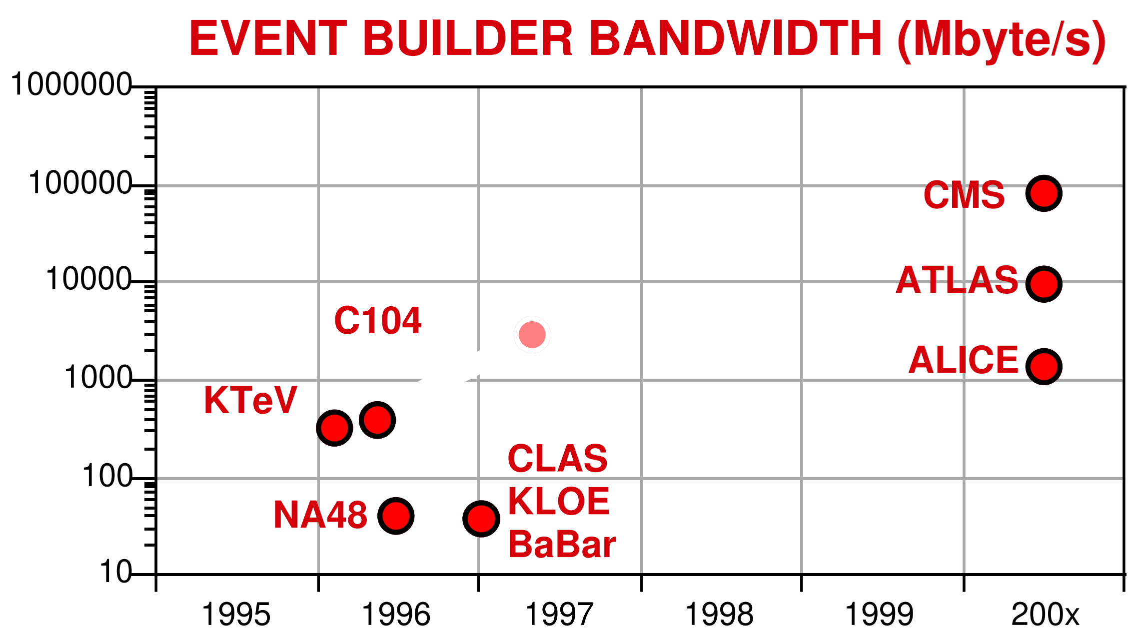
Event builder and event filter simulation languages:
C++, μC, MODSIM

Four decades / four DAQ eras

	MINI 70	MICRO 80	DESKTOP 90	NETWORK 00
TRIGGER	Standard	Custom	Custom	Custom
FRONTEND	Standard Wired	Generic PAL	Custom FPGA	Custom VLSI
READOUT	CAMAC	FB-VME	VME	VMExx
STRUCTURE	Tree	Bus	Bus	Link
EVENT BUILDER	Sequential	Parallel Sequential	Parallel Sequential	Parallel Parallel
OS	Custom	None/RT	UNIX	POSIX...
LANGUAGE	Assembler	Fortran Assembler	C Fortran	Object O. C++ Script
DAQ package	Generic	Custom	Custom	Custom
MASS STORAGE	MTape	MTape	MTape	MTape?
SOFTWARE	simple	easy	complex	+complex?
HARDWARE	Expensive	affordable	cheap	cheaper

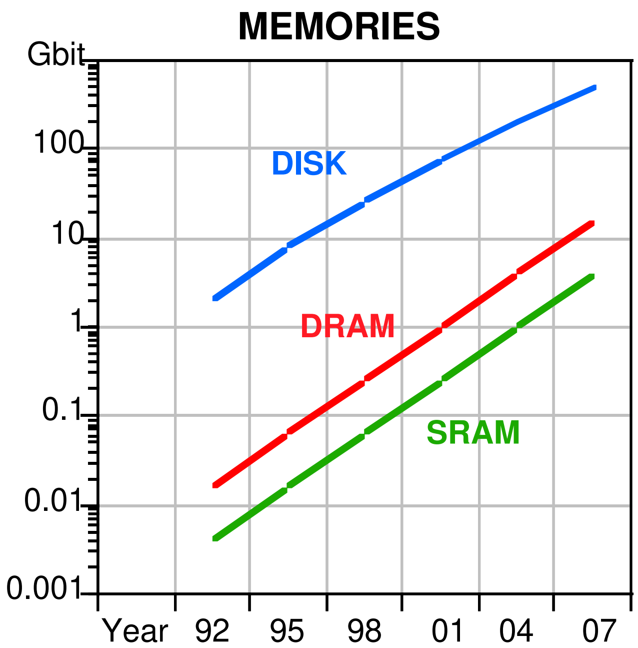
DAQ present and future performances

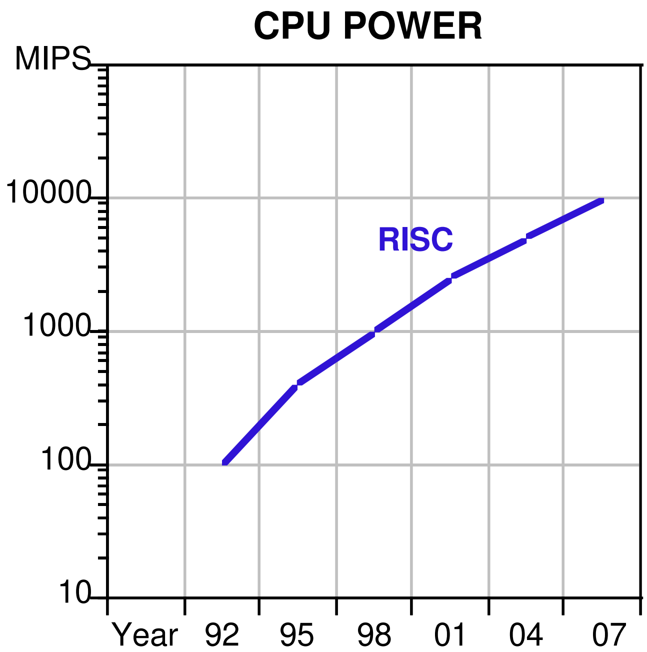


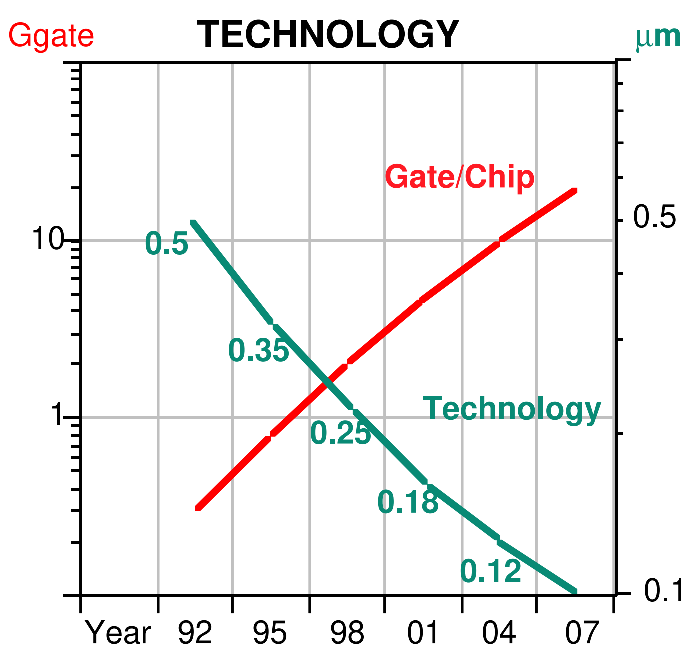


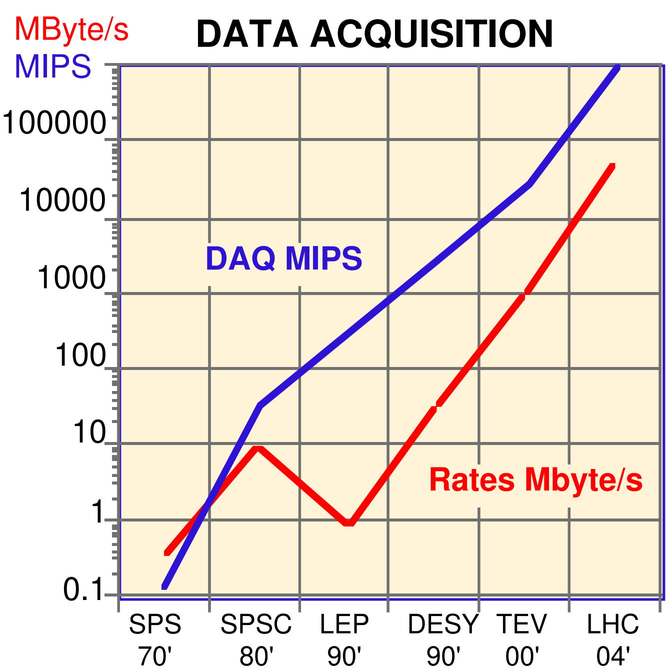
Technology & DAQ trends

from Semiconductor Industry Association - Semiconductor Technology Workshop Conclusions - March '93

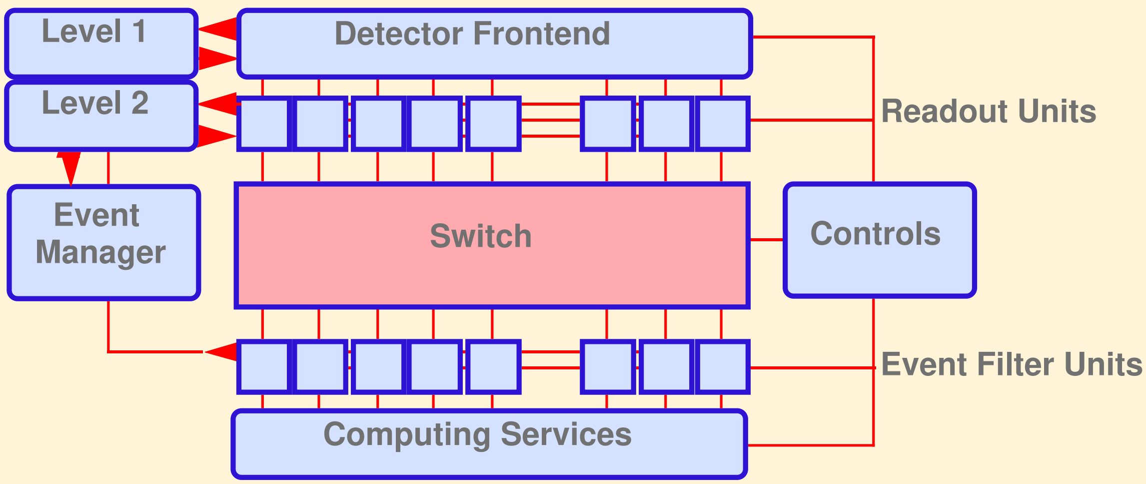








Conclusion

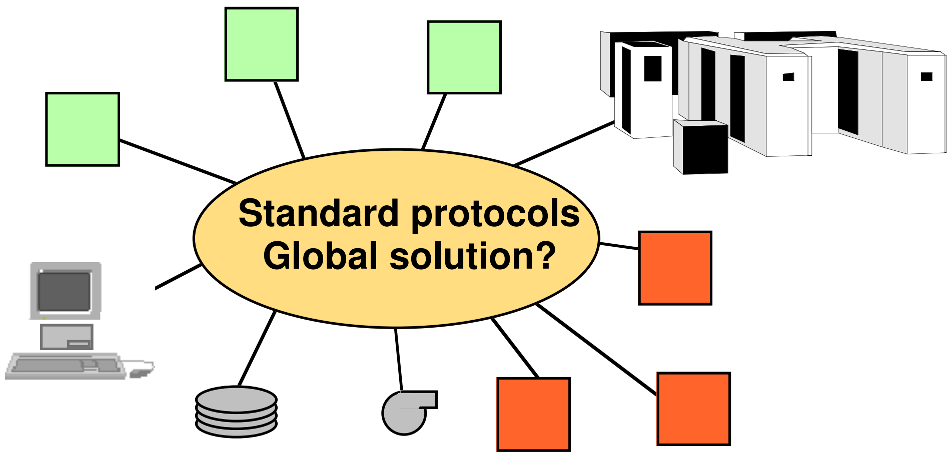


The next generation of Data Acquisition systems can be implemented only by the intimate integration of computing and communications technologies

Requirements

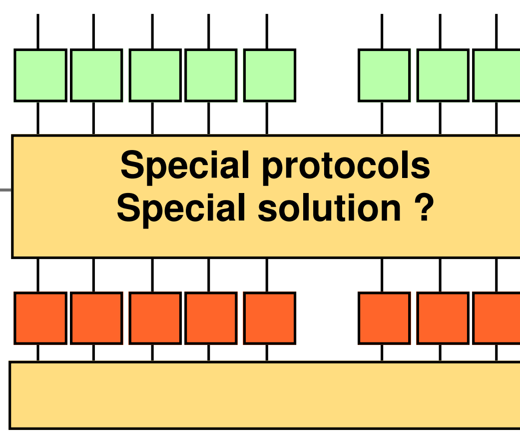
10 to 100 MB/s xx•x event builders

• CDF, D0
• KEK, SLAC
• EUROBALL, CEBAF, KLOE
• ALICE



1 to 100 GB/s xxxx•xxx event builders

• ATLAS
• CMS



Some switch products in 1995

ATM Asynchronous Transfer Mode
(SONET speeds : 155, 622, 1244, 2488 Mbit/s)
- 155 Mb/s components (switches and adapters) available (all scalable)
  ALCATEL 2*2 155 Mbit/s, FORE 155 Mb/s
  AT&T Phoenix 2*2 320 Mbit/s, IBM PRIZMA 16*16 400 Mbit/s
- Small switch fabrics available (4*4, 32*32)
- Interfaces available (PCI)

FCS Fiber Channel System
(FCS speeds : 133, 266, 531, 1062 Mb/s)
- FCS optoelectronics interfaces 266-1062 Gbit/s available
- FCS Fabric (e.g.1 Gbit/s 8*8 scalable up to 192 by AnCor)
- Interfaces available (PCI)

OMI/HIC (Line of switches 200, 1000 and 3000 Mbit/s)
- C104 100 Mbit/s 32*32 node chip. Large systems will exist

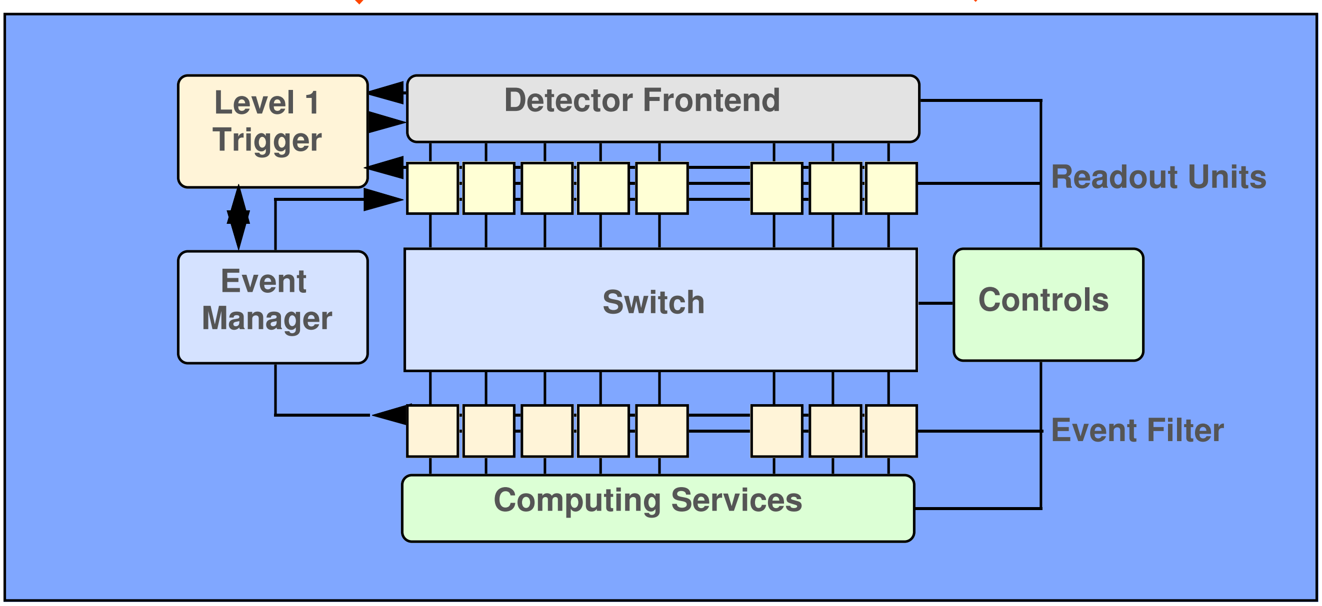
RACEWAY from Mercury MPP systems.
- 16*16 160 Mbyte/s VME backplane cross bar switch scalable to large systems (1000 processors)
- Chip set for port interfacing

Cross bar switch nodes (16*16, 32*32) running at Gbit/s speeds are available in the market today.

Summary

Average event size	≈ 1 MByte
Level-1 Maximum trigger rate	100 kHz
No. of Readout units (200-5000 Byte/event)	1000
Event builder (1000-1000 switch) bandwidth	≈ 500 Gbit/s
Event filter computing power	≈ 5 10^6 MIPS
Data production	≈ TByte/day
No. of readout crates	≈ 300
No. of electronics boards	≈ 10000

CUSTOM DESIGN



COMMODITY

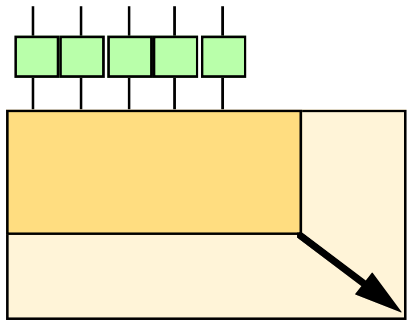
Answer to CHEP organizers

This includes R&D work on future data acquisition systems, Switch designs and development in various technologies, use of special purpose processors in DAQ systems, computer modelling of DAQ systems. We expect to hear about interesting aspects of current DAQ systems which are/will be relevant to Computing for the next Millenium. We expect to hear much about specific R&D projects which are ongoing and ideas for platform independent DAQ.

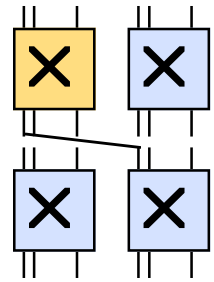
This includes everything from low level hardware triggers to high level software filters. We expect to hear about dedicated hardware
triggers, software trigger issues, use of neural nets in trigger systems and topics on modelling and simulation of triggers.

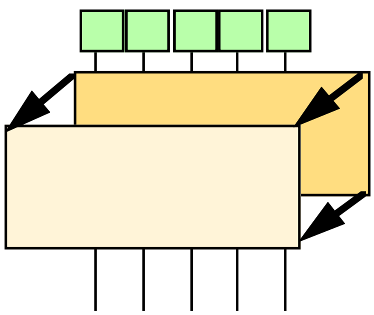
This includes slow control of high energy physics and nuclear physics experiments, commercial systems, accelerator and beam control system topics, and expert systems.

Switch scaling dimensions

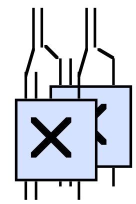


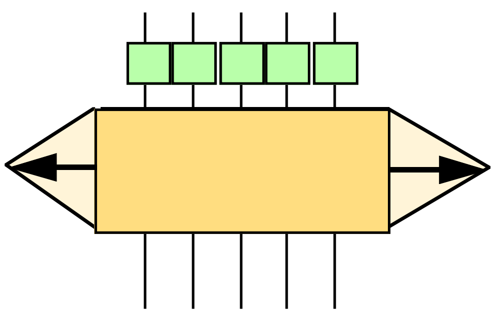
Number of ports



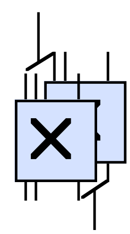


Port speed
Twinning the switch with.
Bandwidth doubled





Aggregate bandwidth
Increase internal resources:
buffering, path etc.



E.g. PRIZMA-IBM 16*16 400 Mbit/s (6.4 Gbit/s)

Scaling of features is embedded in the design

CMS switch performance minimal requirements

- Virtual level-2 ≈ 25% of event data
- Virtual level-2 rejection factor ≈ 0.1
- Switch load for acceptable latency ≈ 30%

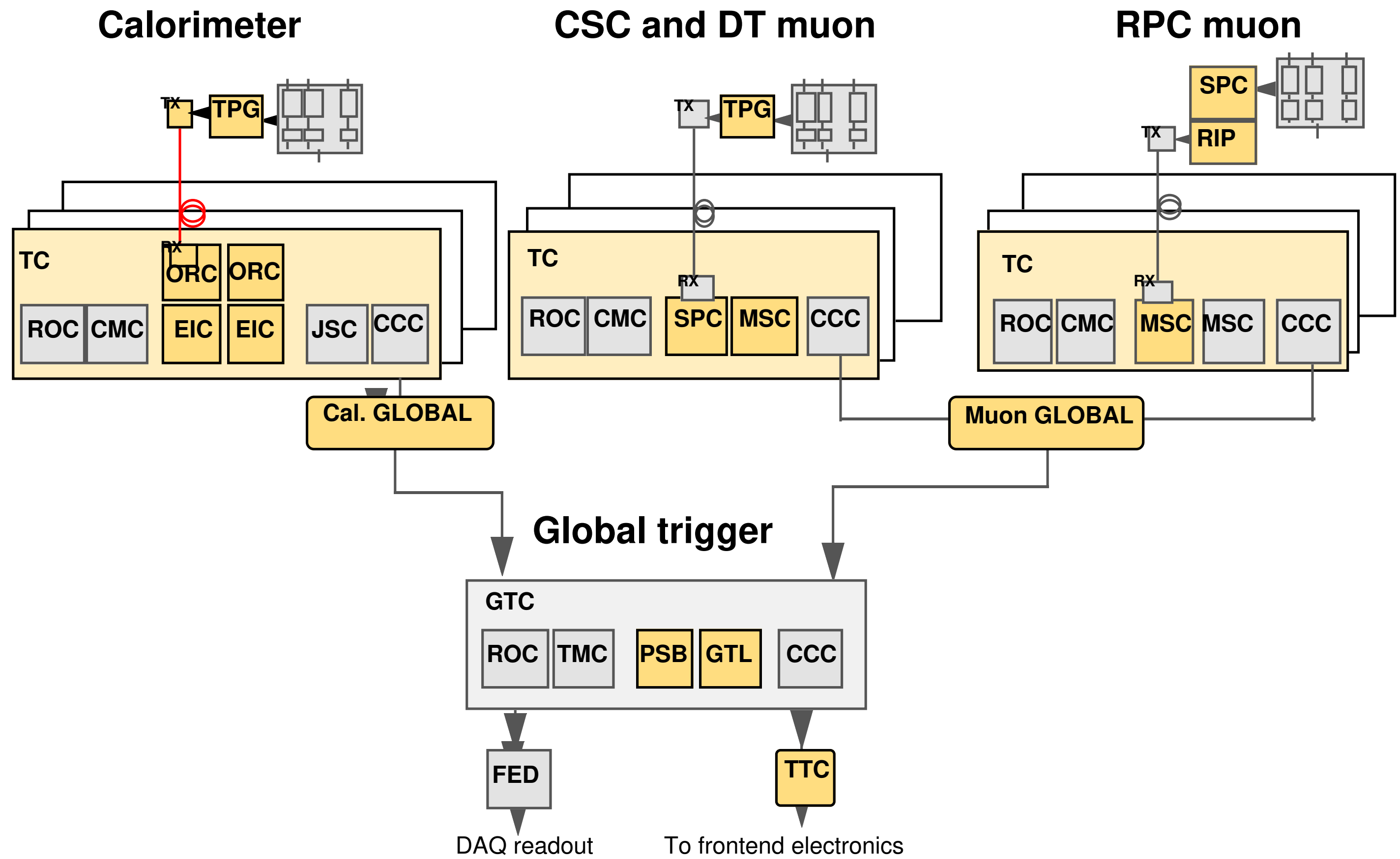
1000 * 1000 port switch with 500 Mbit/s port speed

Still much work to do :

- Simulation of large switches
    - Number of ports / Latency / Switch load
    - Switch protocols
- Classification and evaluation of high trigger levels algorithms and the required farm computing power
- Identification and definition of functionalities of all event builder components
- Integration of commercial switches in DAQ prototypes. Choice of technologies and switch fabric design.

he present evaluation of the readout network is based on the assumption of a large switch fabric (1000-1000) at low speed. If higher peeds will be available, the dimension of switch and so the number of parts in the readout network will be partially reduced. nother crucial item is the cost of high speed (I Gbit/so) optical links, a technology emerging nowadays and not yet developed for a rge market.

CMS level-1 trigger systems



General
TC Trigger Crate
CCC Clock and Control Card
ROC Monitor and DAQ processor
CMC Crate Monitor Card
FED Readout FrontEnd Driver
TPG Trigger Primitive Generator
Calorimeter trigger
ORC Optical Receiver Card
TX Optical transmitter

RX Optical receiver
EIC Electron Isolation Card
JSC Jet Summary Card
CSC and DT trigger
SPC Sector Processor Card
MSC Muon Sorter Card
TPG Trigger Primitive Generator
Mean timer (DT)
Track segment finder (CSC)

RPC trigger
SPC Sector Processor Card
RIP RIng Processor
MSC Muon Sorter Card
Global trigger
GTC Global Trigger Crate
PSB Pipeline Synchronizer and Buffer
GTL Global Trigger logic
TTC Timing, Trigger and Control

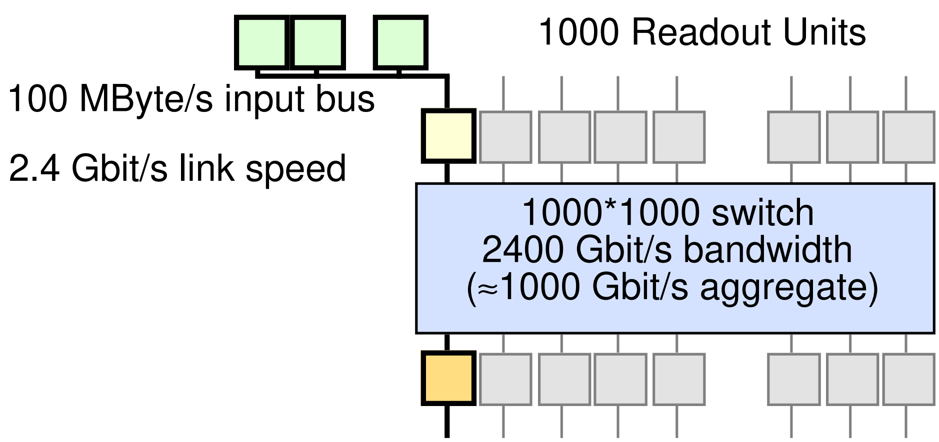
Event building and high level triggers

Two ways may be considered to build events for high level triggers:

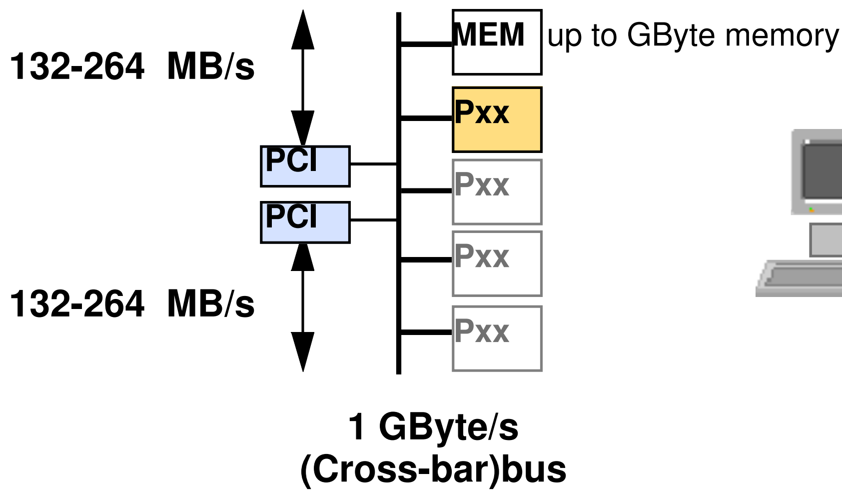
1) The FULL EVENT DATA are trasferred to the event filter and then processed

2) SELECTED DATA (e.g. calorimeter and muons) are sent first, then the process will continue according to the result of successive analysis

Average event size	**≈ 1 MByte**
Level-1 trigger rate	**100 kHz**
No. of Readout units (≈ 1 kByte/event)	**1000**
Required switch aggregate bandwidth for FULL EVENT BUILDING AT 100 kHz	**1000 Gbit/s**



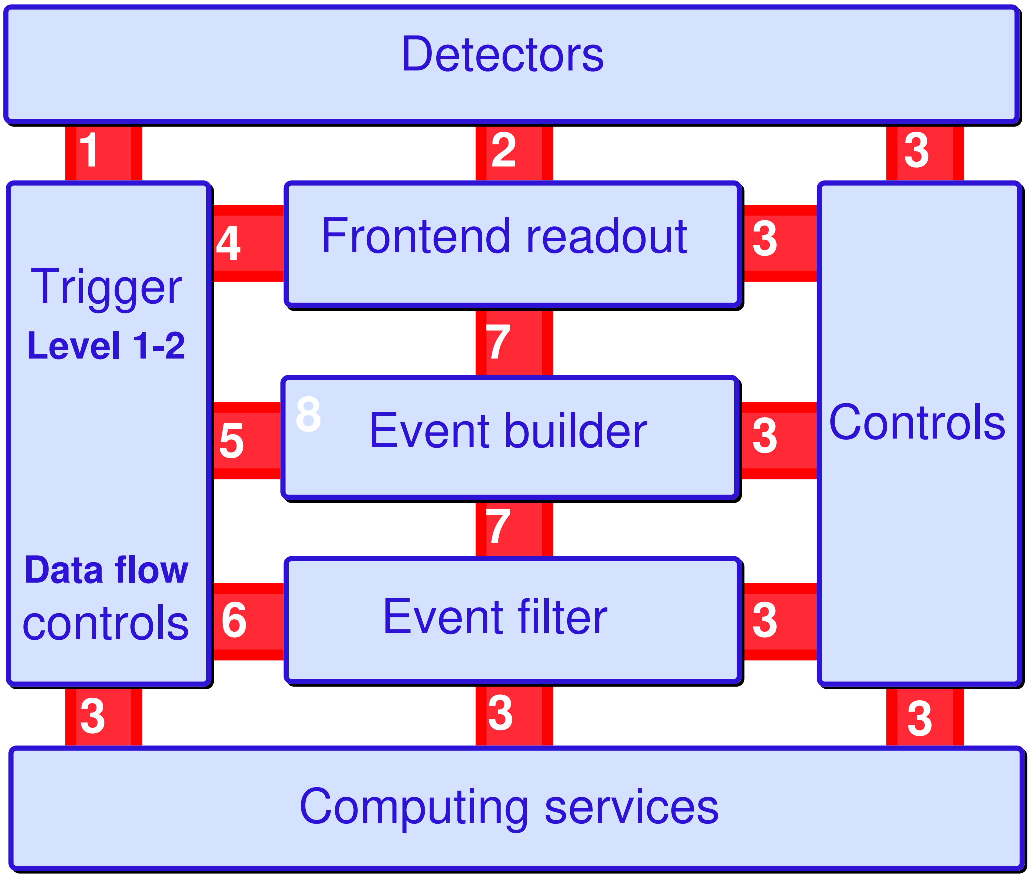
Desktop multiprocessor architectures



Future desktop internal architecture ?

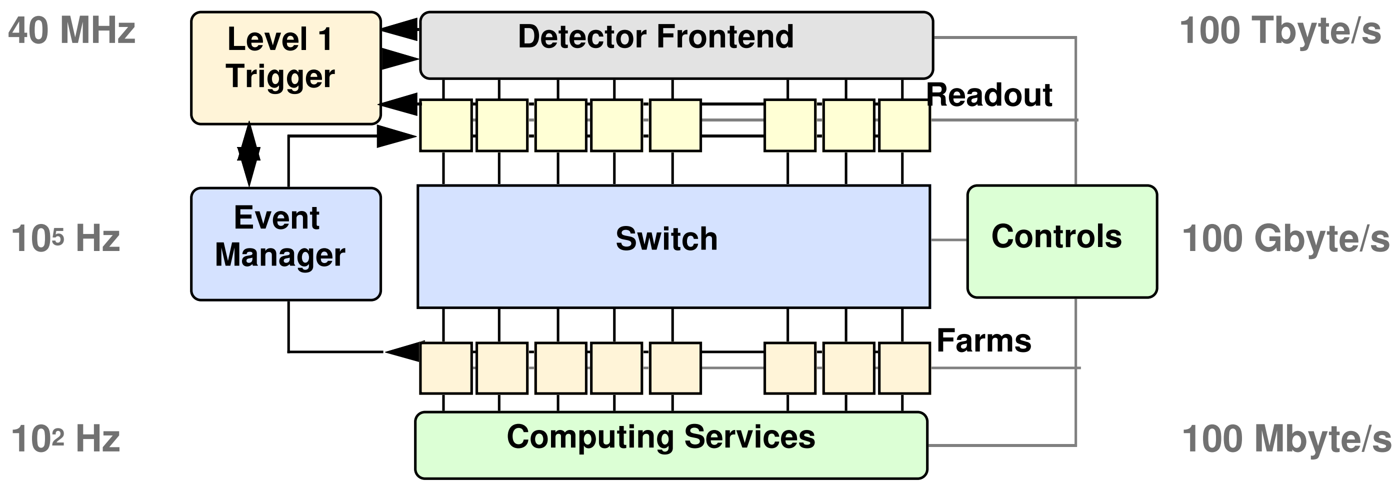
- High performances (winning architecture ?)
- Standard interfacing (PCI?)
- Line of products up to years 2000 ?
- Common architecture from small to large systems
- Low cost, high quality

Trigger and Data Acquisition
computing and communications infrastructures



1) Trigger data readout and fast control signals
2) Detector data link
3) Multi-processor/crate interconnection systems
4) Data flow control and synchronization
5) Level-2 RoI data path
6) Farm and high level trigger status system
7) Readout links
8) Readout network for event builder

CMS data acquisition basic structure



Technology ansatz

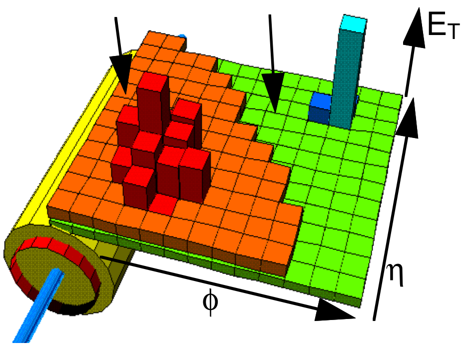
- The CPU processing power increases by a factor 10 every 5 years (at constant cost)

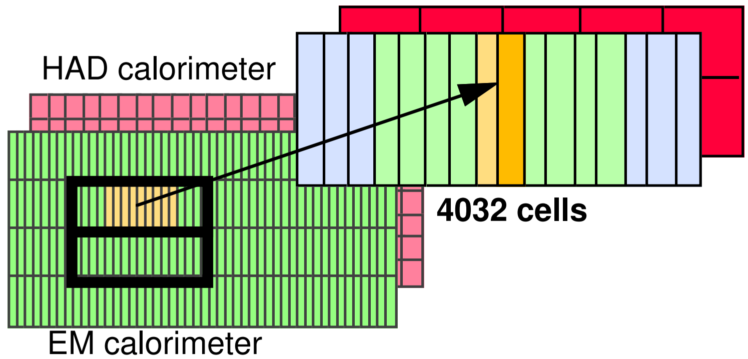
- The memory density increases by a factor 4 every two years (at constant cost)

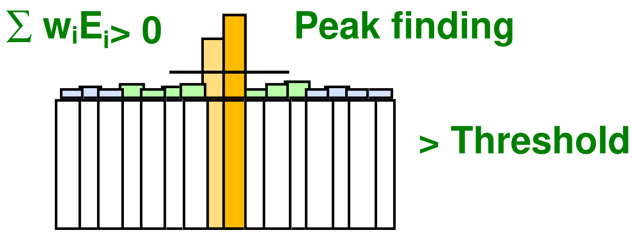
- The 90's is the data communication decade

The high rate at which proton-proton interactions will occur (once every 25 ns) and the physics requirements impose severe constraints on the system. The ability to produce physics results are very dependent upon the DAQ system's capability to acquire data at a high rate and to select the most interesting events to be saved for analysis. This selection is done in multi-level "trigger", which has to reduce the event rate by a factor of 10^{-6} or smaller.

CMS calorimeter level-1. Isolated electron
(peak finding algorithm)



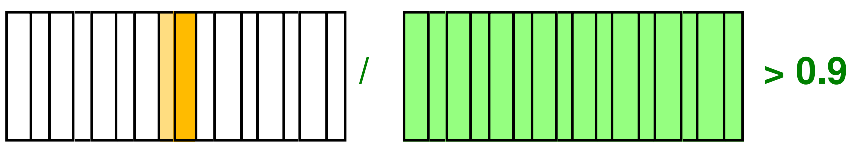




E_t cut

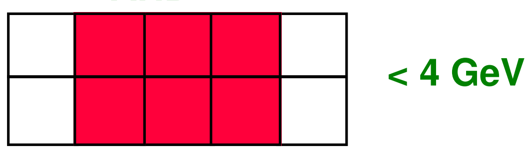
AND

EM isolation



AND

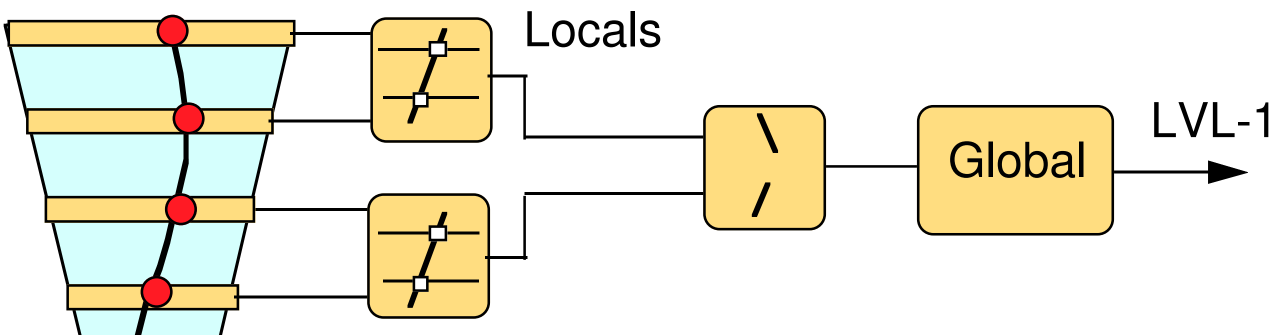
HAD longitudinal and transverse cut



ISOLATED ELECTRON

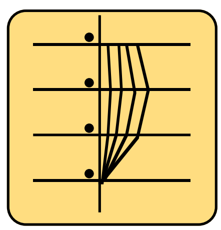
Trigger granularity (Dh * Df)		No.of trigger towers
ECAL : |h| ≤ 2.1	0.044 * 0.174	112 * 36 = 4032
|h| > 2.1	0.087 * 0.174	1008
HCAL :	0.174 * 0.174	162

CMS level-1 muon trigger



- Segment recognition
  - Cone coincidence (RPC)
  - Mean timer (Tube)

  or
- Logic mask



- Track momentum
  - Coincidence matrix
  - Logic mask

- Content addressable memories
- Matrix logic (ASIC, Gate array...)

DAQware

LANGUAGES and operating systems for:
- Microcontrollers and embedded processors
    - I/O sequencers
    - Data flow controls
    - Detector controls
- Desktop development
    - Applications
    - On-line monitoring
    - User interface
- Farm
    - Event filter, calibration, analysis

TOOLS for:
- Group work orchestration
- Concept design
    - Prototyping, simulation, design and synthesis
- User interface
- Data base and documentation
- Quality and Maintenance

....

Hardware cost / Software cost

Platform independent software and freedom

Individual creativity (easy to write code environment)

Abstraction and reality