Low noise charge amplifiers in submicron CMOS

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Outline

I. Design methodology for low noise preamplifiers in submicron CMOS

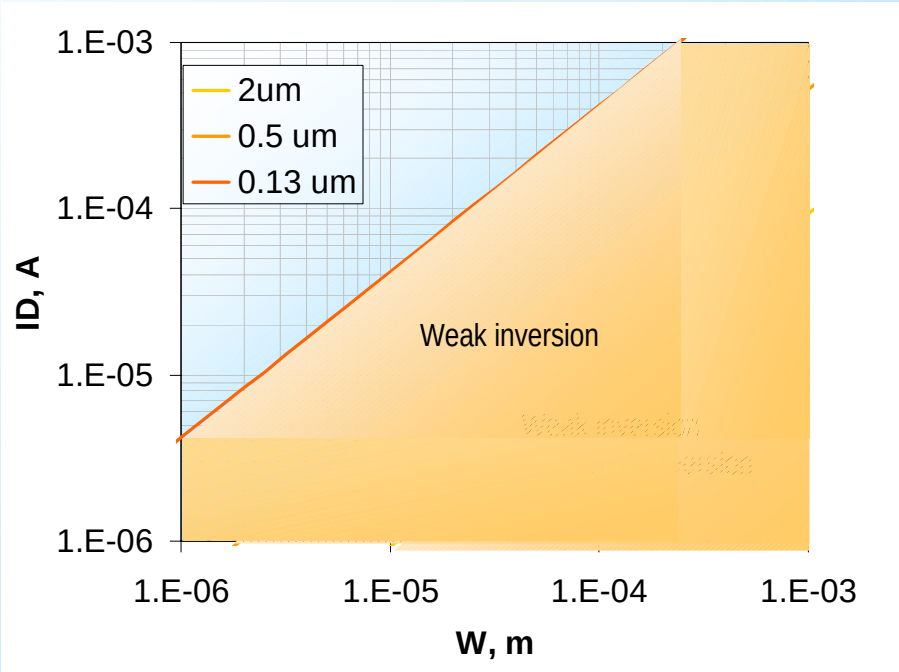
II. Design example: PET front end in 0.18μm CMOS

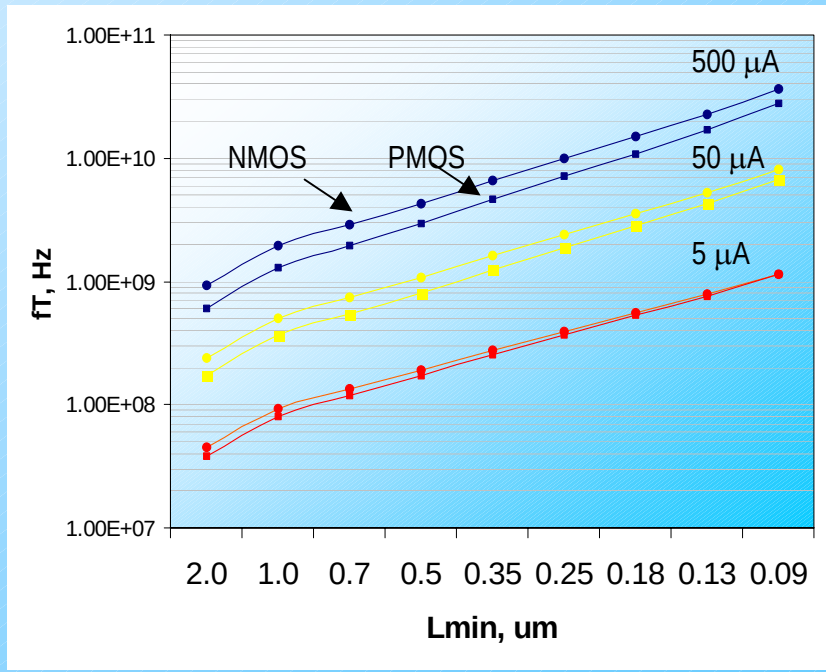
Design Methodology

1. System specifications
2. Technology choice
3. Noise properties of transistors
4. Hand calculate input MOSFET for minimum ENC
5. Design rest of preamplifier
6. Design remaining amplifier stages & bias circuits
7. SPICE simulate analog core
8. Design digital functions (if any)

Increasing importance of moderate inversion

- Linear current density I_D/W for moderate inversion increases by a factor of 10 every 2 CMOS generations.
- Submicron devices have high f_T even at low current.
- Also moderate inversion allows operation at low V_{DS}.





$W/L = 100$; $L=L_{min}$

Dimensioning the input MOSFET for minimum ENC

Series noise "capacitive match" problem:

$$ENC^2 = ENC_{sw}^2 + ENC_f^2$$

$$ENC_{sw}^2 = \frac{a_1}{2\tau_p} e_{n,sw}^2 (C_d + C_{in})^2$$

$$e_{n,sw}^2 = \frac{4kTn\gamma}{g_m}$$

$$ENC_f^2 = a_2 \pi \frac{K_F}{C_{ox} WL} (C_d + C_{in})^2$$

γ and g_m depend on region of operation:

	γ	g_m
weak	1/2	qI_D / nkT
strong	2/3	$\sqrt{2\mu C_{ox} \frac{W}{L} I_D}$

How to handle moderate inversion?

G.De Geronimo, P.O'Connor , V. Radeka and B. Yu, "Front-end electronics for imaging detectors", *Nuclear Instrum. Methods* A471 (2001) 192-199

P. O'Connor and G.De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", *Nuclear Instrum. Methods* A484 (2002) 713-725

L. Fabris, P. Manfredi, "Optimization of front-end design in imaging and spectrometry applications with room temperature semiconductor detectors", *IEEE Trans Nucl. Sci*., 49 (4) ,1978 –1985, Aug. 2002

M. Manghisoni, L. Ratti, V. Re, and V. Speziali, "Submicron CMOS Technologies for Low-Noise Analog Front-End Circuits", *IEEE Trans. Nucl. Sci.* 49,1783-1790, Aug. 2002

Simplified EKV model for hand calculations

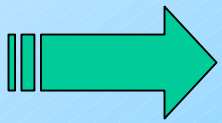
- substrate-referenced compact MOS model
- small, physics-based parameter set
- continuous modeling of weak to strong inversion
- simple set of equations valid for saturation:

Inversion coefficient $i = I_D / I_0$

$$I_0 = 2n\beta \cdot U_T^2 \qquad \beta = \mu \cdot C_{ox} \frac{W}{L} \qquad U_T = \frac{kT}{q}$$

Interpolation function :

$$f(i) = \frac{1}{2}\left(\sqrt{1+4i}+1\right)$$



$$\frac{g_m}{I_D} = \frac{1}{n \cdot U_T} \frac{1}{f(i)}$$

$$\frac{C_{GS}}{WLC_{ox}} = \frac{1}{\frac{3}{2} + \frac{f(i)}{i}}$$

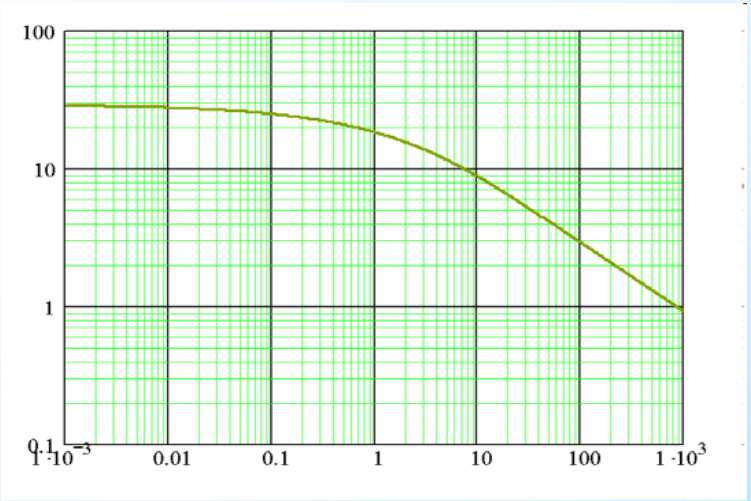
$$\frac{S_{th}}{4kTng_m} = \frac{\frac{1}{2} + \frac{2}{3}i}{1+i} \equiv \gamma$$

short-channel effects not modeled

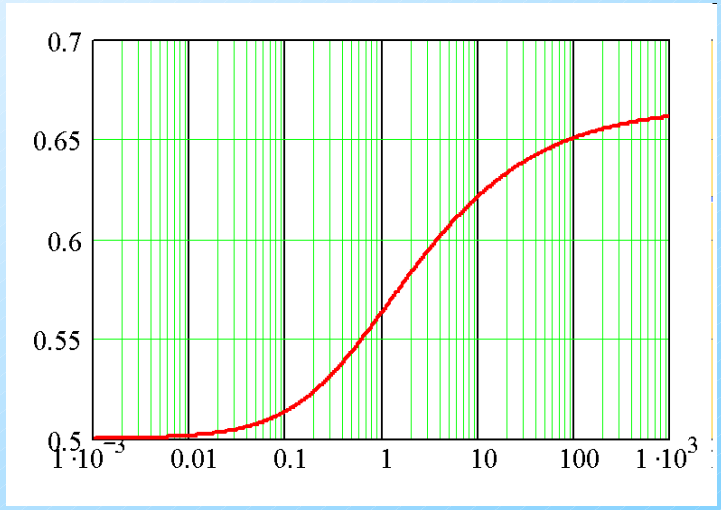
C. Enz, F. Krummenacher, E. Vittoz, "An Analytical MOS Transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications", *Analog Integrated Circuits and Signal Processing* 8, 83-114 (June 1995)

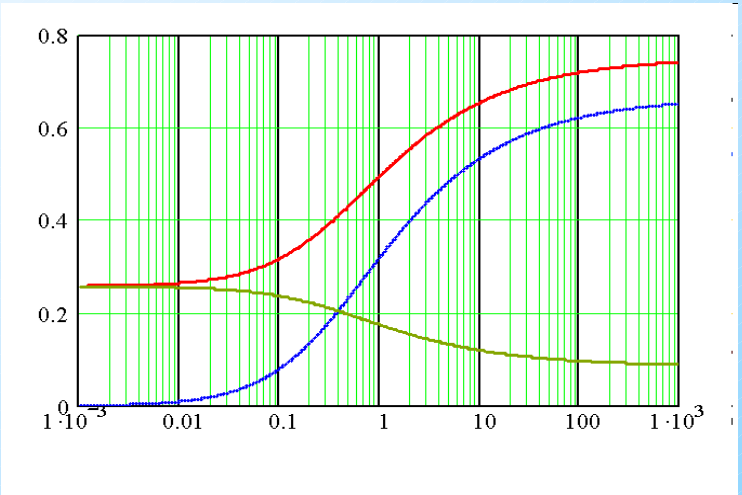
EKV results

g_m/I_D vs. i



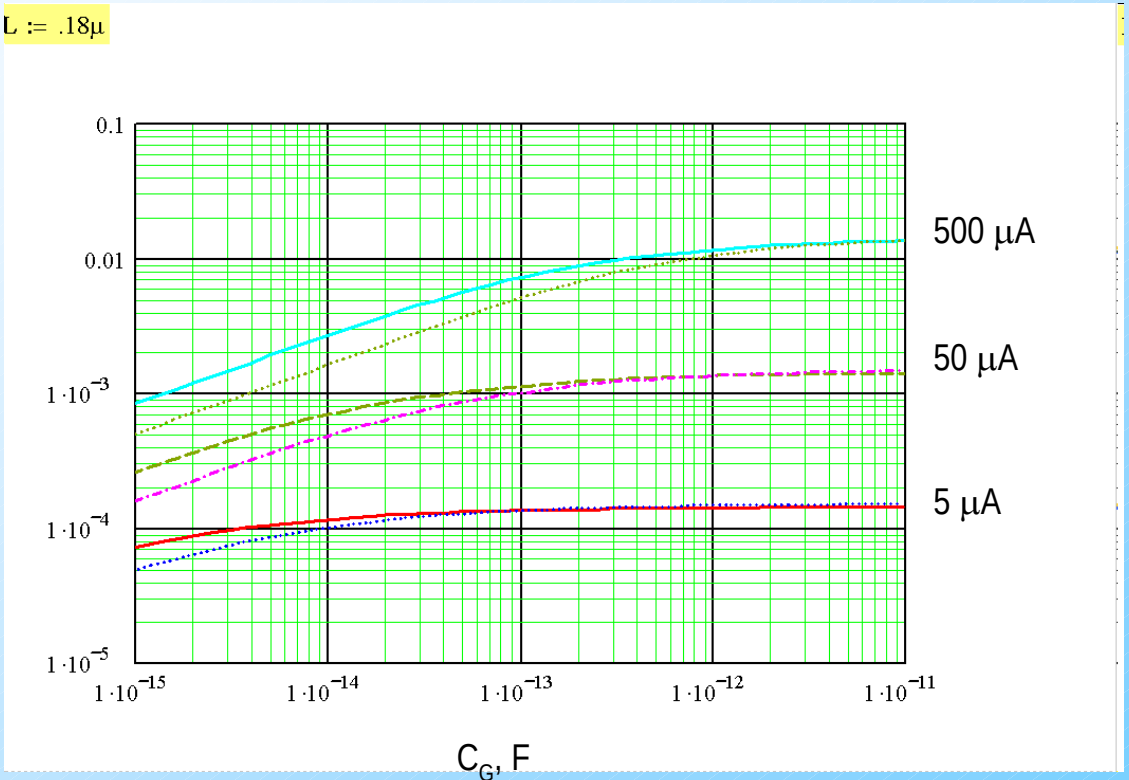
γ vs. i





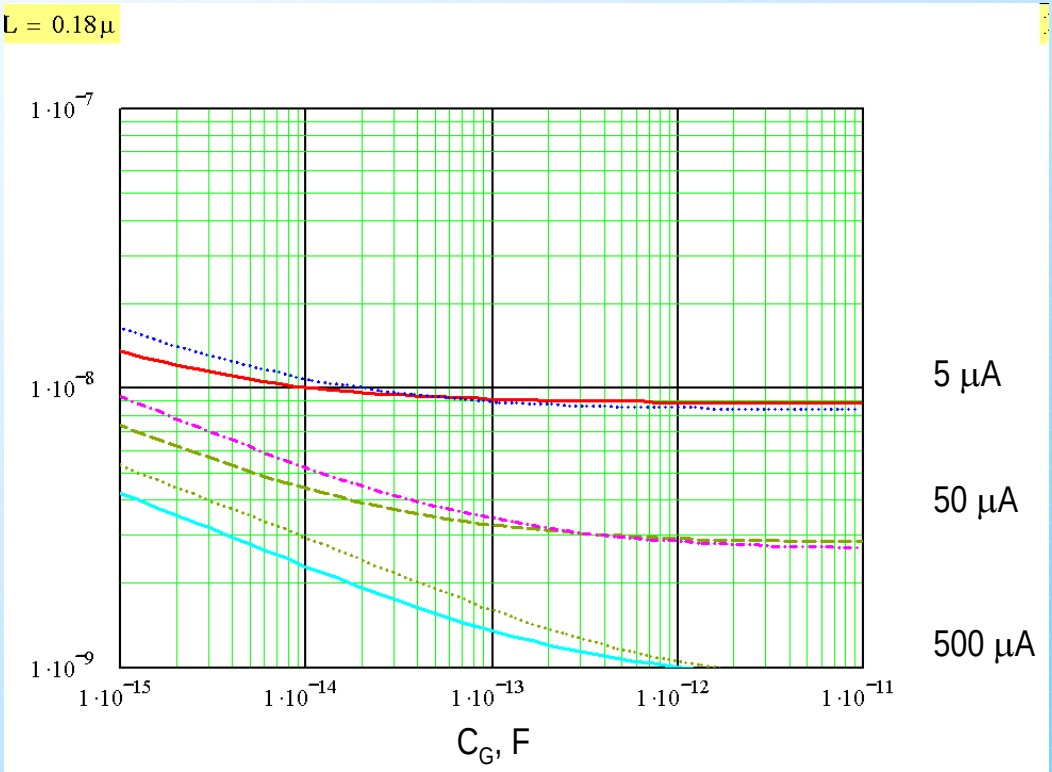
C_{gs}, C_{gb}, C_{in} vs. i

g_m vs. C_G vs. scaling



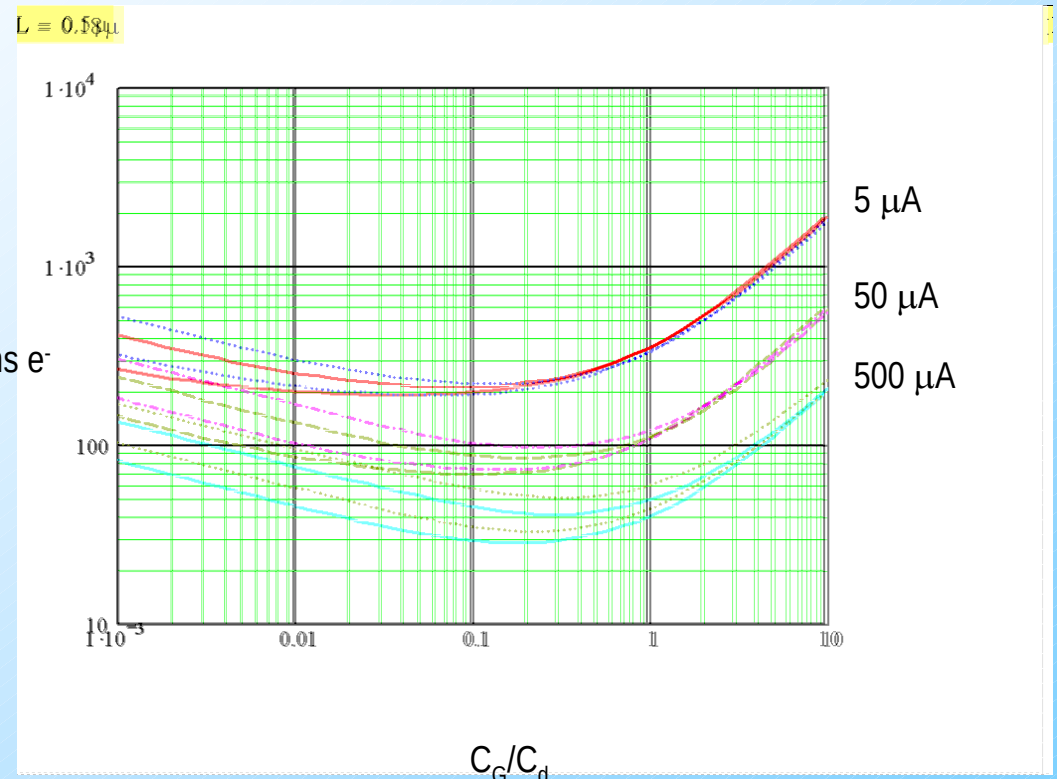
NMOS (upper) PMOS (lower)

e_n vs. C_G vs. scaling



NMOS (lower) PMOS (upper)

White series noise vs. C_G/C_d vs. scaling

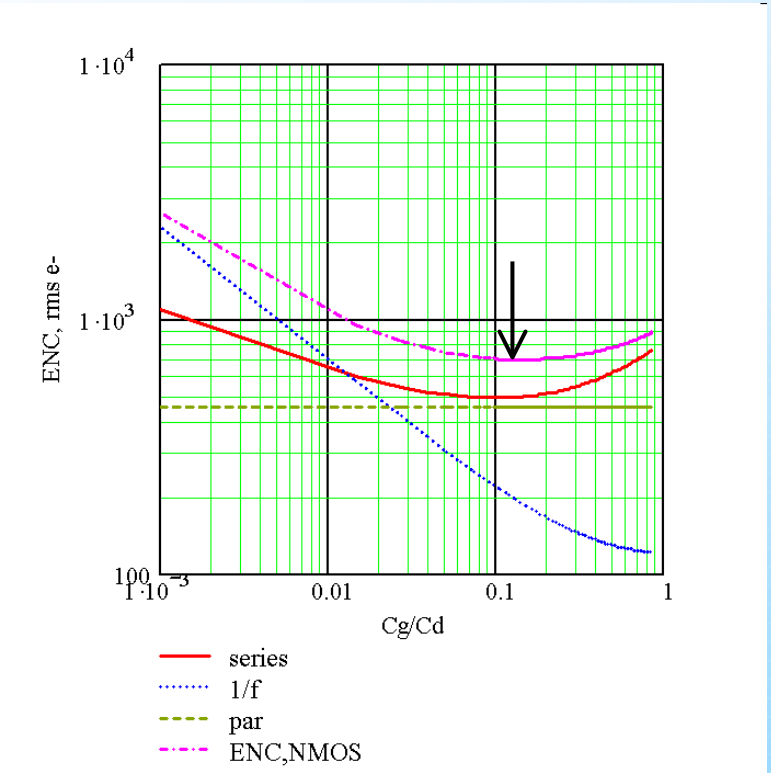


NMOS (lower) PMOS (upper)

Device width for minimum ENC

0.18 CMOS, tp=70ns, P=1mW, Ileak=250nA, Cd=20pF, $KF_n=10^{-24}J$, $KF_p=10^{-25}J$

NMOS

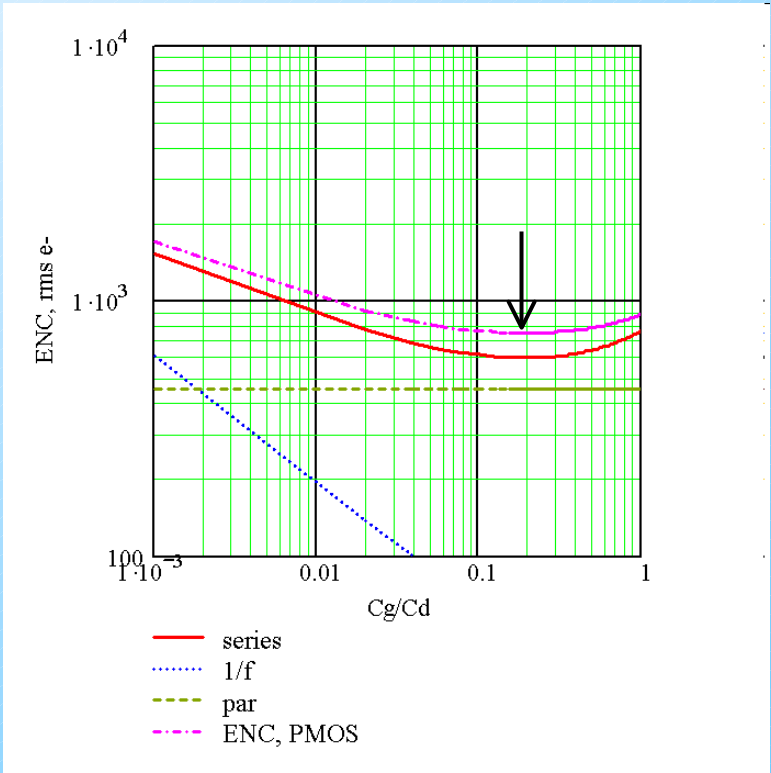


ENC_{min}= 697 e^-

C_{gopt} = 0.14 C_d

IC = 0.136

PMOS

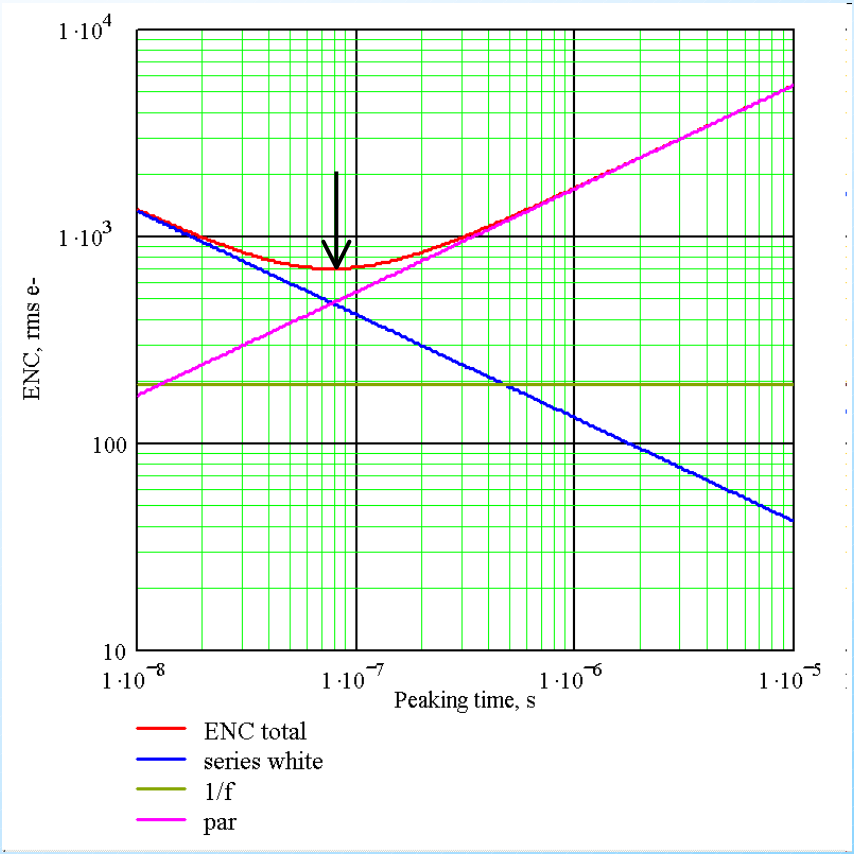


ENC_{min} = 748 e^-

C_{gopt} = 0.19 C_d

IC = 0.316

Noise vs. peaking time for optimized device

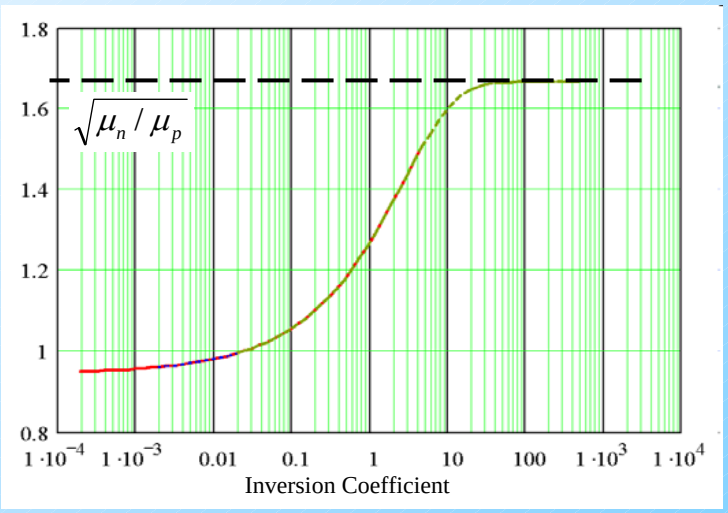


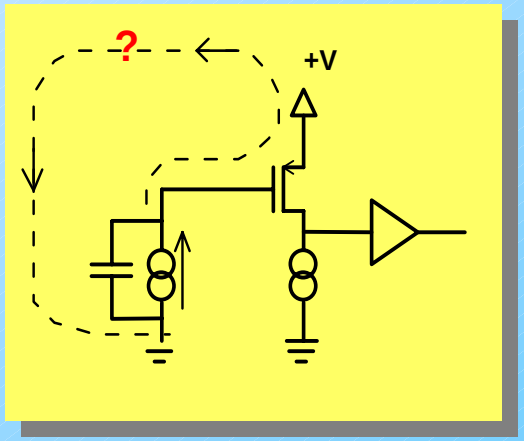
NMOS 1694/0.2, t_p=70ns,
ID=550μA,
Ileak=250nA, Cd=20pF
$KF_n=10^{-24}$J

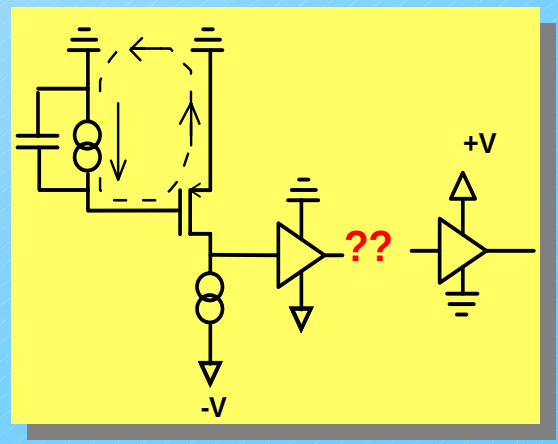
Choice of PMOS vs. NMOS

- PMOS lower 1/f noise
- NMOS white series noise advantage over PMOS diminishes each generation
- PMOS can be operated at reverse V_{BS} to reduce bulk resistance noise
- PMOS lower tunneling current at ultra-thin t_{ox}
- Single-supply operation of PMOS-input preamp awkward:

g_{mn}/g_{mp} vs IC



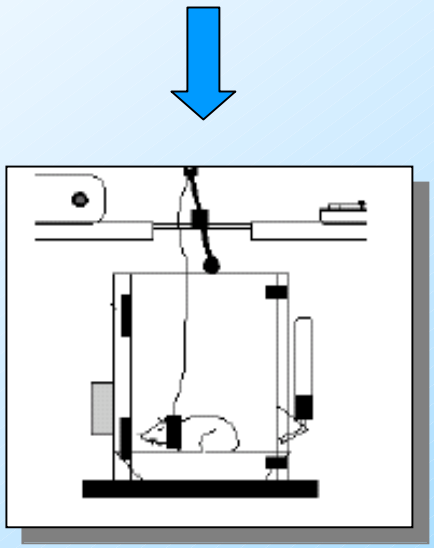




II. Design example: PET front end in 0.18 μm CMOS

RatCAP: Rat Concious Animal PET

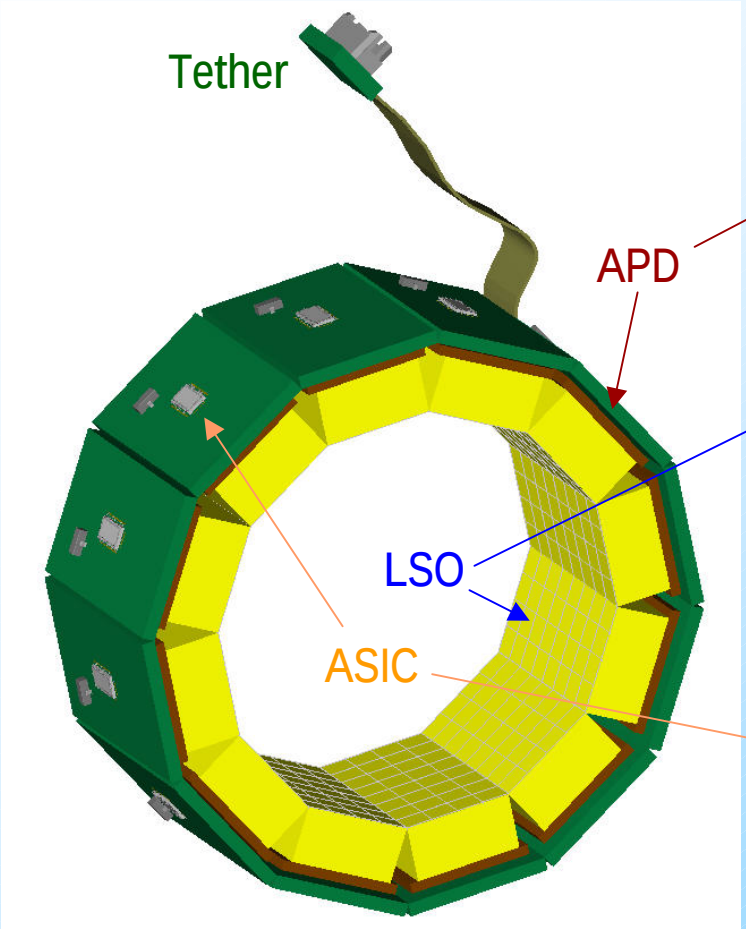
Head-mounted tomograph to image the brain of an unanesthetized, freely moving animal

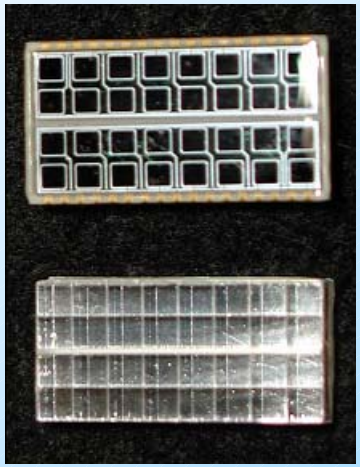


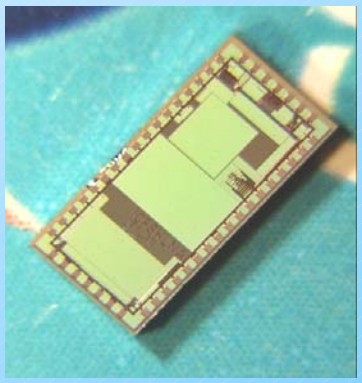
Mockup of the portable ring on the head of a rat

C. Woody et al., "RatCAP: A Small, Head-Mounted PET Tomograph for Imaging the Brain of an Awake RAT", NIM-A (submitted)

Tomograph Ring







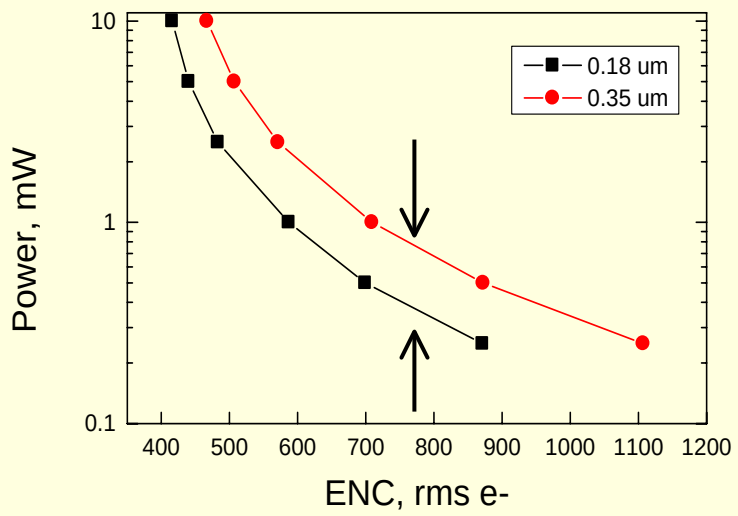
- 4 cm ring containing 12 block detectors (LSO/APD)
- 384 or 768 channels
- 15 Mcps rate for full ring
- 150g total weight
- 1.5W power on ring
- flexible and lightweight cable for signals, power, HV

C. Woody et al., "RatCAP: A Small, Head-Mounted PET Tomograph for Imaging the Brain of an Awake RAT", NIM-A (submitted)

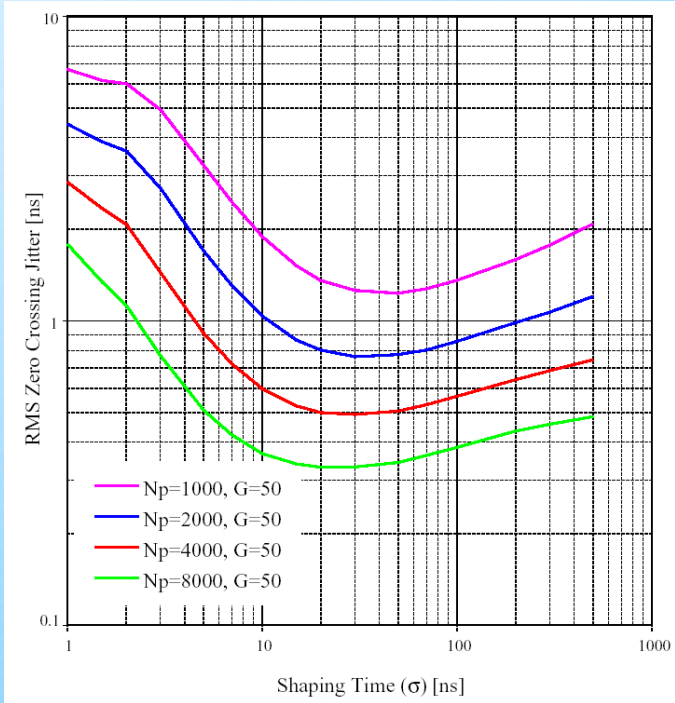
Technology choice

- 0.35 and 0.18 μm available
- Critical requirement: low power and low noise
- Dynamic range low

Preamp power vs. ENC



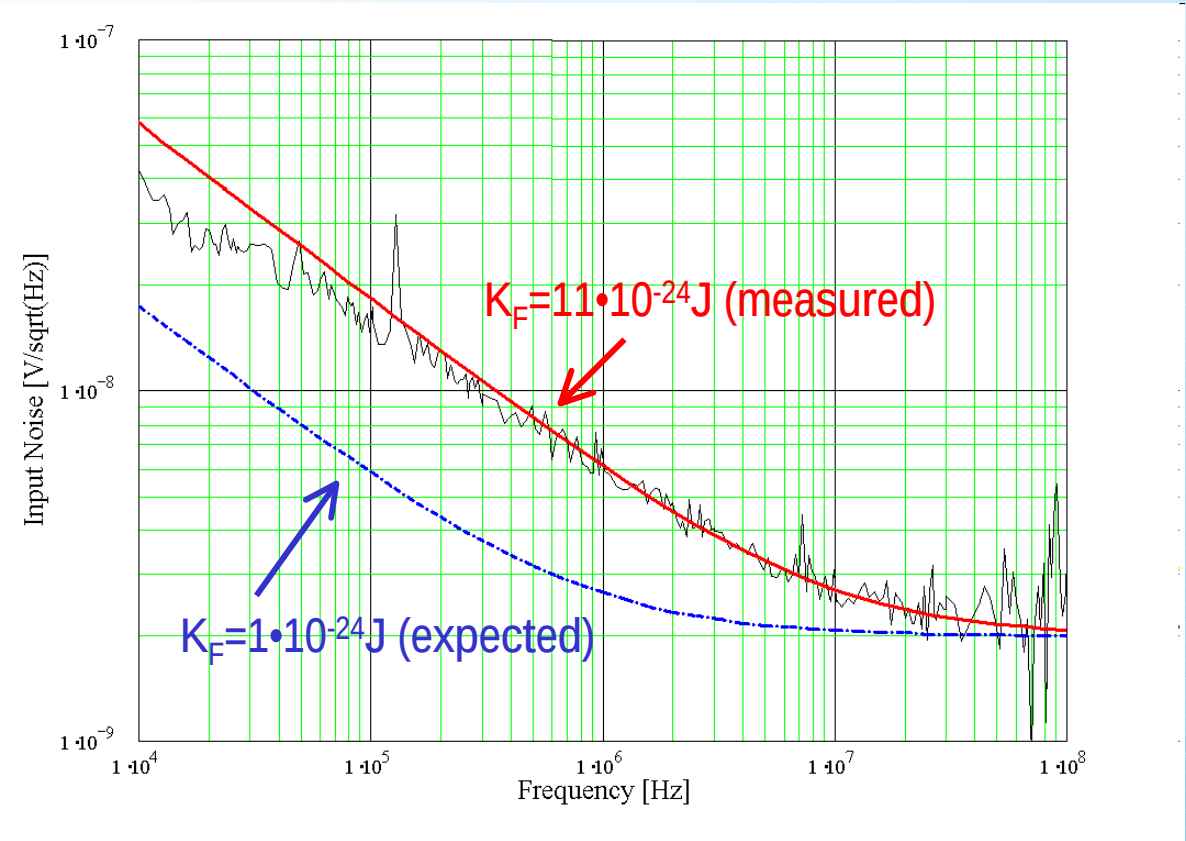
Time jitter vs. shaping time



- LSO decay 40 ns
- e_n ~ 1 nV/√Hz

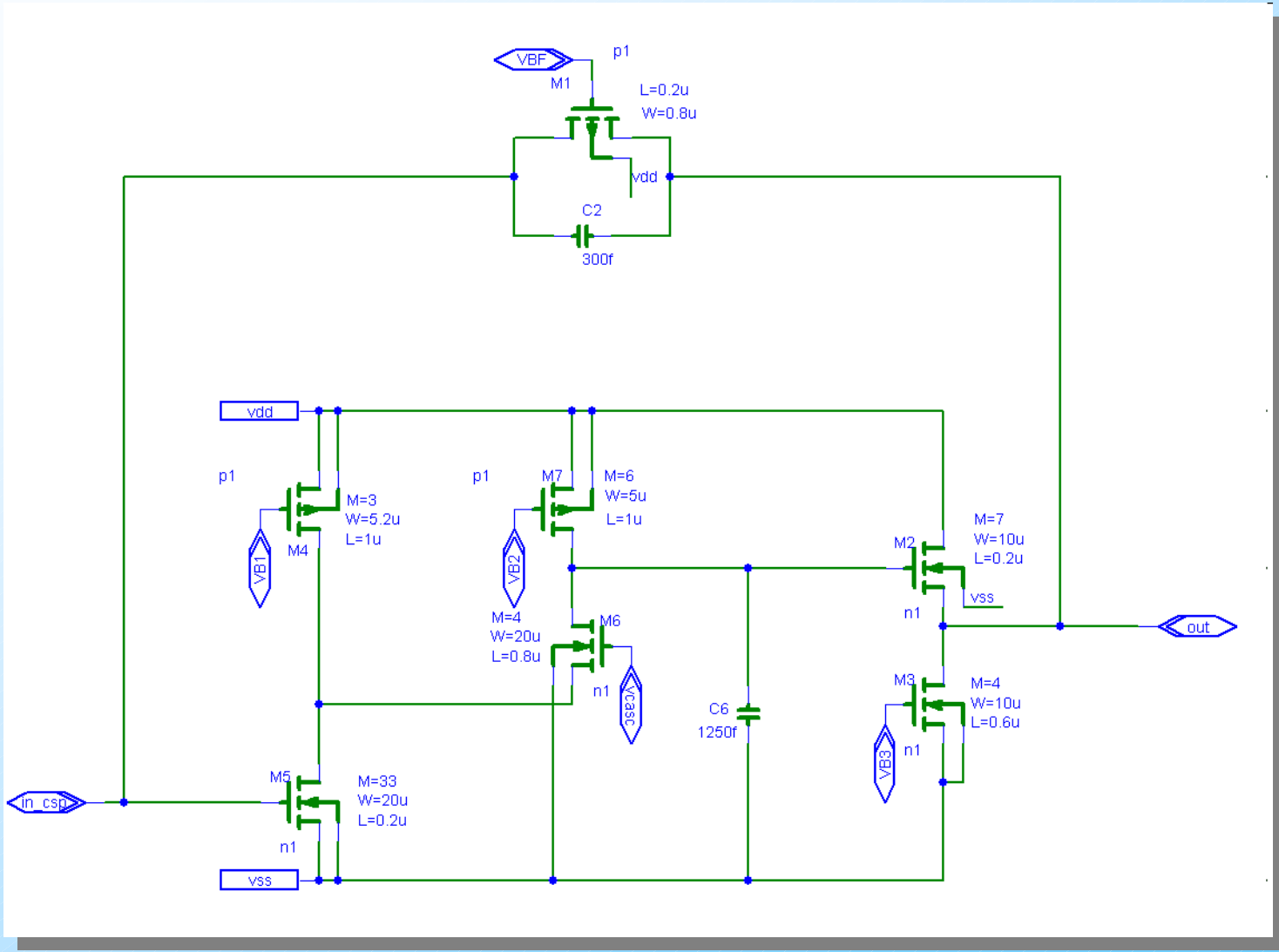
B. Yu

NMOS noise measurement



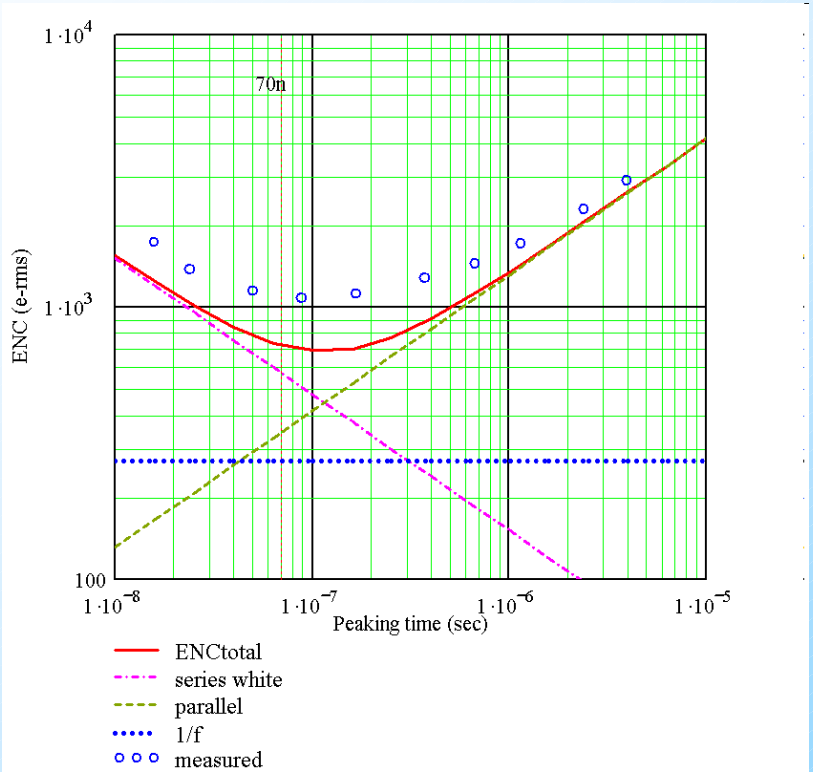
- unexpectedly large 1/f noise found for this technology.
- preamp ENC 32% higher than predicted.
- re-optimizing W for better noise balance could save 11%.
- PMOS a better choice?

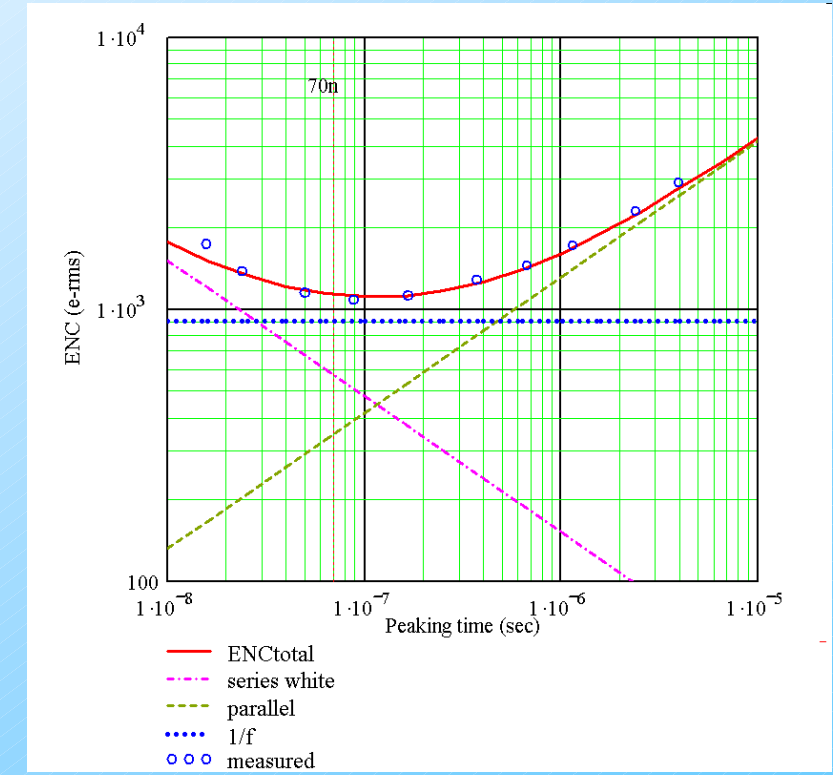
Preamp schematic



Simulated and measured preamp ENC

Preamp ENC vs. shaping time





simulated with $K_F = 10^{-24}$ J

simulated with $K_F = 11 \times 10^{-24}$ J

W=33 x 20/0.2, I_D=550uA, R_G=3, R_B=100

Conclusions

- moderate and weak inversion bias points become more prevalent in submicron CMOS
- simplified EKV model for preliminary design:
  - continuous modeling of the weak-strong inversion transition
  - small parameter and equation set
  - solves “capacitive match” for series white noise
  - simple way to study effects of MOS scaling
- PMOS input device usually lower noise than NMOS but practical concerns limit usefulness
- low-power PET preamp in 0.18 μm CMOS has been designed
  - unexpectedly high 1/f noise in short-channel NMOS is found in this technology