The CDF Run IIb Silicon Detector

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Fermilab plans to deliver 5-15 fb^{-1} of integrated luminosity to the CDF and D0 experiments. The current inner silicon detectors at CDF (SVXIIa and L00) will not tolerate the radiation dose associated with high luminosity running and will need to be replaced. A new readout chip (SVX4) has been designed in radiation-hard 0.25 μm CMOS technology. Single sided sensors are arranged in a compact structure, called a stave, with integrated readout and cooling systems. This paper describes the general design of the Run IIb system, testing results of prototype electrical components (staves), and prototype silicon sensor performance before and after irradiation.

1. Introduction

Until the turn-on of LHC, the Fermilab Tevatron will continue to be the highest energy accelerator in the world. To exploit the discovery potential of the Tevatron, Fermilab is planning on extensive collider running, which will deliver 5-15 fb^{-1} of integrated luminosity. The Run IIa inner silicon detectors (L00 and SVXIIa) are expected to suffer significant performance degradation after roughly 4 fb^{-1} of delivered luminosity. For Run IIb, these detectors will be replaced by a new silicon detector which is optimized for high luminosity running and resistance to radiation [1]. The Intermediate Silicon Layers (ISL) will be retained for Run IIb.

The physics goals of Run IIb are broad and fundamental. Not only is the Tevatron the only place to search for a light Higgs boson until the LHC era begins, but it is also currently the only source of top quarks. Precise measurements of the top quark and W masses will be possible. Studies of B physics can provide constraints on the CKM matrix and many searches for SUSY, SUSY Higgs and extra dimensions can be performed. Crucial for most of these physics goals is the ability to tag the presence of B hadrons efficiently and with high purity. Figure 1 shows one example where the standard model Higgs mass sensitivity is plotted as a function of b-tagging efficiency.

Both the Run IIa and Run IIb detectors have 6 layers where the outer 5 layers (L1-5) each provide two measurement points, typically an axial and a stereo measurement. Both detectors have the layers arranged in a castellated pattern around the beam-line to provide 100% axial coverage. Figure 2 shows an end view of the Run IIb silicon detector.

The basic building block of the Run IIb detector is called a "stave". Based on the experience constructing previous generations of silicon trackers at CDF, a uniform design has been chosen for all the outer layers which emphasizes simplicity of design and assembly. Only the innermost layer, L0, will have a different structure. L0 will have a low mass design (similar to the Run IIa L00) providing good impact parameter resolution. The component counts and diversity of fixtures and procedures required has been dramatically reduced. While the CDF Run IIa tracker had 8 different "ladder" types and 13 different hybrid designs, the Run IIb stave based design will only require one hybrid type for the stave and one for Layer 0.

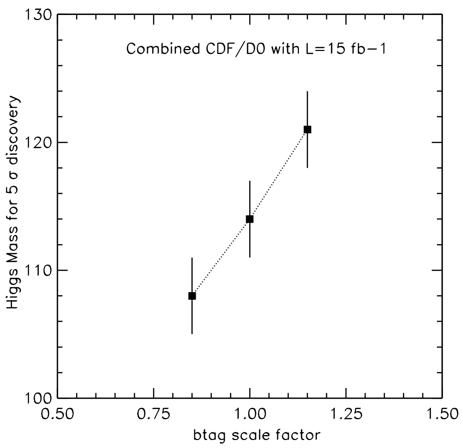

Figure 1. Higgs mass reach for a 5σ discovery as a function of the b-tag efficiency relative to a nominal value of 65% for an integrated luminosity of 15 fb^{-1} per experiment.

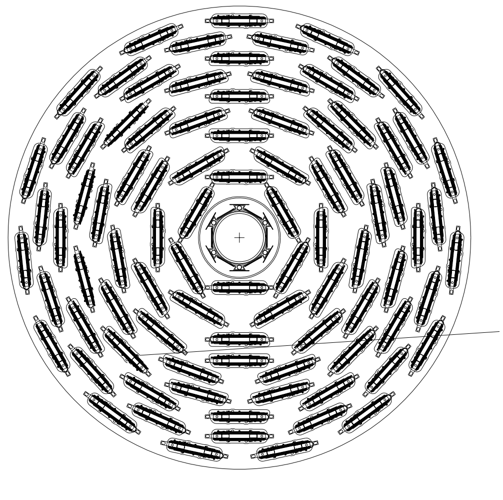

Figure 2. End view of the Run IIb silicon detector design

The Run IIb silicon detector design improves over the Run IIa detector in a number of areas.

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To improve the radiation hardness a new readout chip (SVX4) has been developed in 0.25 μm CMOS technology. The sensors for Run IIb are single-sided and will be actively cooled to temperatures of -5° C. The Run IIb detector has a longer tracking volume (1.2 m compared to 0.9 m) and will therefore provide a larger acceptance for tagging jets with B hadrons. The Run IIb detector design has also expanded in radial coverage (16.6 cm compared to 10.6 cm) and the portcard electronic components (providing regulation and interfacing) have been relocated to outside the tracking volume. This will provide a better connection for tracking between the new SVXIIb detector and the ISL layers. The inner layers of the Run IIb detector are also strengthened compared to Run IIa with redundant axial sensors at Layer 1. Prototype staves have been constructed and extensively tested. The results are discussed below followed by a summary of the performance of the prototype silicon sensors.

2. Stave design and testing results

To meet the needs of the Run IIb tracking environment, the Run IIb stave design features low temperature operation, with embedded cooling channels, minimum mass, and dead-timeless readout and acquisition. Carbon fiber (CF) and foam composites are used for light, rigid structures, and aggressive fine-pitch electrical interconnects are used to minimize the areas of support circuitry. The requirement of dead-timeless operation means that the SVX4 chips store signals on the front end analog pipeline capacitors at the same time as prior events are digitized or read out. Stave electrical performance must accommodate this.

Each stave is built around a thermal mechanical core. The core consists of Rohacell foam with embedded PEEK cooling tubes. Carbon fiber skins are laminated on each side providing mechanical rigidity. The CF layers are connected to the electrical ground of the analog circuitry.

A stave consists of 6 independent silicon strip modules, 3 on each side. Each module is composed of two silicon sensors, wirebonded together and read out by an on-board hybrid circuit holding four SVX4 chips for a total of 512 channels. The overall length of a module is 20 cm. The average radiation length of a stave is 1.8% and is dominated by the silicon.

A bus cable carrying data and control signals runs on each side of the stave core, underneath the sensors. The modules are bonded to the bus cable through 3 mm gaps between the modules. At the end of each stave a kapton flex cable and a mini-portcard (MPC) provide the connections between the top and bottom of the stave and retransmission of the signals to the external electronics racks. The total length of the stave is 66 cm (3 modules plus the MPC). Figure 3 shows a detailed sketch of a stave and its components. Figure 4 shows a end view, detailing the different layers.

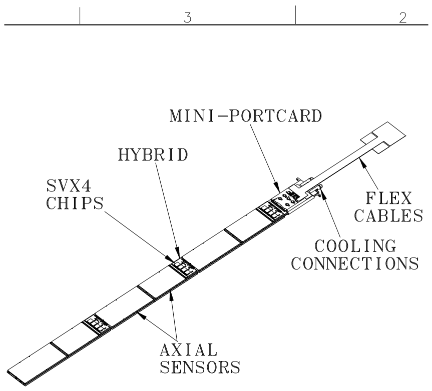

Figure 3. Run IIb stave layout

Axial or stereo sensors can be used on either side of the staves. The strip pitch is 75 μm for axial and 80 μm for stereo sensors. To optimize the strength of the inner tracking, L1 will have axial sensors on both sides. Layers 2-4 will have small angle stereo sensors (1.2°) on one side and axial sensor on the other. Layer 5 will have axial sensors on both sides for a good connection to the outer tracking systems. All outer layer staves use identical 4-chip hybrids. L0 uses a 2-chip hybrid which follows the design of the outer layer hybrid. This uniformity greatly simplifies the assembly and construction.

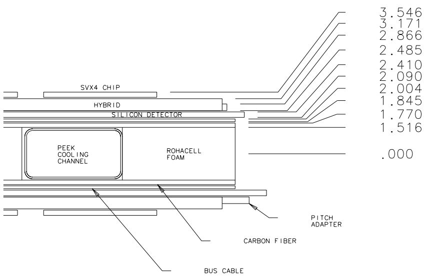

Figure 4. Detailed view of one half of the end of the stave showing mechanical and cooling features.

Both thermal and mechanical properties of the staves have been simulated and measured. Maximal sag due to gravity is 130 μm, within the specifications for the tracker. The innermost silicon detectors need to operate at -5°C. Thermal studies have shown that the temperature rise in a single stave is $\leq$ 2°C for the allowed pressure drops, flow rates and the full heat load. The system is designed to run with an entrance temperature of -15°C for the coolant. Staves will be ganged together to meet the required temperature specifications while minimizing the associated plumbing. Layer 1 will feed individual staves. On the outer layers 3 staves will be ganged together.

The bus cable is a flexible etched laminate of Kapton, Copper, and Aluminum foil. It is insulated from the high voltage back plane of silicon sensors by a thin Kapton cover layer. The bus cable carries wide power traces and narrow (200 μm pitch) traces for clocks, commands, and data. High voltage is also distributed on the bus cable. Bond pads (for bonding to the hybrid) are located on the bus cable to correspond to the gaps between the modules. Bonds are made to exposed gold plated sections of the bus lines. All hybrids on a bus share the data and command lines. Separate clock, power and HV lines serve each hybrid. The readout token (priority line) is also passed between hybrids on the bus.

Both the hybrids and the MPC are fabricated in a thick film process with gold conductors on a Beryllia substrate. Beryllia is used both for its high thermal conductivity and long radiation length. The line-work on the hybrids and MPC is aggressive, featuring 100 μm lines and spaces. This is achieved with a unique etchable thick film conductor technology. The fine line work allows for a minimum package size for the hybrid and MPC, reducing the material burden considerably.

A critical aspect of the stave design is noise performance. Since the digital lines on the stave run directly beneath the detector HV backplane, a significant potential for performance degradation exists. These issues have been addressed through a program of study on various mock-ups and prototypes. It was demonstrated that a shield layer, connected to analog ground is required. With the shield, pickup effects are negligible except for certain short periods when particular command sequences are sent the SVX4 chips. These sequences are associated with changes in the operating mode of the SVX4 chip. During these transitions the total current supply to the digital part of the SVX4 chip may change resulting in induced signals on the bus cable shield. The magnitude of the induced effect, as seen on the pedestal of the SVX4 chip, can be regulated by a number of factors. These include the position of the current settings on various drivers, bandwidth settings of the SVX4 pre-amp, bypassing, and inter-line capacitances within the bus cable. The studies to date indicate close to acceptable performance in a dead-timeless mode of operation.

Beyond these effects, the SVX4 chip includes a real-time event-by-event pedestal subtraction feature (RTPS) which can generally compensate for any residual pickup effects as well. To study noise performance and dead-timeless operation in the stave environment, a set of bench testing tools are utilized. These include a statistical noise measurement on an ensemble of events and a "differential noise" measurement. In the latter case the noise is measured by studying the difference between two adjacent channels event-by-event.

Figure 5 shows noise and "dnoise" for all the channels on a stave. The strips are bonded to 1 or 2 sensors or are unbonded. The near equality of noise and dnoise indicate that little pickup was present. Figure 6 shows a measure of the pedestal of a particular channel as a function of the number of clock cycles between the triggered event and the previous triggered event. In this

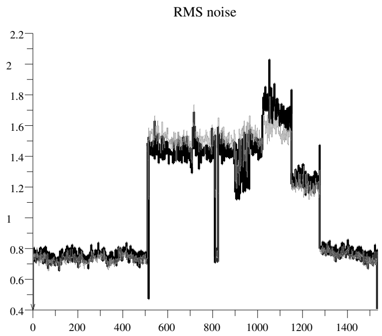

Figure 5. Noise (dark) and Dnoise (light) on a stave. Channels 1-512 and 1350-1536 are unbonded, channels 513-1290 are bonded to two sensors (full load). Channels 1050-1290 are damaged, resulting in excess leakage current and noise. Channels 1291-1349 are bonded to one sensor. Two-sensor noise is about 1200 electrons.

plot the SVX4 chip is sequenced through all its different modes of operation. The data indicate the effect upon a particular charge sample due to other activity in the chip, e.g. readout or digitize on an earlier event. A pedestal shift of significant magnitude, as compared to a minimum ionizing particle, is a source for concern. Such shifts do occur, for certain cycles, when particular commands are in sequence. The lower trace shows the effect when RTPS is invoked. In this case the pedestal shifts always become negligible. Current studies involve efforts to limit the transitions further in RTPS-off mode. To date three fully functional staves have been assembled and studied. A pre-production phase of the project begins Summer 2003 in which of order 25 staves will be built and tested.

3. Silicon Sensors

The Run IIb detector will have ≈2300 single-sided silicon microstrip sensors. The main specifications are: (1) sensors should be operational up to 500 V, (2) full depletion voltage should be in the range from 120 to 250 V; (3) dead channel fraction should be less than 1%; (4) sensors should be uniform in coupling capacitance (>12

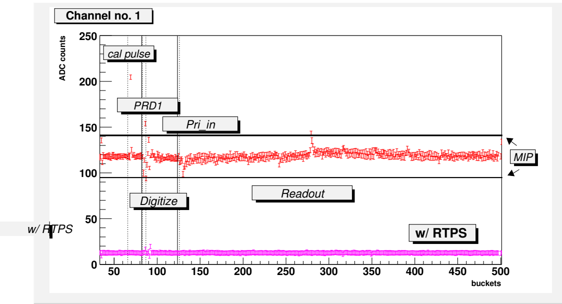

Figure 6. Study of dead-timeless operation with RTPS off (top) and on (bottom) curves. Various operating conditions of the SVX4 chip are indicated.

pF/cm), bias resistance (1.5 ± 0.5 MΩ), interstrip resistance (< 1.2pF/cm), and other electrical properties. We have employed single-sided p^+-on-n sensors with dimensions of 96.4 mm length and 40.6 mm width for axial and 41.1 mm width for 1.2° stereo sensors, so that two sensors can be taken from a 6" wafer. The readout pitch is 75 (80) μm for axial (stereo) sensors. A single intermediate strip is implemented to improve position resolution.

Prototypes of 63 axial and 53 stereo sensors were fabricated by Hamamatsu Photonics (HPK). We have performed detailed electrical characterization of 18 sensors for each type along with other more general tests such as I-V and C-V characteristics. The innermost sensors will receive radiation corresponding to 1.4×10^{14} 1-MeV eq. neutrons/cm^2 in 30 fb^{-1} of data taking period. We have irradiated five sensors up to this fluence. The performance results of irradiated sensors are also reported.

3.1. Initial electrical characteristics

The I-V measurement results are summarized in Fig.7. The leakage currents are normalized to 20°C. Most of the sensors do not exceed 0.2 μA even at 950 V. Only two sensors out of 116 showed noticeable micro-discharge.

Scanning the individual strip current for the two leaky sensors, we found only one strip for each sensor is contributing to the large leakage. The micro-discharge onset voltage shifted higher as we repeated the I-V measurements.

HPK reported in total 21 defective strips on 14 sensors out of 116. Our full characterization for 36 sensors, including these 14 sensors, recognized all the defects reported by HPK. In addition, we found 5 implant opens and a pair of low bias resistors. The five new implant opens were not detected by HPK because they were not set up to test for them. The low bias resistor pair is obviously due to a discharge, probably caused by probing. The estimated dead channel fraction is 0.08% including these defects.

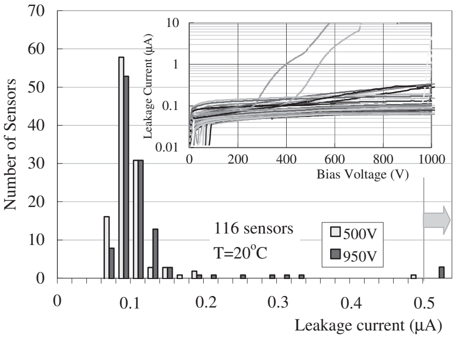

Figure 7. Leakage current distributions of 116 prototype sensors at 500 and 950 V. The overflows are histogrammed on the extreme right. The inset shows the I-V curves of all the sensors.

3.2. Electrical characteristics of irradiated sensors

The irradiation took place at MNRC Irradiation Facility at UC Davis. Three sensors were irradiated to 1.4×10^{14} n/cm^2 and two to 0.7×10^{14} n/cm^2.

The damage constant evaluated from five sensors is $(2\text{–}3)\times10^{-14}$ A/cm, consistent with the previously known value [2]. The I-V curves are good to 1000 V without showing significant micro-discharge.

The full depletion voltage was evaluated when the initial beneficial annealing is almost completed. It resulted to 100 V (40–50 V) for the sensors irradiated to 1.4 (0.7)$\times 10^{14}$ n/cm^2, whereas 90 V (40 V) is an expectation from Rose parameterization [2] .

The capacitance between two neighboring readout strips is plotted in Fig.8. The data is for the two sensors irradiated to 1.4×10^{14} n/cm^2. The curves show shoulders around 130 V corresponding to the full depletion voltages (note: these were measured at annealing conditions different from the above), then decrease gradually with the bias voltage. Though the asymptotic value is consistent with non-irradiated sensors, an excess bias of 200–250 V is required to reach the minimum. The interstrip resistance of >1 GΩ is achieved for a bias of 300 V.

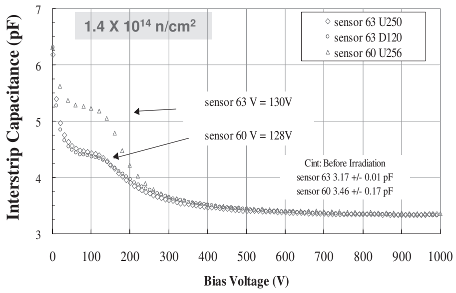

Figure 8. Interstrip capacitance of two irradiated sensors: one pair and two pairs for each.

4. Summary

The Run IIb silicon project is well underway. The prototype phase has been very successful and is nearly complete. Preproduction parts have been ordered and construction of preproduction staves will begin this summer. The preproduction SVX4 chips arrived on May 16, 2003 and initial testing results look very promising. The preproduction hybrids are expected in July and delivery of production sensors will begin in June 2003. Full stave production is scheduled from Feb.-Dec. 2004. Barrel assembly and final preparations have an anticipated completion date of September 2005, with schedule contingency extending from Sept. 2005-May 2006.

REFERENCES

1. (CDF Collaboration) The Run IIb Technical Design Report, CDFNOTE 6261.
2. G. Lindstrom *et. al.* (Rose Collaboration), Nucl. Instrum. and Methods A466 (2001) 308.