Jet Propulsion Laboratory
Electronic Parts Engineering Office

Report on

Known Good Die:

Facilitating Multi-Chip Modules

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Executive Summary

The integrated circuit (IC) industry has been developing a Known Good Die (KGD) infrastructure to support multi-chip assemblies. KGD are tested unpackaged integrated circuits that often come with a guarantee. The industry aims to provide KGD with as little cost and with as much quality and reliability as if the IC were packaged.

Multi-chip assemblies come in two forms: hybrids and multi-chip modules (MCMs). Hybrids, the less complex of the two, contain mainly inexpensive passive and simple active devices. Thus, engineers often either rework or scrap hybrids with bad dice. Conversely, MCMs contain mainly complex, high pin count active devices that are much more expensive and harder to rework. This has led the industry to value assembling dice that are "known good" prior to MCM assembly.

Producing KGD involves establishing temporary die electrical contact and performing tests such as AC and DC parametric tests, functional tests, die-level burn-in, and mechanical and environmental tests. To establish temporary contact, most methods use carriers that companies are developing in three forms: permanent carriers, semi-permanent carriers, and temporary carriers. Besides die-level testing, ensuring KGD involves using a mature process, design-for-testability techniques, and in some cases, sample packaged IC testing.

Deciding on a KGD testing program involves trading off rework costs with KGD testing costs, while taking into account the maturity of the process and the statistics gathered from packaged part tests. Making such trade-offs leads customers to require different amounts of KGD testing. To accommodate these differing needs, many KGD suppliers offer several KGD assurance levels, where each level involves a different testing plan.

The KGD process should not alter the die size or electrical characteristics, and should not damage the die surface or the bond pads. When procuring KGD, the customer should receive all the information necessary to use the KGD in their final system. Also, the customer and supplier should agree on who is responsible for failures and under what conditions. Toward these ends, an MCC-led industry consortium, Rome Labs, and the rest of industry are all working to establish a broad range of KGD products, establish methods to quantify KGD probabilities, standardize KGD equipment and methods, and create a cost-effective KGD market for both the supplier and the user.

1. Introduction

Known Good Die (KGD) are tested bare unpackaged integrated circuits (ICs). IC suppliers often offer several levels of KGD, where each successive level entails a more rigorous test plan. High KGD levels often come with a quality and reliability guarantee, such as guaranteeing them to function on delivery, or to last through a certain time period. Industry aims to provide KGD that have at least as much quality and reliability as they would have if they were packaged.

This paper discusses the following KGD issues: why KGD are important, how to ensure KGD, KGD procurement issues, manufacturers involved with KGD, KGD wafer probe methods, KGD carrier methods, KGD infrastructure development programs, KGD procurement guidelines, and manufacturer KGD programs and perspectives.

2. Background: Why KGD Are Important

Multi-chip assemblies are single substrates on which engineers assemble multiple die. For decades, integrated circuit (IC) manufacturers have prepared multi-chip assemblies to enhance system performance and reliability, and to reduce electronic equipment size and mass. By assembling many dice on a single substrate, manufacturers reduce the number of I/O on the printed circuit board, and reduce the interconnect length between dice. Less I/O on the printed circuit board leads to less power dissipation from I/O drivers that must charge and discharge large interconnect capacitances. These I/O transients can lead to adverse cross-talk and ground-bounce switching noise. Also, shorter interconnect between dice lead to faster, more reliable systems. These multi-chip assemblies have evolved from hybrids, which have had widespread application for over thirty years, to multi-chip modules (MCMs), which have recently become popular.

Hybrids and MCMs have three components: the substrate, the dice, and the die interconnect. To address problems with the dice, we have two choices: 1) prepare ourselves to deal with multi-chip assemblies that tend to have bad dice, or 2) qualify the dice before assembly. Hybrids usually involve the former strategy, while MCMs usually involve the latter. This difference stems from the difference in complexity between hybrids and MCMs.

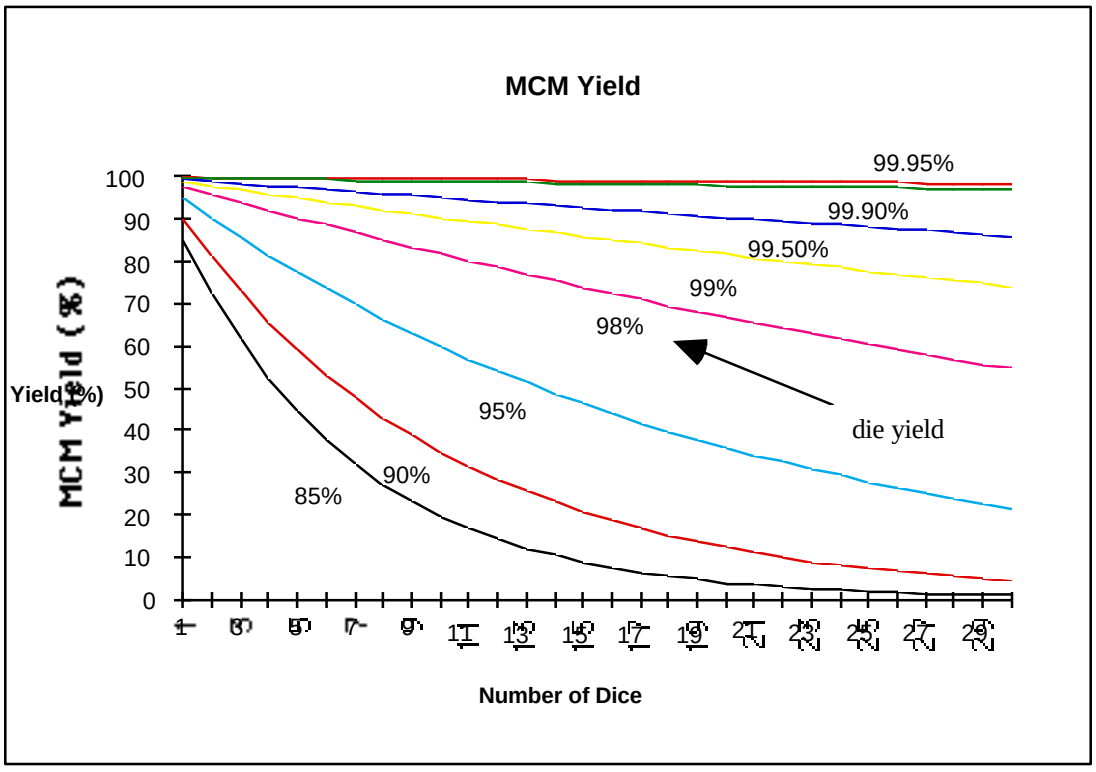
Hybrids usually contain passive devices and low pin count active devices. Compared with MCMs, hybrids contain higher yielding, simpler devices. Test engineers can usually test and rework these devices, once assembled. Hybrids have relatively large signal lines that often facilitate chip-to-chip characterization. Thus, engineers usually find it more cost-effective to either rework or scrap hybrids that have faulty devices than to extensively test each hybrid element before assembly.

MCMs, on the other hand, contain mainly larger, more closely spaced, high pin count, active devices. This makes MCMs more expensive and harder to rework. Smaller signal lines make probing more difficult due to their inaccessibility and due to their sensitivity to probe capacitive loads and impedance discontinuities. Thus for MCMs, engineers generally desire assuring die quality and reliability preceding MCM assembly. This desire has lead to the advent of Known Good Die.

To illustrate KGD importance, consider the following equation for MCM yield:

$$Y_{MCM} = Y_{DIE}^{N}$$

where Y_{DIE} represents the die yield, assuming each die has the same yield, n represents the die quantity on the MCM, and Y_{MCM} represents the resulting MCM yield. Graphing this equation, we see that MCM yield rapidly decreases as the number of dice increase, and as the die yield decreases:



How do you produce a die that is “known good”? This paper aims to answer this question. In general, producing KGD involves electrical contact to the die, mechanical fixturing to facilitate electrical contact to the die, tests such as AC and DC parametric tests and die-level burn-in, and various IC design techniques such as scan design, BIST, and boundary scan. The KGD process should not alter die size or electrical characteristics, and handling and mechanical contact should not create die surface or bond pad damage. Ideally, KGD should not cost more than their packaged equivalents, and should have comparable quality and reliability. KGD must fully function following MCM assembly,

over the specified temperature range, at operating speeds, after MCM burn-in, and throughout their guarantee period. When purchasing KGD, the customer should also receive all the information needed to use the die in their system (see section 11), and it should be clear who bears responsibility for failures and under what conditions.

These issues create many technical challenges that the industry still needs to overcome. To help make MCMs commercially viable, ARPA has sponsored an industry consortium led by MCC to study testing and procurement issues associated with KGD. Rome Laboratory has also begun a "Known Good Devices" program addressing not only the die, but all aspects involved in creating reliable MCMs. Meanwhile, the industry is attempting to 1) establish a broad KGD product range, 2) establish methods to quantify KGD probabilities, 3) standardize the equipment and methods, and 4) create a cost-effective KGD market for both the supplier and the user (today, high-volume KGD generally cost between 5% and 30% more than their packaged equivalents, while low-volume KGD can often cost several times as much). These and other KGD efforts will gradually increase MCM market viability.

However, bare die sales, whether known-good or not, will most likely always be small compared with packaged die sales, since multi-chip packaging will always be a relatively expensive form of microcircuitry. Even five years ago, when the military was frequently purchasing hybrids (the military accounts for about 80% of hybrid sales), bare die sales were a very small fraction of total IC sales. For instance, five years ago, Motorola die sales were only about 0.6% of total their IC sales.

3. How to Ensure KGD

There are four ways to ensure that a bare IC is "known good": 1) through the process under which the manufacturer fabricates the IC, 2) through the IC design, 3) through bare IC testing, and 4) through sample packaged IC testing.

Process: Nothing is more important than having a mature process. While testing at the end of the line can reveal problems, quality cannot be "tested-in". Thus, finding stable processes (six-sigma if possible), understanding process history, and assuring that the process has proper statistical process control are all first steps toward producing KGD. Process maturity dictates the degree of further KGD assurance required. For instance, high yield and favorable process statistics can often justify lower KGD assurance levels than using new or unstable processes.

IC Design: You cannot assure that a die works unless you can test it. IC designers use several design strategies (called design-for-testability) to make ICs testable. Besides providing extra pads for testing, designers enhance testability by using techniques such as scan-paths, built-in self test (BIST), boundary-scan, and test structures.

Scan-paths are register chains that, in test mode, configure as shift registers through which test engineers send test patterns. Using such shift registers enhances the controllability and

observability of each node in the circuit. That is, shift registers enable the circuit to set registers to certain values and determine whether they function correctly. Nodes in the IC that do not function properly cause faults. Engineers measure the comprehension level with which a scan path can test an IC in terms of fault coverage, defined as the ratio of detectable faults to the total possible faults.

BIST is test circuitry designed on the chip to enable an IC to exercise about 50% to 80% of non-random logic (PLAs, ROM, RAM, etc.) automatically. While extremely costly, the limited chip accessibility on MCMs often justifies using BIST. Also, by using BIST, the manufacturer does not need to disclose proprietary information such as test patterns for internal design features. BIST can be exercised at-speed without the loading effects or speed limitations associated with external test equipment. Finally, burn-in can utilize BIST by having engineers perform dynamic burn-in without supplying external vectors.

Boundary scan is a JTAG (Joint Test Action Group) standard (IEEE 1149.1) method where test engineers use a 4-wire serial bus as a test access for verifying bond wire integrity and assembly-level interconnects. This method employs a shift register chain amongst several chips on an MCM from the test data input pin, around each die's periphery, and finally to the test data output pin. Besides verifying interconnects, chips can use boundary scan as a gateway to internal device logic. This gateway facilitates using BIST at all assembly levels. While mainly a DC test, boundary scan also verifies parametrics such as input switching threshold, output drive, and slew rate. Its most powerful feature is its ability to drive I/O to specific known states as required for parametric tests. This typically would otherwise require thousands of test patterns to set up.

Test structures test the quality of the metallization, the dielectrics, and other material properties of ICs. Test structures come in three forms: 1) as entire ICs, 2) as circuits or transistors in wafer scribe lines, and 3) as part of an IC. As entire ICs (called drop-ins), test structures characterize the wafer on which they are fabricated. As circuits in wafer scribe lines, test structures characterize the wafer, but can only be used at wafer level, since sawing the wafers destroys them. As part of an IC, test structures, like BIST, are an expensive but effective way to test a particular IC.

Bare IC Testing: KGD testing includes electrical, mechanical and environmental tests (for a description of these tests, see section 4). Engineers use two basic approaches to electrically test bare ICs: with pressure contact and with metallurgical connections. Wafer probes and temporary carriers use pressure contact while semi-permanent and permanent carriers use metallurgical contact (see section 8 and 9 for discussions on wafer probes and carriers respectively). Bare IC electrical testing aims to rigorously test the die using low resistance connections that do not damage the IC pads. However, some dice require more testing than others. For instance, a state-of-the-art high-density memory that pushes the limits of a process' capability will most likely have a high infant mortality, requiring burn-in on every die (see "Burn-in" in section 4). Conversely, a part with a long history fabricated on a mature process line may require a less comprehensive test plan (for

examples of different testing levels for KGD, see section 6). This report continues to discuss bare IC testing later.

Sample Packaged IC Testing: We can gain quality and reliability information about an entire lot by packaging IC samples and performing tests on them. Thus, testing packaged IC samples from a given lot can reduce bare die testing needed. However, this requires close cooperation between the KGD supplier and the MCM manufacturer, and, in general, many statistics. Sample packaged IC testing espouses the QML philosophy, in that it promotes doing as much testing on each die as demonstrated necessary and then leaving the other tests out. In general, the less testing required on each die, the better, since less testing implies less handling. Handling, in many cases, may actually cause more defects than the tests detect.

The need for KGD goes down as rework costs go down. That is, in some cases, it may make sense to decrease KGD testing and plan on reworking where needed. Thus, trading off KGD costs with rework costs helps MCM test planners to figure out how much testing constitutes "known good-enough die". Rework costs depend on several factors including: 1) MCM materials (MCM-C withstands the heat required to remove die better than MCM-L), 2) die pad number and pitch (high number and low pitch are more labor intensive), 3) die-attach material (epoxy is relatively easy to remove), 4) die-to-substrate interconnect mechanism (tape automated bonding (TAB) and sometimes flip-chip dice can have pull strengths high enough to lift surface metallization), and 5) die costs (high die costs increase total rework costs).

The following MCM testing strategy illustrates a way to balance KGD testing with rework. Consider an MCM with a microprocessor, an ASIC, and several support dice. A smart testing strategy would involve the following: test the MCM substrate before committing any dice to the substrate. Then minimally test the support dice and commit them to the tested MCM. At this point, test the partial setup and plan to rework where needed. Then, fully test the microprocessor and ASIC and commit them to the MCM. Finally, test the entire assembly. Thus, this strategy commits small resources to testing the support dice and large resources to testing the complex and expensive dice. This approach minimizes reworking the complex dice, while exploiting the relatively low cost of reworking support dice (as support dice tend to have less I/O and cost less).

4. Tests For KGD

Tests for KGD can be grouped into six categories: 1) DC parametric tests, 2) AC parametric tests, 3) functional tests, 4) structural tests, 5) burn-in, and 6) other mechanical and environmental tests. MIL-STD-883 describes burn-in and many mechanical and environmental tests.

DC Parametric Tests: DC parametric tests measure analog voltage and current values at I/O pads under different I/O loading, temperature, and supply voltage conditions. Since these tests do not run at full speed, they typically run at wafer level. DC tests do not take

long to perform, and thus test the vast majority of ICs, whether further testing occurs or not. However, DC tests alone typically provide only about 85% confidence that an IC has no defects. DC parametric tests measure shorts and opens by applying current and measuring forward diode p-n junction voltage drops on I/Os. DC tests also include leakage tests (excessive current flow through internal paths), and measure parameters such as input switching thresholds, output voltage levels, output current source and sink capability, static supply current, and for CMOS circuits, dynamic supply currents where IDD varies with frequency.

AC Parametric Tests: AC parametric tests measure signal timing attributes to determine minimum, typical, and maximum timing values at differing supply voltages and temperatures. AC parametric tests require a much higher bandwidth than DC tests. Since wafer probes tend to have limited bandwidth, usually test plans can include only limited wafer level AC parametric tests. To do full AC parametric testing requires establishing a high bandwidth connection. Thus, AC tests normally occur after packaging an IC. For KGD, this implies using some kind of carrier (see "KGD Carrier Methods"). The NRE costs associated with AC testing can run from $2K to over $30K. AC tests measure propagation delays (input to output time), setup and hold times (verifies signal validity before and after asserting a second signal), signal timing (signal edge placement), pulse width (period), and clock frequency tests (duty cycle and period).

Functional tests: "Function" refers to the set of inputs and resultant outputs that the designer intends the device to process. Functional tests thus test that a device outputs meaningfully correct responses to a given set of inputs. Since function can only be interpreted by the designer, designers are responsible for developing functional tests. Ideally, functional tests verify that the device will function during actual system operation; thus functional tests ideally run at system level speed. Like AC tests, full-speed functional tests usually occur after packaging an IC (again implying using a temporary carrier for KGD), due to wafer probe bandwidth limitations. However, functional tests sometimes run at wafer level anyway, at lower speeds. In special cases, low device speed and a high bandwidth wafer probe may enable wafer level at-speed testing.

Functional tests, excepting non-random logic devices such as memories, do not thoroughly test every node in a circuit. Structural tests help test the nodes that functional tests miss.

Structural tests: "Structure" refers to the physical layout of logic elements, without regard to their function. Structural tests detect manufacturing defects by providing input to a device and comparing the output with expected results. Because structural tests do not limit input and output vectors to those the device would use for functioning, structural tests can test for many more faults than functional tests. Structural tests especially facilitate testing complex random logic devices such as ASICs, where functional tests particularly lack thorough fault checking.

Automatic test pattern generation (ATPG) tools normally generate input vectors and expected output vectors which analyze the device from a structural standpoint, without

regard to functionality. Structural tests rely heavily on scan paths and other design-for testability features for achieving high fault coverage (see the discussion on scan paths under "IC Design" in section 3). Since structural tests typically do not test for timing problems, they need not perform at operating speed. Thus, in some cases, engineers apply structural tests at the wafer level.

Burn-in: Burn-in exercises ICs at high supply voltage and temperature for several hours (for military applications, 168 hours and for commercial applications, anywhere from 10 to 168 hours). Burn-in exercises IC's in one of two ways: 1) static, applying a static voltage pattern to the circuit, and 2) dynamic, applying varying input patterns so as to flip the states of as many nodes in the circuit as possible. Burn-in screens "infant mortalities" which are parts that have imperfections (such as contamination and process variations) that do not cause failures during electrical testing but will likely cause failures within the first few operating months. Even as processes become more reliable, infant mortalities are inherent in every new design.

Performing burn-in on the assembled MCM rather than on each die separately may appear to cost less. However, performing MCM-level burn-in usually costs more and measures less than die-level burn-in. It tends to cost more because it detects problems later in the production cycle, and tends to measure less since it cannot control and observe nodes on each IC as effectively as die-level burn-in.

Some companies have "intelligent" burn-in which combines functional, programmable testing with burn-in in the same chamber. These systems can compute infant mortality rates as a function of burn-in time, establish optimal burn-in time per product, and correlate burn-in failure rate and life test data to determine field failure rate.

Other Mechanical and Environmental Tests: Engineers can perform several mechanical and environmental tests by packaging a dice sample from a given lot. Temperature and humidity tests, die shear tests, bond pads cross section, centrifuge, and passivation integrity exemplify such tests. MIL-STD-883, method 5008 and MIL-H-38534, section 4.3.2 contain procedures for performing what the military calls "element evaluation". Element evaluation refers to testing various parts of a hybrid, including the bare dice. Bare die element evaluation is the closest test procedure military specifications have to a KGD procedure. Therefore, we review what bare die element evaluation requires here.

Bare die element evaluation requires first that each die has an electrical test specification including electrical test parameters, values, limits and conditions. Second, it requires packaging a dice sample from each wafer or wafer lot, the number of which depends on the class (B and S for single chips, H and K for hybrids): for class B or H, it requires at least 10 per lot, and for class S or K, it requires at least 3 per wafer and at least 10 per lot.

Class B & H element evaluation calls for performing the following tests on packaged samples:

• *Internal visual, MIL-STD-883 method 2010:* This test uncovers surface defects in processing or handling and uncovers gross contamination or metallization problems such as pad damage and stains.

• *Initial, interim, post-burn-in, and final electrical tests, according to the die's specification:* These tests guarantee functional, AC, and DC compliance to data sheet parameters and to the functional and parametric specification. They also screen marginal units. For instance, leakage current variables analysis can screen out material with marginal oxides. Test engineers apply these tests before and after mechanical tests, after burn-in, and after the life test.

• *Wire bond evaluation, method 2011:* This test, while normally thought of as an assembly-level test, also tests for die issues such as bond-to-pad and pad-to-metallization adhesion. Wire bond evaluation consists of pulling the wires away from their bonds to find out when something breaks. This method detects bad bond-to-pad adhesion when the bonds breaks at low pulling force. It also detects bad pad-to-metallization adhesion when the metallization peels off the bond pad before the bond breaks.

For class S & K, add on:

• *Stabilization bake, method 1008:* This method simply stores the IC at high temperature for extended periods. It detects parameter degradation and failure mechanisms that arise due to prolonged increased temperature.

• *Temperature cycling, method 1010:* This method cycles the IC through high and low temperatures several (usually about 100) times. Such thermal cycles can be useful to screen out material with microcracks or abnormal residual or internal stress. Another useful test for detecting these potential problems involves subjecting the die to sudden changes in temperature (thermal shocks) .

• *Mechanical shock, method 2002 or constant acceleration, method 2001:* These tests detect problems with the metallization and lead systems.

• *Burn-in, method 1015:* See "Burn-in" above. To minimize handling, it is good to combine electrical tests with burn-in.

• *Steady-state life, method 1005:* This is basically an extended burn-in; that is, burn-in for 1000 or more hours (see "Burn-in" above). It intends to detect failure mechanisms beyond those associated with infant mortality.

• *Scanning electron microscope (SEM), method 2018:* This employs a 1,000X to 20,000X microscope that scans for interconnect metallization problems such as voids and poor (low) step coverage. Step coverage is the percentage of level-area metallization thickness present at junctions where the metallization connects or "steps" from one plane to another.

• *Dose rate induced latchup, method 1020:* This method detects the IC's susceptibility to the radiation-induced phenomenon called latchup. Latchup is a parasitic effect on CMOS devices where sufficient current injects into a substrate to cause a pnpn or npnp silicon-controlled rectifier-type structure to form. When this structure forms a low-impedance path from power to ground, the resulting high current flow can stop a device from functioning and may permanently damage or destroy it.

• *Total dose, method 1019:* This test measures the IC's susceptibility to accumulated ionizing radiation by injecting radiation from a cobalt 60 or gamma ray source into the oxide layer of the IC.

There is also one final test, neutron irradiation, method 1017, but do not use this method for space applications.

5. KGD Procurement and Information Exchange Issues

Procuring KGD is difficult for several reasons, all that stem from one basic reason: the industry lacks motivation to develop a KGD infrastructure. Companies tend not to commit large resources to KGD programs because bare die sales comprise a small fraction of total IC sales. Thus, most IC suppliers are slow to develop or acquire special equipment such as the KGD fixtures necessary for burn-in and testers. They also tend not to provide data sheet information unique to die applications. Supplying die data sheets would be a good first step toward placing emphasis on bare die issues.

Because the industry has placed little emphasis on bare die issues, the industry lacks bare die standards. Bare die issues that lack standards include mechanical dimensions (die size and pad locations), bare die circuit models, and test programs. For instance, the mechanical dimensions of die connected via tape automated bonding (TAB) and Chip-on-board (COB) differ from those that are connected via wirebonds. Also, vendors supply most bare die without circuit models such as functional models for designing and laying out larger systems. Finally, bare die test vectors often do not come in a format readable by the KGD tester's test machinery. Translation can take thousands of man hours. Clearly, establishing standards would greatly simplify procuring and subsequently dealing with bare die. To illustrate why standards would help, consider how many players contribute to developing MCMs.

In general, there are nine players involved in developing MCMs: 1) the IC designer, 2) the IC fabricator, 3) the KGD carrier (test equipment) manufacturer, 4) the IC (KGD) tester, 5) the substrate manufacturer, 6) the MCM (or hybrid) designer, 7) the MCM (or hybrid) manufacturer, 8) the MCM (or hybrid) tester, and 9) the end user. Bare die procurement physically occurs at two of these interfaces: from the IC fabricator to the IC tester, and from the IC tester to the MCM manufacturer. Yet we face procurement and information

exchange concerns not only at these interfaces, but at all interfaces. For instance, the IC designer holds responsibility for design-for-testability and test vector issues, which affect KGD-level and MCM-level testing. The KGD temporary carrier manufacturer must work with the IC manufacturer to assure that the carrier has an interposer that contacts the die's bond pads and distributes them to the tester (see section 9 and "MMS/TI" in section12). The IC tester and the MCM tester must understand each other's test strategies so that they minimize testing overlap, yet maximize test comprehensiveness. For instance, the IC tester must be aware of whether boundary scan is built into each chip to allow boundary scan at the MCM level. The end user must assure that their requirements are met at each interface. Die test houses (third parties) must get test vector software from the IC designer. And so on. Of course, in most cases, companies perform more than one of these roles. Even if there are only three or four companies involved, the procurement and information exchange issues can be very complex. The ways MCM manufacturers can acquire KGD exemplify how companies can perform more than one role.

There are three ways for MCM manufacturers to acquire KGD. First, MCM manufacturers can procure KGD from a die supplier such as Micron who will fabricate ICs, test them, and supply them as KGD. Second, they can procure KGD from a die test house (third party) who buys bare ICs, tests them, and supplies them as KGD. Third parties include Chip Supply, Elmo Semiconductor, Minco, and Semi Dice. Third, the MCM manufacturer can procure bare untested die from an IC fabrication facility and then test the die themselves. Micro Module Systems exemplifies this third KGD acquiring strategy. Each of these strategies entails a different KGD procurement approach.

Procurement contract developers must determine what information should accompany the die through the complex web of KGD and MCM designers, testers, manufacturers and users. By considering what activities bare dice go through, we can deduce what information bare die suppliers should include in a bare die procurement package. First, a die will have to be affixed into its final application, whether that be a single chip package, an MCM, or a hybrid. Thus, its procurement package should include information such as mechanical data (X, Y, and Z in GDSII format), a bond pad map including passivation opening side, jumper bonds, backside surface, metal and passivation material, and required backside electrical potential. Also, since a die will be tested in an MCM or hybrid at some point, the procurement package should also include boundary scan information and other testability features. Furthermore, considering that a die eventually must perform in an MCM or hybrid, information such as minimum and maximum junction temperature should accompany the die. Finally, the IC fabricator should indicate any process limitations so that engineers can account for them later.

Other procurement issues associate themselves with handling, marking, packing, shipping, and assembly. For instance, bare dice can be packed in sleeves, trays, waffle packs, pocketed tapes, and GEL-paks (see section 12, "Vitchem"). Each of these packing strategies have their own set of handling issues.

As has been illustrated, KGD procurement and information exchange is complex; hence, there presently lacks a standard approach. Due to KGD procurement complexity, MCC has developed a guideline for KGD procurement (see section 11), although it has not yet been widely accepted by industry.

One final point about KGD procurement. Because so many different people handle, assemble, test, and otherwise exercise bare dice, bare die suppliers concern themselves with a legally important issue: who has the liability when a die fails? And who, if any, is responsible to perform failure analysis in such an event? After all, a die can fail at assembly, test, burn-in, or in the field. Since failures can result from poor handling, poor assembly, poor testing, and poor system-level design as well as from defects and infant mortality, liability is indeed a complex issue, often implying lengthy contracts between the supplier and the customer. This is yet another reason IC manufacturers hesitate to sell bare die. Many IC manufacturers prefer to sell fully tested KGD rather than partially tested or untested die to reduce the chances that this liability problem will ever manifest itself. Or, they offer minimally tested or untested die with no guarantee.

6. Levels of KGD Assurance

Depending on quality and reliability requirements, rework costs, and the MCM-level testing strategy, KGD customers have different KGD assurance needs. To accommodate these different needs, many KGD suppliers offer several levels of KGD assurance, where different levels imply different amounts of testing and thus, presumably different degrees of quality and reliability. I will describe six such KGD plans from the following companies: Chip Supply, Elmo, Micron, Motorola, National, and Texas Instruments. In most cases, KGD suppliers are willing to negotiate a test plan with the user that differs from their standard assurance levels.

Chip Supply: Chip Supply sells KGD that undergo four levels of die qualification:

• 1.) *Functional wafer probe only.* This typically provides less than 90% confidence that the die is in fact a defect-free die.

• 2.) *DC, at-speed and functional wafer probe at elevated temperature.* This level, according to Chip Supply, provides between 80% and 95% confidence.

• 3.) *Lot acceptance test.* This strategy employs sample packaged IC testing (see "Sample Packaged IC Testing" in section 3). Chip Supply packages 38 ICs per lot and performs burn-in on each of them. If two do not pass, they throw out the whole lot. Chip Supply claims that this provides between 90% and 98% confidence. Recall that military standard element evaluation requires packaging only ten die per lot (as opposed to Chip Supply's 38) for this testing strategy.

• 4.) *Full KGD.* This level provides 100% AC, DC, functional, and at-speed testing over the specified temperature range, as well as burn-in and inspection on each die. Chip

Supply believes that this method provides at least 99.9% confidence that the die contains no defects.

For more information on Chip Supply, see “Chip Supply” in section 12.

Elmo Semiconductor: This supplier has five KGD assurance levels:

• *Level 1.* This method applies wafer probe, visual inspection, bondability test, and electrical test to each die. Also, Elmo packages a dice sample from each lot and performs burn-in, bond-pull, die shear, and gold back adhesion testing on each sample.

• *Level 2.* Same as level 1, with the option to wafer probe at elevated temperature, up to 160 °C.

• *Level 3.* Same as level 2, but add thermal cycling, interim electrical test, and burn-in.

• *Level 4.* Add SPC probe, SEM analysis, and life test to level 3. SPC probing involves AC and DC testing to parametric limits derived from process statistics rather than from data sheets. SPC-derived limits tend to be tighter than limits derived from data sheets.

• *Level 5.* Level 5 employs Elmo’s KGD coating process and contact assembly. For more information on Elmo’s unique level 5 KGD process, see “Elmo Semiconductor” in section 12.

Micron: Micron has three die qualification levels:

• 1.) *Standard probed die.* This level uses wafer probe at 65 °C and at 100 °C, as well as voltage stress tests.

• 2.) *Hot chuck speed-probed die.* This level matches the standard probed die level, but also adds an extensive wafer probe that tests cell margins, function, as well as parametrics and speed grading.

• 3.) *Fully tested and burned-in die.* This level includes complete AC and DC parametric testing at 85 °C and 125 °C, as well as burn-in at 125 °C and 145 °C. Micron fully warrants these dice to meet data sheet specifications. Micron claims that this level produces KGD quality and reliability equal to their standard commercial packaged product.

For more information on Micron, see “Micron” in section 12.

Motorola: Motorola has 3 levels:

• 1.) *Bare die.* This level uses DC and functional wafer probing at 25 °C only.

• 2.) *Known tested die*. This level involves full AC, DC, and functional testing at 0 °C, 25 °C, and 125 °C.

• 3.) *KGD*. KGD are the same as known tested die, with burn-in added.

For more information on Motorola, see "Motorola" in section 12.

National Semiconductor: National has five levels:

• 1.) *DC Probe*. National's products can all be purchased under this option. National typically uses this option only when the product has well-characterized DC, AC parameters over the full temperature range.

• 2.) *DC Probe with Lot Acceptance Test (LAT)*. This includes level 1 testing plus full test and burn-in on a dice sample from each lot.

• 3.) *AC and DC Hot Temperature Probe with LAT*. This extends level 2 to include AC and DC parametric testing at 25 °C and 125 °C for each die. Only selected products can use this option.

• 4.) *100% Die-Level Test at All Temperatures and Burn-In*. This represents their full KGD solution, and again only selected products can use this option.

Texas Instruments: TI has four levels:

• 1.) *Commercial*. This level involves DC wafer probe at 25 °C only. TI does not guarantee that these die will be defect free.

• 2.) *SM-L*. TI tests these dice at 0 °C, 25 °C, and 70 °C. They also perform 40X visual inspection per MIL-STD-883, method 2010. Burn-in is optional. TI guarantees that these dice will work.

• 3.) *SM-M*. SM-M uses the same tests as SM-L, but TI tests these dice at -55 °C, 25 °C, and 125 °C.

• 4.) *SM-P*. SM-P adds MIL-STD-883 tests and burn-in to the SM-M level.

7. Companies Involved with KGD

Who sells KGD? KGD have been sold since 1992, and presently there are at least 23 KGD suppliers:

1. AMD
2. AMI
3. Analog Devices
4. ATMEL
5. Chip Supply (third party)
6. Cypress
7. Elmo (third party)
8. Harris
9. Honeywell
10. IDT
11. IBM (c4)
12. Intel (11 devices offered as KGD)
13. Lattice
14. Maxim
15. Micron (Memory) (7 devices)
16. Motorola (Microprocessor, SRAM, DSP, RISC) (7 devices)
17. National (48 devices)
18. Quicklogic (FPGA)
19. TI
20. Triquint (ASIC)
21. UTMC
22. Vitesse
23. Xilinx (FPGA)

Third parties test ICs, but do not fabricate them.

Who proposes KGD testing methodologies (i.e. carriers, see section 9)? While only Chip Supply, Elmo, IBM, and Micron have carriers in production today, at least 36 companies are developing KGD carriers:

1. 3M
2. Acsist
3. Aehr Test Systems
4. AMP
5. BTQI
6. California Contacts
7. Chip Supply
8. Cinch
9. Elm Technology Corp.
10. Elmo Semiconductor Corp.
11. Fresh Quest
12. General Electric
13. Harris
14. Honeywell
15. Hughes
16. IBM
17. ISA
18. IST Associates
19. Lockheed
20. MCC
21. MCNC
22. Micro SMT Incorporated
23. Micron
24. MMS
25. Modular Automation
26. National
27. nChip
28. Nitto Denko America
29. Northern Telecom
30. Packard-Hughes
31. Plastronics
32. Sandia
33. Stanford
34. Tessera
35. TI
36. Tribotech

8. KGD Wafer Probe Methods

In order to test dice without encasing them in a package, engineers or automated equipment must probe them. In the past, cantilevered probes and controlled impedance multi-layer epoxy ring probe cards have tested dice at the wafer level. However, today's devices have revealed cantilevered probe limitations. Thus, a popular alternate probe

method, membrane probing, may eventually replace cantilevered probing. If current development efforts continue, we will see a very efficient membrane wafer probe technique in the future: wafer-level burn-in.

Cantilevered Probes: Cantilevered probes can test the die at wafer level, thus minimizing handling and maximizing efficiency. However, they become very expensive and impractical for high speed, high pin count devices. As the number of pins per device increases, cantilevered probes must get longer to access them. Because they must be long, these probes introduce the device to an uncontrolled impedance environment, which in turn provides low bandwidth. For power and ground probes, low bandwidth can lead to voltage drops. Also, the longer the probes, the more self-inductance each probe has. Furthermore, tips are unshielded from one another, causing cross-talk. These problems tend to keep cantilevered probes from effectively testing today's fast devices at operating speed. Thus, although they can perform DC testing and slow-speed functional testing, they tend to have trouble with AC testing and at-speed testing. Furthermore, cantilevered probe alignment and planarization become to burdensome and even impossible as die pad pitch decreases. The absolute limit is about 350-400 probes per device, and a more practical limit is about 200 probes per device. Today's devices often exceed these pin count limits.

To test at elevated temperatures, many die testing operations use an extension of cantilevered probing: hot chuck wafer probing. However, these probes introduce two more problems. First, it is difficult to maintain wafers at hot or cold temperature. Second, it is hard to remove the heat generated by each die.

Membrane Probes: Membrane probing avoids many problems associated with cantilevered probing. Membranes consist of compliant sheets of material (such as kapton) with bumps on them that align with die pads. Membranes provide a higher bandwidth than cantilevered probes because they use a ground plane to control impedance and to reduce unshielded signal paths. Bump alignment is more accurate than cantilever-style needle alignment, and does less damage to the pads. Membranes can support higher pin count than cantilevered probes, but still cannot support high pin count ASICs. Membrane probes tend to last longer than cantilevered probes and have higher contact reliability. Engineers can even use membrane probes for microwave testing by using membrane materials that provide low losses at tens of GHz. Many see membrane technology as a step toward wafer-level membrane probes, where each pad of each die on an entire wafer is connected via membrane simultaneously.

Wafer-Level Membrane Probes: Some companies are developing wafer-level membrane probes to facilitate wafer-level burn-in in the future. This will eliminate the need for packaged part and KGD burn-in. Also, it will be fully automatable, it will have a short cycle time, it will be applicable across many products, it will provide reliability learning, and will be a step toward full wafer test. The main challenges to be faced are differences in the thermal expansion coefficients of the silicon and the membrane probes, and routing to the vast number of I/O (some solutions propose routing to whole wafers that can have

greater than 30,000 I/O!) Other challenges include routing power throughout the wafer to dice that may have shorts, and building test structures into the probe card.

We can break wafer-level membrane probe approaches into three categories: 1) integrated probes (temporary interconnect requiring additive and subtractive post-processing), 2) silicon-based probes (provides a coefficient of thermal expansion (CTE) match, but is not very compliant), and 3) organic membrane probes (has a CTE mismatch and a low thermal range, but is relatively compliant). Companies experimenting with wafer-level membrane probes include Elm Technology Corporation, Hughes Research, Micro Module Systems, and nChip (see these companys' descriptions in sction 12).

Reducing unnecessary packaging costs drives wafer-level burn-in development. That is, by screening out more dice at wafer-level burn-in, they save the cost of packaging dice that would otherwise be later screened out by die-level burn-in. Facilitating KGD sales does not drive wafer-level burn-in development as much, since the industry expects KGD sales to always compare low with packaged part sales.

9. KGD Carrier Methods

A basic question to ask about KGD is: how can you test a die before it has the mechanical support offered by its final package? Only after assembling dice into packages do dice have adequate support for plugging them into burn-in boards and applying high speed tests. Thus, to test KGD, the dice need to have temporary mechanical support to distribute their signals. KGD carriers provide such support.

KGD carriers are physical support systems that provide the necessary mechanical means to distribute a die's I/O to a standard test socket. Thus, they facilitate die testing including burn-in, provide die protection, and reduce handling-induced problems. Since Micron marketed the first KGD carrier (Softool), many other companies have begun to search for their own solutions to the KGD testing problem.

While most companies agree on what characteristics a KGD carrier should have, they have not reached consensus on how to overcome problems associated with making temporary contact to aluminum pads on bare dice. Most agree that the ideal carrier would provide KGD assurance using existing test and burn-in equipment, provide good mechanical protection for the die, cause no electrical, thermal, mechanical, or environmental degradation to the die, have low contact resistance, and be cost-effective. However, many unresolved issues remain such as how to penetrate native oxides on die pads, how to achieve probe-to-probe compliance, and alignment. At least 29 companies have come up with different solutions to address these issues.

Carrier techniques fall into 3 categories: permanent carriers, semi-permanent carriers, and temporary carriers. Information about each follows. MCC conducted research determining

companies involved with each type of carrier as listed below (see "ARPA/MCC Effort", section 10).

Permanent Carriers : These methods provide mechanical support that attaches permanently to the die. Since these are essentially minimal packaging technologies, they limit final assembly options. However, the minimal packages ruggedize the die and create a wider pitch, enhancing the ability to do burn-in and decreasing problems with handling and bare die contact. No permanent carrier technologies are in production, except of course the standard tape automated bonding (TAB) process. The companies developing permanent carriers include:

1. Hughes Aircraft
2. Micro SMT
3. Northern Telecom
4. OMPAC
5. SLICC
6. Tessera

Many permanent carriers resemble the standard TAB process which I will describe here. The non-recurring engineering (NRE) cost for TAB usually ranges from 16 to 25 thousand dollars. TAB requires plating for gold bumps at the wafer level and uses a lead frame attached to a film strip or tape. The lead frame attaches to the gold bumps (using inner-lead bonding). After burn-in and test, engineers exercise the die from the TAB socket along with the inner lead frame and bond the die to an MCM (using outer-lead bonding). Design challenges include selection of the proper tape metallurgies and bonding methods, rework issues, and ensuring that the passivation layer will accommodate bumping. This process has several advantages: TAB uses a mature process that provides assembly automation, TAB module reliability is well proven, and it has built-in capability for full functional testing and burn-in. However, it also has many drawbacks: it requires device-specific tooling for tape fabrication, bonding, excising and forming, it requires a high NRE cost for tape design and tooling as well as high recurring tape and assembly costs, the process requires an additional wafer processing step (depositing bumps), the bonding approaches lack a standard, TAB parts require more board area for assembly than wirebonded or flip-chip parts, and TAB parts limit assembly options.

For other permanent carrier descriptions, see "Hughes" and "Tessera" in section 12.

Semi-permanent Carriers: Semi-permanent carrier strategies involve providing metallurgical connections to die pads for test access and then severing those connections after testing, so as to end with tested bare dice. This strategy has a minimal impact on process flow. These methods are by far the most mature, and are the only methods used today to actually produce KGD besides TAB. These methods especially suit low-volume, low pin count applications that can afford to pay more for KGD. IBM's Reduced Radius Removal (R3) technology (for Controlled Collapse Chip Connection (C4) interconnect only) has produced by far the most KGD. Some of these methods (such as IBM's R3) limit final assembly options. This category includes overlay approaches (such as GE High Density Interconnect (HDI), anisotropic conductive adhesive films, z-axis films, and other

like materials). The following companies have carrier technologies that are in production today:

1. Chip Supply Softab
2. Elmo Semiconductor
3. IBM R3
4. Micron Softool (licensed to Chip Supply)

The companies developing semi-permanent carriers not yet in production include:

5. GE
6. MCNC

Other companies not listed above use a method similar to Micron's Softool called sacrificial packaging. For this method, engineers temporarily bond the die to a package resembling actual single chip packaging. They usually use a low-temperature thermoplastic die attach and an aluminum-wire low-ultrasonic energy bonding technique called "soft-bonding". Sometimes engineers perform soft-bonding in reverse by bonding the wire to the package post before the die pad to eliminate "drag" on the bond. Sacrificial packaging's main advantage is that engineers can use standard test equipment. However, forming the temporary wire bonds tends to be labor-intensive and therefore costly and slow. Soft-bond scars may degrade subsequent bondability (JPL performed an SEM analysis of this: see "Soft-Bond Scar Study" under "Honeywell" in section 12). Also, some methods limit final assembly options. Finally, it is hard to determine whether soft bonds electrically perform the same way as final assembly bonds since the force applied (which may vary), the diffusion characteristics, the area of bonding, and the scrubbing method may all be different.

For more detailed descriptions of semi-permanent carrier companies, see "Chip Supply", "Elmo", "GE", "IBM", and "Micron" in section 12.

Temporary Carriers: These methods, like semi-permanent carrier methods, result in tested bare dice with minimal impact on test process flow, but involve pressure contact rather than metallurgical connection to die pads. This allows much faster electrical connection and disconnection compared with using semi-permanent carriers. Temporary carriers have the most potential for being low-cost, for facilitating high-volume production, for not limiting final assembly options, and for not requiring wafer post-processing. Consequently, the KGD industry is giving this carrier type the most attention. However, temporary carriers are the least mature. In fact, none are in production yet. They require high NRE costs and also high recurring costs associated with the thin-film interconnects between the chip and the fixture. The companies developing and testing temporary carriers are:

1. 3M Adapt-A-Pack
2. Acsist Associates Inc.
3. Aehr Test Systems/ Nitto Denko
4. BTQI
5. California Contacts Micro Beam
10. MP Inc.
11. Packard Hughes Membrane Probe
12. Plastronics
13. Qualhi
14. Sandia

6. Fresh Quest
7. IBM Dendrites
8. MCC
9. Micron KGD+
15. TI/Micro Module Systems
16. Tribotech
17. Yamaichi

For more detailed descriptions, see “Micron” and “MMS/TI” in section 12.

All carrier types vary according to what die types they can support (DRAMS, ASICs, microprocessors, etc.), what contact methods they use (temporary bonds, permanent bonds, scrubbing (deformation) contacts, non scrubbing (penetration) contacts), and what alignment methods they use (mechanical, manual optical, automatic optical). Many companies have patented their carrier approaches.

KGD carrier developers aim to make carriers reusable, to minimize cost. However, product cycle may limit their re-use. For example, assume that the IC manufacturer also performs KGD testing, and that a particular IC product requires a 168 hour burn-in time. This allows for 52 burn-ins per year. If the design goes obsolete in two years, they can only use the carrier 104 times even if it can physically handle many more uses. For carriers that contain two parts: a standard fixture and a custom interposer (for example, see “MMS/TI”, section 12), the product cycle limits only the interposer to 104 uses.

Using KGD carriers at the same company that performs IC manufacturing enables cost savings as the company amortizes carrier costs over many die sales. But carriers also enable the customer do their own KGD testing and thus procure die from suppliers who do not offer KGD.

Carrier Issues: Carriers have many challenges associated with them. This explains why companies propose so many different solutions. Pad and probe issues include contact force and interface durability (avoiding pad and probe interface damage), number of times probes make contact with die pads (multiple probing tends to degrade die pad bondability), contact integrity (including contact planarity and materials used), probe-to-pad alignment (accuracy, tolerance, repeatability, mechanical versus optical alignment), and contact point integrity. Durability issues include carrier lid, latch, and support durability, substrate durability, socket durability, carrier-to-socket and socket-to-board contact durability, and overall carrier durability after high temperature burn-in, thermal excursions, multiple mating cycles, and mechanical stresses. Other carrier issues include IC contamination or surface damage problems due to burn-in or other test environments, power and signal distribution, thermal management, and the ability to automate the insertion and testing process.

10. KGD Infrastructure Development Programs

There are three major programs that concern themselves with making MCMs commercially viable: ARPA/MCC, Rome Labs/Ratheon, and RELTECH. Since MCM viability depends on KGD, each program addresses KGD to some degree. ARPA/MCC

has devoted its entire program to KGD, while Rome/Ratheon and RELTECH focus on MCMs in general.

ARPA/MCC KGD Program: MCC is a research and development consortium that finds problems and subcontracts vendors to solve them. Funded half by ARPA and half by industry, MCC has surveyed over 40 companies that propose KGD carrier solutions (see section 9). They have also organized an industry consortium to write a KGD Procurement Guideline Specification (co-sponsored by Sematech, see section 11) and to identify and improve KGD strategies that exist in industry. Their overall objective is to resolve issues for supplying and procuring KGD to foster industry acceptance and confidence in Application Specific Electronic Modules (ASEMs) and MCMs.

The MCC KGD program consists of two phases. Phase I has consisted of: 1.) KGD cost analysis, 2.) surveying proposed and existing KGD testing methods in industry, 3.) developing Technology Assessment Guidelines (TAG) to evaluate each KGD testing method's effectiveness, and 4.) scoring each KGD testing method according to the TAG. Phase II will deal with validating some of these methods. The total budget for both phases is 3 million dollars.

Cost Analysis. For the cost analysis, MCC used a spreadsheet-style cost model to compare 1.) dice placed in a temporary package or carrier for burn-in and test and then shipped as bare dice (KGD) with 2.) dice assembled into a permanent, single use package for burn-in and test. This comparison helps determine whether it is cost-effective to ship KGD. According to this cost analysis, the major cost drivers concerning KGD cost-effectiveness as compared with their equivalent packaged parts are:

• *The type of packages used in the comparison:* Since ceramics cost much more than plastics, it is much more cost effective to provide KGD when compared to ceramic parts than when compared to plastic parts.

• *The die pin count:* KGD with a high pin count are more cost-effective than KGD with low pin count since you save more on package interconnection costs.

• *Cost of carrier and carrier-to-die interconnect:* Less expensive carriers and carrier-to-die interconnects provide more cost-effective KGD.

• *Number of times a single carrier can be reused:* When considering carrier reuse issues, the limiting factor may either be the carrier lifetime or the product lifetime. If carrier lifetime is the limiting factor, then carriers that can be reused many times provide for more cost-effective KGD because the carrier costs are amortized over more KGD tests. On the other hand, if product lifetime is the limiting factor, then short burn-in time and long product life provide more cost-effective KGD, since they increase the number of times a carrier can be reused before the product becomes obsolete.

Technology Assessment Guidelines. MCC has gathered experts in the industry to determine what KGD carrier characteristics best satisfy KGD testing demands. This effort has resulted in Technology Assessment Guidelines (TAG) which outline desired KGD carrier characteristics. The TAG aims to define requirements for processes, materials and equipment capable of performing all actions necessary to generate and deliver bare, TABed, and bumped die with quality and reliability equal to their packaged equivalents.

MCC "scored" each surveyed KGD testing strategy using a weighted line-item scoring system by comparing each KGD strategy to the TAG. A perfect score is 175. The following KGD testing strategies scored 170 or higher: Aehr, Micron KGD+, Qualhi, MMS/TI, Tribotech, and Yamaichi. However, these scores reflect comparisons to a generic requirement list that tends to favor temporary carrier solutions. Requirements for a specific application may be quite different, causing the scoring to come out differently.

Micron Softool as well as most sacrificial packaging (semi-permanent carrier) strategies do not score well when evaluated against the TAG because they can only handle low I/O count, are labor-intensive, and often limit final assembly options. Carriers have much better flexibility, commanding higher TAG scores (they can often accommodate array pads, bumps, TAB, flip-chip, high I/O, etc.)

The TAG rules, outlined below, provide good insight into what is generally valued when selecting a KGD carrier technology:

• *Device types:* Shall be capable of handling and processing all active device types including: 1) analog, digital, and mixed devices, 2) bipolar, CMOS and BiCMOS devices, 3) silicon, silicon-on-insulator (SOI), and GaAs devices, 4) all device types such as memories, microprocessors, ASICs, etc., and 5) devices with peripheral bond pads, array bond pads or bumped bond pads.

• *Cost:* The cost shall not be significantly higher than that associated with packaged dice.

• *Die size:* 2500-500,000 square mils with a tolerance of at least +/-0.5 mils.

• *Aspect ratio:* The aspect ratio shall be a maximum of 3 to 1.

• *Die thickness:* 10-30 mils. The carrier must have a die thickness tolerance of whatever is less: 1 mil or 10%.

• *Planarity:* The carrier must allow for up to 1.0 micron pad height variation, without degrading the IC planarity.

• *Die interconnect metallurgies:* The carrier shall be able to maintain reliable contact with aluminum, gold, or solder and cause no damage.

• *No rule changes:* The methodology must not require changes to device design rules, wafer fabrication rules, or wafer mount and saw rules.

• *Wafer/die probing:* The KGD methodology shall not prohibit wafer probing or require new probe equipment. The probe shall not contact passivation. The pad damage from the probes shall pass MIL-STD-2010.6.

• *Test capability:* Shall be capable of BIST, basic functional test, and connection to external devices.

• *Die contact:* Shall be capable of contacting die pads in passivation wells up to 1.5 microns in depth, and ideally up to 8.0 microns in depth.

• *Contact resistance:* The contact resistance shall be compatible with bandwidth.

• *Pin 1 indicator:* Shall have pin 1 indicator.

• *Test rules:* Shall operate from 0 to 125 °C, have a contact resistance of less than 0.5 ohms, have a clock frequency of at least 100 MHz, be able to contact peripheral or array pads, accept aluminum, gold, and Solder pad metallization, have greater than 200 micron pitch (for high I/O, greater than 150 microns), have greater than 100 micron pitch (for high I/O, greater than 75), have a characteristic impedance of 50 ohms +/- 10%, have a bandwidth of 500 MHz, have a power handling capacity of 3W/cm^2 (for high I/O, 10 W/cm^2), and allow at least two touchdowns per die. For burn-in, it shall allow for a die maximum temperature of 175 °C, a maximum ambient temperature of 150 °C, and a clock frequency of a least 20 MHz.

• *Pack and ship:* Shall follow pack and ship guideline per the KGD Procurement Guideline (see section 11).

• *Optical inspection:* Shall allow optical inspection.

Phase II Plan. The phase II plan consists of three subphases: evaluation, qualification, and product insertion. This phase will last about two years, if funded.

• *Subphase I, Evaluation:* IC suppliers will supply die for four or five of the 24 KGD carrier suppliers identified in phase I. Die suppliers will also supply all documentation necessary for socket and carrier fabrication, design and procure the test board, and perform thermal analysis. MCC or MCC subcontractors will perform the following tests on each carrier methodology: 1) die and interconnect planarity, 2) die damage or contamination, 3) temperature cycling, 4) contact resistance, 5) maximum clock frequency, characteristic impedance, and bandwidth, 6) die damage or contamination after two touchdowns, 7) burn-in and test, 8) thermal resistance, and 9) contact resistance during burn-in.

• *Subphase II, Qualification:* Based on each carrier's ability to perform test and burn-in, MCC will select one or two carriers to undergo phase II. Phase II consists of qualifying the IC supplier which uses each carrier selected for subphase II. Each IC supplier will qualify their line to develop their capability to supply KGD executing the following tasks as a minimum: 1) modify existing production device fixtures, loadboards, test programs, etc. to work with the carrier test socket, 2) supply functional die for the qualification plan, 3) visually inspect each die after assembly into carriers, 4) functionally test each die in each KGD carrier, 5) burn-in each die using each KGD carrier, 6) package the devices to standard production requirements, 7) perform an accelerated life test, 8) perform temperature cycling, 9) provide a final report documenting all testing and test results

• *Subphase III, Product Insertion:* Using the IC supplier's qualified process, KGD will be used in an application. The IC supplier must perform failure analysis on all failures as they occur and send the results to MCC. Finally, MCC will acquire data about KGD used in each application to determine the effectiveness of each KGD process.

Rome Labs/Raytheon Program: Unlike ARPA/MCC, which focuses strictly on KGD, this program focuses on all processes used to create a high-reliability MCM. They call this program the "Known Good Devices" program. The Known Good Devices Program aims to assure that each of the following MCM-related materials and processes are "known good": 1) wafers, 2) wafer saw, 3) dice, 4) substrates, 5) test techniques (including testers and fixturing), 6) computer aided engineering (CAE) tools, 7) IC and MCM design, 8) specifications, 9) design for testability, and 10) design for radiation. The program emphasizes testability at the die and wafer level.

The program divides into two phases: the study phase (November, 1993 to May, 1994) and the demonstration phase (May, 1994 to July, 1995). During the demonstration phase, Ratheon and subcontractors (Chip Supply, Boston University, and N-Chip) will pick one or two known good device strategies identified during the study phase and fabricate MCMs using them.

Since this program has a more general emphasis than ARPA/MCC, they pay relatively little attention to KGD. So far, their KGD study includes 1) researching the effectiveness of traditional burn-in and screening, 2) putting together a spread sheet to compare KGD carrier techniques with respect to mechanical and electrical capability, manufactureability, and cost effectiveness, and 3) studying reliability issues associated with Chip Supply's Softab and Softool techniques. They have not released their findings yet.

RELTECH: This program's deliverable is an Electronic Industry Association (EIA) MCM Qualification Specification. RELTECH places emphasis on advanced packaging reliability, and is studying several MCM packaging solutions including solutions by GE, IBM, ISA, Motorola and N-Chip.

Like the Known Good Devices Program described above, relatively little emphasis is placed on KGD. RELTECH makes the following recommendations for minimizing the

KGD problem: 1) work closely with IC manufacturers, 2) use the chip supplier's extensive test capability, 3) eliminate oxide-related failure mechanisms on CMOS devices by screening using 30% over voltage stress, and 4) use BIST with ASICs.

11. KGD Procurement Guideline

A working group set up by MCC and Sematech has written a KGD Procurement Guideline Specification. The working group intends KGD customers and suppliers to reference this specification in both commercial and military KGD procurement contracts.

The effort to write this specification began in January, 1992. The working group, including die suppliers and MCM integrators, submitted the first draft to JEDEC in September, 1992 for standardization. The JEDEC JC-13 subcommittee on KGD has slightly modified the draft. Motorola, Intel, National, TI, and Harris are in process to comply with this specification.

The original specification addresses only wirebond interconnection strategies since MCM assemblers physically and electrically connect flip-chip and TAB-interconnected dice differently than wirebonded bare dice. Thus, the working group added two addendums to the KGD specification in July, 1993: one to address the additional bumps on the die surface of flip-chip dice, and the other to address the leadframe supplied along with TAB-interconnected dice.

The specification aims to provide the customer with dice whose electrical performance and reliability are as good or better than if the dice were packaged. Toward this end, it addresses supplying the extra information a customer needs beyond packaged part information. This information includes design data, die electrical test data, quality assurance provisions, reliability provisions, change notification, packaging and shipping information, storage information, as well as other information. Some of this information may be proprietary. In such cases, the manufacturer may not agree to supply the information, or the customer may sign nondisclosure agreements.

While this specification aims to assure KGD as fully as possible, it acknowledges that KGD cannot be assured in the same manner as packaged parts. This is because KGD require more cooperation and information exchange between the vendor and the user. For instance, the vendor's warranty depends on the customer's ability to follow the vendor's quality controls. Also, for customer-designed ASICs, the supplier and the customer must agree about design for testability techniques. When different companies simultaneously design the die and the module, they must agree on procedures for information exchange. This specification attempts to provide provisions for exchanging information amongst users, testers, designers, and manufacturers.

The specification recommends that the KGD vendor supplies various data to the customer. While the specified data represents a rather thorough KGD information list, most procurement contracts will likely reference only part of the specification.

A breakdown of the recommended vendor-supplied data follows. First, each KGD must have a unique part number. The rest of the recommended KGD requirements are broken into 1) design data, 2) die electrical test data, 3) quality assurance provisions, 4) reliability provisions, 5) change notification, 6) packaging and shipping information, 7) storage information, and 8) other information.

1. Sample Die Types: To begin, the specification distinguishes between four sample die types that the customer may request from the vendor: 1) packaged equivalents for system prototyping (TAB dice may not be available packaged in all cases), 2) reject mechanical samples with the same layout, orientation and pad metallurgy as the final KGD, 3) proof-of-design parts with the same form, fit, and function as the KGD, and 4) KGD representatives with design or manufacturing changes.

2. Design Data: The specification calls out several design parameters that the user may find useful. Parameters common to wirebonded, flip-chip, and TAB-interconnected dice are: 1) die dimensions with tolerances (for flip-chip devices this includes bump dimensions and bump-to-bump dimensions), 2) feature sizes, 3) bond pad map (for wirebonded devices only) including available bonding area and passivation opening size, 4) pin-out list, 5) test pad identification, 6) backside surface material and surface finish type and thickness, 7) maximum/minimum die junction operating temperature, 8) conditions that affect die function (known physical process limitations such as temperature, pressure, or ultra-violet light sensitivity, critical temperature environments, components normally connected to or used within the packaged part such as trimming capacitors, and die attach materials for wirebonded dice only), 9) final die passivation material and minimum thickness, 10) pad metal composition (for wirebonded devices only), 11) maximum and minimum pad metal thickness, 12) die bottom surface electrical potential, 13) maximum bias voltage and current, and 14) minimum current carrying requirement for the user's substrate (for high power applications).

The following design parameters apply to flip-chip devices only: 1) bump map including electrical contact, mechanical stabilization, and heat conduction, 2) bump metal composition, volume, and height, 3) guaranteed die edge smoothness and smoothness tolerance, specifying die edge perpendicularity, parallelism, and taper, 4) minimum distance from most peripheral bump to edge of diced die, 5) physical requirements for mating substrate pads such as heat flow capability and pull strength, 6) identification of polyimide dielectrics or other materials sensitive to plasma cleaning or bonding conditions and thus affect the attachment process, and 7) identification of any post-die manufacturing coatings intended to protect the die in shipment, along with the processes and chemicals required to assure good connections.

The following design parameters apply to TAB-interconnected devices only: 1) TAB frame map identifying reference to standard TAB outline in JC11.4-UO-018, TAB Packaging Family Outline or specifying TAB frame dimensions, electrical potential, pin ID, and test designator, 2) tab part map with alignment or registration marks identified (to

facilitate optical pattern recognition), 3) identification of polyimide dielectrics or other materials sensitive to plasma etch cleaning or bonding pressures (to facilitate tab leadframe attach), 4) identification of any post manufacturing surface coatings intended to protect TAB leads in shipment, along with process and chemicals for removal of these coatings (to facilitate proper TAB usage).

3. Die Electrical Test Data: The specification calls for a design-for-testability (DFT) description including descriptions for: 1) redundancy, 2) control fuses, 3) error correction, 4) ad hoc vectors, 5) structured, 6) boundary scan including IEEE 1149.1 device boundary-scan description language model, 7) BIST, and 8) control fuses (for flip-chip devices). The specification also calls for exceptions to the supplier's packaged die data book.

4. Quality Assurance Provisions: The specification recommends that the manufacturer have one or more of the following QA provisions: 1) MIL-I-38535 QML certification, 2) MIL-STD-883 compliance, ISO 9000 compliance, 3) National Electronic Component Quality Audit, 4) JEDEC JC 19C compliant, 5) internal quality control methods, 6) die DPM (defects per million) due to all causes (such as electrical reference to the data sheet, visual, mechanical, missing or low volume bumps, including definition of bump rejection criteria (for flip-chip devices), reject versus cosmetic defects, failures due to improper mechanical contacts between die and TAB frame (for TAB devices) such as missing or broken TAB leads, or improper leadframe contacts, 7) electrical test agreed by vendor and user, 8) quality control methods specific to flip-chip devices such as die bumps, or 9) quality control methods specific to TAB devices such as specialized process controls or inspection systems, post-manufacturing die coatings, or packing containers intended to preserve die quality. Visual and mechanical requirements should have an emphasis on bond pad damage and be based on MIL-STD-883, method 2010, or MIL-H-38534. Best commercial practice or element evaluation (MIL-STD-883, method 5008) should guide die acceptance testing.

5. Reliability provisions: The specification recommends that the manufacturer have one or more of the following reliability provisions: 1) burn-in data including PDA (percent defective allowed), 2) life test data based on comparable packaged parts including FIT rates (failures in time), 3) long term failure rates, 4) historical fabrication process yield data, 5) statistical process control, 6) in-line monitors, 7) end-of-line monitors, 8) baking, 9) temperature cycling, 10) bump reliability testing and failure modeling (for flip-chip devices), or 11) TAB interconnection failure modeling and TAB lead reliability testing (for TAB devices).

6. Change notification: If the die complies with MIL-STD-883, MIL-S-19500, MIL-H-38534, MIL-I-38535, or any other appropriate military document, the following applies. The following requires immediate notification: 1) degradations in quality and reliability and 2) unanticipated changes in QA provisions. The following requires three months advanced notice: changes to 1) die size, 2) die thickness, 3) size or location of contact pads, 4) glassivation, 5) bond pad opening, 6) metallization, 7) die electrical data, 8)

mechanical handling requirements, 9) transportation protection requirements, 10) shipping requirements, 11) storage requirements, 12) bumps (i.e. location, composition, hardness, height or uniformity of bumps for flip-chip devices), 13) TAB outline or location or TAB lead configuration (for TAB devices), or 14) anticipated changes in die quality and reliability or QA provisions. Finally, discontinuation of die type requires a minimum of 6 months advanced notice.

7. Packing and shipping: The specification recommends that the supplier ensure die protection from: 1) mechanical damage (including bump mechanical and chemical integrity for flip-chip devices, and the following for TAB devices: TAB lead mechanical and chemical protection thus assuring proper TAB bonding, and tape reels or other container integrity), 2) electrostatic discharge (ESD), and 3) contamination. Also, the die should have traceability to its wafer lot for a minimum of 5 years because the customer may want to make inferences regarding die quality from lot and wafer characteristics. Note that the user must also maintain this traceability.

KGD shipments should include the following information: 1) supplier name, 2) generic die type, 3) revision number, 4) wafer lot number, 5) links to corresponding documentation, 6) guaranteed speed grade, 7) KGD quantity, 8) product specific information such as ESD, light sensitivity, and atmosphere required upon opening, 9) ship date, and 10) wafer number if required.

8. Storage: The specification recommends that engineers store KGD under the following conditions: 1) using ESD protective materials, 2) in an inert gas or dry air atmosphere, 3) with storage temperature between 65 and 75 °F, 4) with humidity at less than 30%, and 5) with particles in the air according to class 1000 (FED-STD-209).

9. Other information: Finally, the specification suggests that the following data also be included in a KGD procurement contract, as negotiated: 1) suggested die attach material, properties, and pressure, 2) suggested bond wire size and down bonds (pad number and electrical potential), 3) suggested bonding methods, 4) unique materials or exposed surfaces requiring special attention during assembly, 5) suggested wire bonding sequence, 6) suggested quantity of bond wires on power and ground pins, 7) suggested stitch-bond connection between ground pins, 8) suggested lid material and sealing procedure, 9) packaged component ESD sensitivity, 10) environmental conditions necessary to ensure long term die reliability (sealing atmosphere, etc.), 11) power dissipation versus frequency, junction temperature, loading, and location on die surface 12) fault coverage and grader used, 13) test patterns in WAVES (Waveform and Vector Exchange Specification, IEEE 1029.1), 14) die driver and I/O buffer SPICE models, 15) VHDL structural or behavioral model, 16) parameters actually tested versus parameters guaranteed by characterization, correlation, or inference, 17. maximum peak die assembly process temperature and times, 18) junction temperature versus die backside temperature, 19) dimensional data in GDS Stream II Format (Valid Logic Systems trademark) such as top metal features and glassification mask layers, 20) backside surface roughness, 21) environmental conditions and storage duration prior to shipment, 22) saw kerf shape, 23) unusual die material

properties (for example, SiC backside coatings), 24) moisture resistance data (for non-hermetic applications) using data from packaged part accelerated tests, such as 85% relative humidity-tested at 85 °C and autoclave, and 25) alpha particle die coating and recommended die coating including material, thickness, and application process.

The following refer to flip-chip devices only: 1) recommended bumped die attach process including heating process (hot bar, furnace, infrared, laser) and compatible chemical and materials, 2) recommended bumped die removal and rework process including compatible chemicals and materials, 3) recommended re-use criteria and process (e.g. bump reflow) for reworked die prior to subsequent reattach, and 4) recommended materials, conditions and preparation for substrate bumps mating to die bumps.

The following refer to TAB-interconnected devices only: 1) recommended TAB excise method and attach process including bonding parameters (thermosonic bonding, laser, etc.) and compatible chemicals and materials, 2) recommended TAB removal and rework sequence process including compatible chemicals and materials, 3) recommended re-use criteria and process for TAB contact reprocessing prior to subsequent reattach, and 4) recommended materials, conditions and preparation for substrate bumps to which assemblers should attach TABed die.

12. Manufacturer KGD Programs And Perspectives

I have compiled KGD information by personally talking with the following representatives from various companies involved with KGD:

Company	Contacts	Phone
Chip Supply	Jim Rates	(407) 298-7100
Cyprus		(818) 753-5800
Elmo Semiconductor	Larry Duncan	(818) 768-7400
GE	Glen Forman	(518) 387-7420
Harris	Matt Salatino Celeste Null (MicroRel)	(407) 724-7563 (602) 968-6411
Honeywell	Mike Mitchell Bill Jacobson Chuck Utrius	(612) 954-2428 (612) 954-2332 (612) 954-2052
Hughes	Richard Dinsmore Dennis Elwell Mark Stelling	(714) 759-6512 (714) 759-7386 (714) 759-2507
IBM	Dave Polak	(703) 367-3458
IDT	Gary Connor	(408) 944-2080
Intel	Jose Avalos Allan Ignatowski	(602) 554-2242 (602) 554-8476
Irvine Sensors	Tony Johnson Rafael Some Dave Castrucci	(802) 769-1931 (802) 769-2746 (802) 860-6800 ext. 13

Lattice	Jim Krebs	(800) 327-8425
LSI Logic	Mike Stover	(408) 433-7404
Martin Marietta	Jack Thornton	(407) 356-1481
MCC	Marshall Andrews John Prokop Larry Gilg	(512) 250-2732 (512) 250-2726 (512) 250-3044
Micro Module Systems / Texas Instruments	Howard Green Fariborz Agahdel	(408) 864-5986 (408) 864-7437
Micron	Jerry Johnson Mike Grant	(208) 368-3958 (208) 368-3851
Motorola	Ev Sherwood Don Kost Phou Nugyn	(602) 897-5043 (602) 897-3791 (602) 441-6512
Phillips	Steve Clark	
TI	Steve Martin	(915) 561-7205
Triquint		(714) 261-2123
TRW/ESL	Paula Hurt Don Haislet (ESL)	(310) 812-1576
Unisys (Paramax)	Chuck Packard Chuck Kryzak Don Meyer	(612) 456-0275 (612) 456-4853 (612) 456-2509
Westinghouse	Frank Marcinko	(410) 765-1958
Xilinx	John Pierce	(818) 865-6220

A brief synopsis of what I've learned about each company follows.

Chip Supply: Chip supply is a third party KGD testing house. That is, they purchase bare dice from IC vendors, test them, and sell them as KGD. They sell mostly KGD, but do custom packaging as well. One of their ongoing KGD customers is National. They test hundreds of thousands of KGD using one of four techniques: 1) Softab, 2) Softool, 3) Chip-on-Substrate (COS), and 4) TAB.

Softool. Micron developed Softool, a sacrificial package method, and licensed this technology to Chip Supply in 1993. This method involves wirebonding the die to a temporary package for test and burn-in. The light adhesion bonds leave a mark similar to a probe mark. They use a thermoplastic adhesive to bond to the temporary package (see "Semi-permanent Carriers", section 8). This method requires a low NRE, but is highly labor intensive, and is limited to dice with less than 28 pins. Thus, the method is good for low volume (less than 500 dice), low pin-count applications.

Softab. Chip Supply prefers to use Softab rather than Softool whenever possible due to its efficiency and its capability to test high I/O, fine pitch ICs. Softool resembles TAB in the following ways: it applies only to dice with peripheral aluminum pads, dice must be gold bumped at wafer-level, it requires NRE costs associated with tooling ($16K plus the cost

of the test software), and they attach a lead frame to facility test and burn-in. It differs from TAB in that the inner lead bonding (ILB) to the lead frame is "soft" (i.e. they apply the bonds at lower force, power, and time), allowing them to remove the lead frame to be removed after testing using a modified pull tester. Finished die have gold plated bumped bond pads sealed to the glassivation for increased reliability (gold bonded to gold provides a high-reliability interconnection). Also, gold bump thickness can be varied (20-25 microns) to accommodate different final assembly processes including high-density interconnect (HDI). However, the bumping process may cause defects and limits final assembly to gold wedge or ball wirebonds. Finally, the cooling requirements for high power dynamic burn-in may cause difficulty.

COS. The COS process involves attaching the die directly to a custom ceramic substrate with epoxy. The substrate, which coincides with the die's mechanical characteristics, has pads that fan out to a burn-in test socket. Engineers wirebond the die to these pads with 1.5 mil wirebonds. After test and burn-in, they trim the substrate 30 mils outside the die periphery and attach the substrate with attached die to the final application. This method requires low NRE costs, and allows bond pad relocation.

TAB. For a description of TAB, see "Permanent Carriers", section 9.

Cyprus: Cyprus does TAB, using a plastic spring loaded fixture to do speed functional tests and burn-in. This spring loaded fixture applies no stress or strain on the TAB assembly.

Elm Technology Corporation: Elm is working on a solution for wafer-level burn-in. They are developing a micro-machined silicon membrane technology with micro fabricated probe tips, designed to probe the entire wafer.

Elmo Semiconductor: Like Chip Supply, Elmo is a third-party KGD testing house. Half of their business (measured in dollars) is selling KGD. The other half is divided between custom packaging and MCM design and fabrication. Their competitors are Chip Supply and Minco (Minco works also with Austin Semiconductor who bought Micron's military assembly).

Five years ago, when the military was buying lots of hybrids, Elmo produced 3,000,000 KGD per month to support them. Now, Elmo only sells 600,000 die/month. However, in one way, Elmo benefits from the military market collapse. That is, as military sales fall, large companies that have high-volume military lines can no longer keep these lines running. Thus, they give their remaining business to small businesses that support low-volume lines, such as Elmo.

Elmo's "fifth level" KGD Process. Elmo offers five KGD assurance levels (see "Elmo Semiconductor", section 6). The fifth level involves coating the die surface with a special organic material, creating vias to the die pads, and adding an enlarged pad on top of the coating. This process is compatible with wirebonded, flip-chip and TAB-interconnected

die. The process involves a $5K NRE cost and a $250 recurring cost per wafer (a 10,000-volume, $40 SRAM tested by this process required $7.25 per die for KGD testing). This method has three major benefits: 1) the coating acts as environmental and handling protection, 2) the enlarged pads over the coating provide a very low pad damage ratio, and 3) the coating and enlarged pads improve reworkability.

The coating forms a strong mechanical barrier, 10 microns thick, which solves many handling problems. In particular, it protects against mechanical damage due to scratching the die during wirebonding, die attach (i.e. using a collet to place die on substrate), visual inspection, and removing the die from the waffle pack (or other container type). It also protects the die from problems associated with wirebonding. The combination of the added coating and added enlarged die pad metallization provides a 12 micron protective barrier between the bond and the die. Without this coating, excessive force applied during wirebonding could cause cracks that lead to leakage paths through the oxide underneath the fractured aluminum pads. Also, without this coating, uncentered wirebonds could crack the passivation around the pads. Besides protection from handling problems, the coating acts as an alpha particle barrier and as a shock absorber.

To perform tests and burn-in, Elmo places the die in a temporary package resembling the package to be used in the final application. Elmo uses mainly ceramic side-brazed hermetic DIPs, bottom-brazed FPs or LCCs, or standard PGAs as temporary carriers. Elmo uses a thermoplastic die attach that is soluble in alcohol. They can use one of several thermoplastic films to meet thermal and electrical conductivity requirements. The end-user has two options for final die attachment: 1) remove thermoplastic to use standard die attach, and 2) leave some thermoplastic from the temporary die-attach as a preform for final thermoplastic die attach.

A step-by-step summary of Elmo's fifth-level KGD process follows: 1) receive the wafer, 2) perform cursory visual inspection on a dice sample, 3) take a die photograph, 4) develop the mask for the KGD process, 5) take the wafer to 100% visual inspection, 6) mark rejects, 7) put an organic dielectric on the wafer surface, 8) make windows on the pads with 40-50% angular sides to provide good step coverage for the additional die pads, 9) add an additional 2 micron-thick die pad (about 5 times as thick and twice as much area as a normal pad) on the added dielectric's surface (they try to put the new pad over the ESD circuitry associated with the original pad to avoid crosstalk), 10) visual inspection, 11) wafer saw, 12) wafer sort (throw out marked rejects), 13) 100% visual inspection, 14) attach the die to a temporary package, 15) wirebond with ball bonds to the area farthest from the original bond area, 16) perform destructive bond pull on the die sample, 17) seal the lid with solder or with the die-attach thermoplastic (using this thermoplastic allows more lid seals so they can use the temporary package more times), 18) do any screening (typically includes stabilization bake, temperature cycling, centrifuge, initial electrical test, burn-in, and final electrical test), 19) heat the die, remove the lid and clip the bonds leaving the ball bonds on the pad (this way, engineers cause no damage to the pad by trying to shear the ball off), 20) visual inspection, 21) clean the die with alcohol, and finally, 22) place the die in a waffle or gel-pack.

General Electric: GE High Density Interconnect (HDI) is an MCM technology involving a ceramic substrate with holes for chips. The chip interconnect is laid over the chips. Since they need KGD to use HDI, they are adapting the HDI process to create a KGD methodology. For this methodology, they place dice on a flat substrate or one with holes for the chips. They then spray polyimide over the chips. Like Elmo's process, this coating protects the chips from handling-induced damage. They then drill holes to the bond pads and add a new metallization layer that provides new temporary bond pads on top of the coating, again like Elmo's process. Finally, they cut the substrate to separate each die, wirebond the die to temporary packages, do test and burn-in, remove the wirebonds, excise the dice from the temporary packages, and remove the temporary bond pads. The KGD are then ready for their final application.

Harris: Harris buys MCM substrates and assembles them with KGD (which are traceable to the wafer level). Harris' has three KGD methodologies: 1) TAB, 2) Soft-TAB (licensed from Chip Supply, see "Chip Supply" above for a description), and 3) Prototype KGD. Their main KGD methodology is TAB. For their TAB process, they perform tests at -65, 25, and 125 °C, and burn-in for 168 hours at 125 °C. They have essentially qualified their TAB process to be MIL-STD-883 class B-equivalent as defined by JEDEC (quality specification development was led by Celeste Null). For low-volume dice with less than 100 pads, they can use their prototype KGD sacrificial packaging technique (see "Semi-permanent Carriers", section 9). Prototypes leave aluminum bond pads with a small stub from the temporary bond that does not interfere with subsequent wirebonding. Besides these methods, Harris is looking into other KGD techniques such as disposable low cost fixtures.

Harris, MCC's largest shareholder, has a working relationship with MCC. Through this relationship, MCC has developed rework methods where Harris can rework TAB-interconnnected die on MCM-C and MCM-D 3 to 4 times without damage. In addition, Harris and MCC are developing KGD carrier methods.

Honeywell: Honeywell uses sacrificial package testing to qualify KGD. For this method, they use "soft bonds" to temporarily assemble a die in a package, perform AC and DC structural and functional tests along with burn-in, remove the die from the sacrificial package, and if it passes, mount it in its final multi-chip assembly. "Soft bonds" have less than 2 grams pull strength as opposed to normal bonds, which have over 10 grams pull strength. For the sacrificial package, they typically use a 36-pin flatpack. Thus they can only test dice with low I/O, such as RAMs.

Honeywell fabricates these RAMs with tabs (small L-shaped pad on bonding pad) for temporary wirebonding purposes. They then test the RAMs at 25 °C on a Teradyne J397 tester, perform burn-in dynamically for 72 hours at 125 °C, and retest them. Honeywell can provide 8k x 8 and 32k x 8 RAMs as KGD. They also have an arrangement with Micron to purchase SRAM KGD, and then package them as class S devices.

Soft-Bond Scar Study. To study soft bond scar effects on die quality, we (JPL) conducted a study in October, 1993 on a Honeywell die that had undergone both wafer probe testing and sacrificial package testing. Scanning electron microscope (SEM) observations have revealed two significant issues: 1) Wafer probe scars are generally deeper than sacrificial package scars. Since wafer probe scars do not generally present a reliability hazard, we conclude that the depth of these particular sacrificial package scars also does not present a reliability hazard. 2) The length of sacrificial package scars makes fitting them on the tabs difficult. Tabs are areas on the die pad edges with decreased width designed for testing. Thus, many scars disturbed the glassivation layer around the bonding pad perimeters. This presents a reliability hazard, as gaps in the glassivation layer may allow contamination to cause shorts between metal lines underneath the layer. Also, disturbed glassivation often makes inspection beneath the disturbed area impossible.

Note on issue 2): Bonding onto the wider area of the die pads, rather than on the tabs presents one solution to the sacrificial bond scar problem. This would allow the scars to fit on the pads and thus keep them from disturbing the surrounding glassivation. Perhaps the tab concept, which keeps the final wirebonds from being applied on top of test scars, is not necessary for this particular application. Testers have frequently applied wirebonds on top of wafer probe scars, and as discussed earlier, wafer probe scars are even deeper than these sacrificial package soft-bond scars. Thus, if bonding on top of wafer probe scars generally presents no problems, wirebonding on top of these particular sacrificial package soft-bond scars should also not present problems.

Honeywell is also looking into performing HP's Below-a-Minute Burn-in (BAMBI) at the die level. BAMBI uses stress gradients to activate latent defects, and accepts or rejects the die based on lot statistics.

Hughes: Hughes is developing a TAB-like soft-tooled KGD approach called Testable Ribbon Bonding (TRB). Unlike TAB, it requires no IC post-processing (i.e. bumping). It consists of four steps. First, they interconnect the chip to a disposable test carrier using ribbon bonding (1 x 3 mil gold wires). A standard automatic bonder with a custom chip alignment stage connects the ribbon bonds to 100 micron pads. Second, they perform pretesting and burn-in. Standard TAB test sockets (modified to allow carrier registration) contact the outer carrier pads. Third, they excise the chip from the carrier by laser-cutting the ribbons. This eliminates misalignment problems associated with hard tools. Fourth, they assemble the die into the final MCM by vacuum picking the die from a Gel-Pack (see "Vitchem", below) and bonding the outer ribbon leads to the MCM substrate using an automatic thermosonic wire bonder with a wedge tool.

This soft-tooled approach offers many advantages over TAB. First, TRB has relatively low NRE costs and allows rapid change between chip types. Second, it is faster and cheaper by eliminating device-specific tooling required by TAB. Finally, it allows for tighter chip spacing than TAB (TAB requires 5 mm chip spacing, while face-up TRB requires 1.78 mm spacing, and face-down TRB requires only 1.14 mm).

Hughes is also working on a wafer-level burn-in solution using extended die-level membrane probe cards.

IBM: IBM has two main MCM products: the VHSIC Chip on Silicon (VCOS) and the Thermal Conduction Module (TCM). They have facilities for chip and MCM substrate fabrication, KGD testing, MCM assembly and MCM test.

For VCOS (NTK cofired alumina, epoxy attach, flex substrate, solder sealed), they consider logic-populated modules to yield high enough to forgo bare die testing. Memory VCOS, on the other hand, goes through wafer-level temperature cycling and C4 sacrificial package burn-in.

For TCM (aluminum and polyimide on a silicon substrate) they use the R3 process for KGD test and burn-in. R3 tests C4-interconnected dice only. IBM has sold over 1,000,000 R3 C4 KGD. R3 accommodates between 100-2700 C4 bonds. The R3 methodology involves C4-connecting the die to a pin grid array package (and placing a lid over the die) for test and burn-in. After KGD testing, they twist the die out, breaking the C4 connections at the point where they make contact with the R3 set-up. They break at this point rather then the point where the C4 ball makes contact with the chip because the connection to the R3 set-up involves a reduced radius compared with the connection to the die. Thus, the connection to the R3 set-up represents the weakest link, and the connection breaks there.

IBM also has a special probing technique for C4-interconnected dice called the Cobra Probe. This probe uses what they call a buckling beam contact, where the vertical wire curves when pressed against the pad. Like all other cantilevered probes, the Cobra Probe's wires are unshielded, and therefore have limited bandwidth.

IDT: IDT began offering KGD in 1992 and they are now formalizing their approach. For KGD testing, they use a temporary package (hermetic DIP or PGA), a thermoplastic die attach, a sealed lid, and permanent gold bumps. KGD then go through the same testing as packaged parts. They can sell all their products (both military and commercial) as KGD. They have plants in Santa Clara, San Jose, Salinas and Panang, Malasia. They may begin using their more cost-effective Panang facility for KGD production.

Intel: Intel offers two ways to purchase KGD (which they call smart die): 1) using smart sort and 2) using a temporary carrier. They offer KGD at the same quality level as their packaged dice (aimed at below 100 DPM). Smart sort involves wafer probing at 25 and 80 °C. They use guardbanding to assure the parts will work at 0 °C. Smart sort offers full AC, DC, and at-speed functional tests up to 50 MHz, but no burn-in. When the application calls for burn-in, they subcontract work for the second option, the temporary carrier. The temporary carrier option uses a scrubbing contact.

Irvine Sensors: Irvine Sensors sells chip stacks, and thus concern themselves with "known good stacks" as well as KGD. These stacks can be flip-chip interconnected, but

they prefer using wirebonds. They sell a Mbit DRAM stack 100 mils thick, involving five dice with a non-shrink co-fired ceramic top. They are also looking into flash EPROMs and 4 Mbit SRAMs.

To obtain "known good stacks", they perform wafer-level electrical test at 25 °C to assure good electrical characteristics such as access time (most of their products are memories). They sort according to which pass 60, 70, and 80 nanosecond access times.

For chip stack burn-in, they use a probe card attached to pads on top of the chip stack. To facilitate burn-in, the chip stack pads have a flexible pitch. These rugged pads on the ceramic top allow them to perform burn-in without packaging (the pads were gold, but they are now transitioning to using aluminum).

JPL: JPL designed a carrier in early 70's but it had many problems. This carrier used membrane technology consisting of metallized kapton. The process involved etching a pattern to match the die pattern.

Lattice: Lattice sells EEPLDs (electrically-erasable programmable logic devices) only, and sells only their in-system programmable devices (ISPLSI) in bare die form. For bare die testing, Lattice only performs wafer-level functional tests, whereby they program and erase the device several times.

Lattice KGD Questionnaire. Lattice sends a questionnaire to their bare die customers. This questionnaire provides a good example of the information a die supplier needs to know to satisfy customer requirements. A list of such requested information from Lattice's questionnaire follows:

• *Target device type:* The questionnaire asks for the following information: 1) targeted device type, 2) package and packaging techniques (MCM, custom package, etc), 3) finished product part mark, 4) will the finished product be built according to MIL-STD-883? 5) operating temperature range, and 6) Vcc range.

• *Die attach:* They ask about: 1) the substrate material, 2) is substrate material isolated? (must be for Lattice die), 3) die attach material and temperature, 4) die attach temperature and time, and 3) package seal and encapsulation. If the seal is hermetic, they ask for: 1) the seal material (gold tin eutectic or glass), 2) the seal profile, 3) the seal peak temperature. If the seal is plastic, they ask for: 1) the mold time and temperature, and 2) the cure time and temperature. For any other seal methods, they ask for the seal profile. If the specification calls for performing temperature cycling after packaging, they ask for 1) the minimum and maximum temperatures used, 2) the duration, and 3) the number of cycles.

• *Programming:* Lattice assumes programming will occur after package assembly. They ask for 1) the programming method, 2) the plan for using in-system programmability features during field operation, 3) the method for making electrical connection to the die,

4) the temperature range over which programming will occur, and 5) plans and requirements for post-programming AC, DC and vector testing.

• *Additional Information:* They ask for any specifications and procedures for testing, programming, and encapsulation.

LSI Logic: LSI Logic performs full DC testing and selected at-speed AC testing (such as propagation delay tests on certain paths) on their KGD, but no burn-in. They have a substitute for burn-in that they claim is just as effective: high temperature storage followed by a high voltage stress test with 100% toggle coverage. This way, they catch temperature related failures and voltage related failures just like burn-in does. They also perform a tightened IDD test which resembles IDDQ testing, but uses only a couple vectors. They are looking into using Aehr's or Nitto Denko's KGD carrier.

Martin Marietta: Martin Marietta uses TAB and "snapstrates" for KGD. The snapstrate method works as follows: 1) mount the chip on a substrate which has a metalization layer underneath it for interconnection to an MCM, 2) fanout the die I/O to a tester via the substrate, 3) perform KGD testing, 4) cut the substrate just outside the die periphery so that the substrate acts as a package for the die, and 5) mount the cut substrate (with the chip mounted on it) onto the final MCM. Companies often use this method for RAMs. Others implementing the snapstrate concept include Harris and the German company Diehl.

Micro Module Systems and Texas Instruments (MMS/TI): MMS has teamed up with TI to develop a KGD temporary carrier. This carrier exemplifies many temporary carriers being developed today in that it has three basic elements: 1) a fixture that plugs into a standard test socket, 2) a custom interposer that electrically connects the die to the fixture, and 3) a mechanism to hold the die in place. This carrier enables complete AC, DC and functional testing up to 260 MHz and up to 1,000 die-level burn-ins. TI and MMS have been in the alpha testing phase since about April, 1993, and many major semiconductor manufacturers are currently evaluating this carrier.

The fixture is a bulky mechanical structure designed with standard I/O, connecting the test socket I/O to the interposer's I/O . The interposer uses a bumped membrane technology that applies mechanical pressure to the die to connect the die pads to electrically active bumps. Engineers must fabricate a custom interposer for each different die footprint. Since the interposer is a piece separate from the fixture, they may use the same fixture with several differnt interposers, allowing the fixture to test dice with several different footprints.

The interposer, originally designed for DEC, provides an electrical connection between the die and the fixture. The interposer fabrication process forms an aluminum-based wafer with a thin film multi-layer copper and polyimide structure on top. The process then etches off the aluminum backing, leaving a more compliant copper and polyimide interposer. This way, the interposer can accomodate the die pad non-planarity. Copper traces on the

polyimide terminate into pad-shaped contacts (bumps) that align with die pads. This interposer technology can accommodate different pad metallurgies such as gold, aluminum, and solder. It can also accommodate different pad shapes such as flat or raised. The process builds a fence on the interposer to align the die-to-interposer contact points using die edges as a reference. This fence enables either engineers or automated vision die pick and place equipment to assemble the die into the interposer.

To hold the die in place, the carrier includes a metal lid that pushes the die toward the bumped interposer, holding the die in place and providing thermal management. As TI and MMS figure that wiping action causes damage, they developed a way for the bumps to penetrate the native oxides on the die pads without wiping. That is, the lid provides up to ten grams of pressure for the bumps to to penetrate the oxides on the pads. TI and MMS claim that this pressure contact technology damages the pads less than cantilevered wafer probes do.

Micron: Micron has two KGD methods: 1) Softool (liscensed to Chip Supply, see "Chip Supply" above), and 2) KGD+. KGD+ involves placing the die in a reusable carrier that looks like a DIP. A lid applies pressure to connect the die to terminals inside the fixture with minimal pad disturbance. This method applies to all devices including bumped dice, and lends itself to automation.

Micron uses "intelligent" burn-in to test their devices. This method combines functional, programmable testing with burn-in. Using this method, they can compute infant mortality failure rates as a function of burn-in time.

Motorola: Motorola, Tempi, Arizona has a KGD program (in the Commercial+ Technology branch) designed to enable their MCM program. They perform all KGD testing at the wafer level, where they claim they can perform hot chuck at-speed testing at 125 °C. They also perform visual inspection per MIL-STD-883, method 2010. They do not test at cold temperatures or perform burn-in. If stored properly and not removed from the Gel-pack, they guarantee their KGD for six months. They have looked into using KGD carriers and found them not to be cost-effective.

Motorola sells the following as KGD: 1) SRAM, model MCM6226A (128Kx8), 2) SRAM, model MCM62110 (32Kx9), 3) DSP, model DSP56156 (16 bit), 4) DSP, model DSP96002 (floating point), 5) microprocessor, model MC68020, 6) microproprocessor, model MC68040, and 7) RISC, models MC8800 and 88200.

Hybrid component re-sellers for Motorola include Chip Supply, Elmo Semiconductor, Minco, and Semi Dice.

nCHIP: nCHIP is developing a wafer-level burn-in technology that uses a silicon substrate with multilevel interconnect and compliant bump technology. This technology uses integral decoupling capacitance between power planes and integral resistors for chip isolation.

Tessera: Tessera has a permanent carrier KGD strategy which translates the peripheral die pad pattern to an area array. This presents a solder ball grid array that they solder surface mount to a module assembly.

Texas Instruments: TI has shown that KGD processing costs for their 4-Mbit DRAM costs about four times as much as the equivalent packaged part. For a description of the temporary carrier technology they co-developed with Micro Module Systems, see "Micro Module Systems (MMS) and TI" above.

Triquint: Triquint sells bare die ASICs after DC sorting them and visually screening them. They then can perform tests at commercial or military temperature.

TRW: TRW won the contract to fabricate the RF MCM for Pluto. It will be interesting to see what KGD techniques they believe in. Speaking with Paula Hurt, she informed me that they like the MMS/TI temporary carrier KGD strategy best.

Vichem Corporation's Gel-Pak: Gel-Pak replaces the traditional wafflepack for packing and transporting bare die. This technology utilizes a gel (sponge-like surface) that holds the die on the surface. Gel-Pak surfaces can come in any size; the standard sizes are 2"x2" and 4"x4". To remove dice from the gel-pak, engineers apply a vacuum beneath gel surface to "wrinkle" the surface as it is pulled into voids beneath the surface. This reduces the surface area of the gel that contacts the die, facilitating die removal. Many bare die suppliers including Motorola, Intel, and Micron ship bare die using Gel-Pak. Gel-Pak can accomodate any size die, wafer, substrate, MCM, etc.

Gel-Pak offers convenient storage and retrieval. There are no pockets in which fit dice, so many device sizes fit in a single tray size. This eliminates dice sticking in pockets, as when using waffle packs. Also, tweezers and inspectors can fully access die edges. Finally, automated die-attach equipment can easily remove dice from Gel-Paks, as engineers can precisely define the die position and orientation on the Gel-Pak.

Gel-Pak also offers die protection. Since the surface and edges do not make contact with the tray, the edges do not chip. Also, dice do not spill, even if handling tilts or jars the Gel-Pak. The gel tends to capture dust and other particulates retained by device if these particulates make contact with the gel. Finally, the absence of pockets implies no dust generation from die movement in pockets.

Westinghouse: Westinghouse has developed a KGD temporary carrier much less expensively than MMS/TI's carrier. They produce most of their KGD to support in-house projects. They have a partnership with TI to develop MCMs for the F22 program. They do government work, but no commercial work. Their biggest product is radar.

Xilinx: Xilinx offers FPGA KGD by using Chip Supply as a third party KGD test house for small volumes. For large volumes, they are considering using Elmo.