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The BUG
BITBUS Universal Gateway

Greg Nawrocki

1. Introduction

The BITBUS Universal Gateway (BUG) provides a unique, cost effective solution to many different computer interface problems. Each BUG node, utilizing ”on board” intelligence, has the ability to provide a communication link between BITBUS protocol and other computer–signal interfaces. Among them, IEEE–488, RS232, and raw analog and binary signal I/O. BITBUS is a multidrop, multinode link with the ability to communicate over great distances. By using this method of signal transfer, along with the communication conversion ability of the BUG, one could accomplish such things as the ability to run IEEE–488 instruments over great distances, extend a multidrop links to RS232 instruments, and provide a convenient interface point for remote analog and binary I/O signals, all on one homogeneous network. The BUG not only provides this through the wired ”twisted pair” standard of BITBUS, but extends the ability to fiber optic communications for signal transfer over extreme distances and through electrically ”noisy” environments.

2. Problems With Current Interfaces

Currently IEEE–488 and RS232 interfaces are being used in instruments within the APS control system. These interfaces have severe limitations when used in an industrial, non–office type environment for computer control systems. IEEE–488 offers no error detection mechanisms, no ground isolation, and severe distance limitations. Although both fiber optic and Twisted pair extenders are available for IEEE–488 they are prohibitively expensive. RS232 offers no ground isolation, severe distance limitations, and exists with a single node master/slave topology. Again although extenders are available for RS232 they still maintain the single node topology. Multidrop RS232 network solutions are available, however, their use is again, prohibitively expensive. Basic binary and analog I/O have obvious distance and noise immunity problems when interfaced to a control system. Currently the Allen–Bradley 1771 series I/O modules provide remote interfacing for these types of signals in the APS control system. Although effective, it is best used fo a multitude of signals as its use becomes cost prohibitive when used with just a few raw binary or analog signal points. Another problem with the Allen–Bradley solution is that the network and I/O chassis are proprietary designs of Allen–Bradley. Modules cannot be customized to meet the unique requirements of the APS control system.

3. A Bit on BITBUS™

BITBUS was selected as the subnet for this type of interface to the APS control system. Although now more popular in Europe than the United States, BITBUS is gaining popularity and is likely to be accepted as an IEEE standard (IEEE P1118). BITBUS was introduced by Intel to provide high speed transfer of short control messages in hierarchial systems. Features of this specification include:

– Mechanical Interface
  9 pin D subminiature connector or 10 pin header type connector
– Electrical Interface: RS485 (differential twisted pair)
  – Self–clocked Mode (NRZI encoding): 62.5Kb/s @ 1200m or 375Kb/s @ 300m
    28 nodes per segment, 250 nodes total on multiple segments connected with repeaters
    Single segment subnets require one twisted pair for data
    Multiple segment subnets require two twisted pair, one for data, one for transceiver control

– Synchronous Mode: 500Kb/s to 2.4Mb/s up to 30m
  28 nodes maximum, requires two twisted pair, one for data, one for clock
– Data Link Protocol: subset of SDLC
  Single master/multiple slave topology
  Provides CRC error detection and message sequencing
  Provides automatic retry on detection of errors
– Message Protocol
  Destination address includes Node and Task
  Predefined messages for I/O and memory commands
  Data length up to 248 bytes per message

For more information refer to The BITBUS™ Interconnect Serial Control Bus Specification, copyright 1988, Intel Corporation, Order number 280645–001.

4. The BITBUS™ Universal Gateway

4.1 Hardware Description

The BITBUS Universal Gateway (BUG) system is physically a three board sandwich configuration consisting of the BITBUS interface board, the CPU board, and the personality board. The BITBUS Board, as the name suggests, provides the BITBUS network interface for the Intel 8044 BITBUS Enhanced Microcontroller. The CPU board contains the Microcontroller, memory, and configuration circuitry. While the personality board is the control interface to the supported hardware; IEEE–488, RS232, basic analog and binary I/O to name a few.

The BITBUS Interface Board

The BITBUS interface board comes in two ”flavors”, a wired, opto–isolated interface and a fiber optic interface. The wired subnet is that of the BITBUS specification, the fiber optic subnet was developed specially for the BUG and will be detailed later. Both contain the necessary circuitry to supply the CPU board with the proper lines for the DATA and I/O pins. In addition the BITBUS interface board contains the red and green status LEDs supported by the CPU board. There is also a series of 8 diagnostic LEDs and a latch on the BITBUS interface board. The latch is connected via connector to the data lines of the CPU board. This latch, triggered by an address sequence, will allow for a byte of data to be written to the 8 LEDs for ease of software diagnostics. The power is also brought in through the BITBUS interface board. When placed in an enclosure the BITBUS interface (either fiber optic or 9 pin D) connectors are at the front of the case. Directly to the right are the two 8044 status LEDs followed by the byte of diagnostic LEDs. The most significant bit is on the top right, with the least significant bit on the bottom left.

The BITBUS Opto–isolated Interface

The electrical, opto–isolated BITBUS interface uses a 9 pin D connector (BITBUS standard) for the electrical interface. RS485 dictates that a transmitter shall be capable of driving a 60 ohm termination (120 ohm at each end) and up to 28 standard loads. Therefore, there will be two such connectors on this board for ease of feedthrough in a multidrop system or for the connection of a line terminator for a BUG placed at the

termination point of such a system. In the Advanced Photon Source BITBUS wired subnet, Belden 9463 78 ohm twinaxial cable will be used, therefore, the termination at each end will be 150 ohms. On the board itself, the differential RS485 line is connected to a SN75176 differential bus transceiver. This takes, as input, single ended data and outputs RS485 differential data, or takes, as input, RS485 differential data and outputs single ended data. The transmitter and receiver sections of the chip are enabled in opposition to one another so data sent out is not immediately read in. This enabling is governed by the logic state on the I/O pin of the CPU. The BITBUS interface board also contains a transceiver for the differential RTS lines, so the BUG can be used as a slave node when repeaters are used.Both the DATA and I/O lines are separated from the transceivers and the CPU by opto–isolators. Implemented are the Hewlett Packard HCPL–2630 series opto–isolators. These parts have a minimum common mode transient immunity of 100V/μs for the HCPL–2630 and 1000V/μs for the HCPL–2631. A DC–DC converter, Power General DC1–1–5/5 is used to separately supply power to the isolated side of the BITBUS interface board, it provides 500VDC input/output isolation. More courageous efforts at isolation can be made, however, the method listed here should be sufficient.

The BITBUS Fiber Optic Interface

The BITBUS fiber optic interface was developed specifically for the BUG, so BITBUS transmission could be accomplished in environments with severe electrical noise. Although this is not defined in the BITBUS standard the data link and message protocol are the same as the standard RS485 interface. The fiber optic BITBUS interface must be operated in the self clocked mode at either speed. Since repeaters are not used, the fiber optic subnet may be operated with up to 250 nodes.

The BITBUS fiber optic interface board utilizes the Hewlett Packard HFBR–1412T or HFBR–1414T fiber optic transmitters, and the HFBR–2412T or HFBR–2412TC receivers. The HFBR–1414T is simply a higher optical power version of the HFBR–1412T, and the HFBR–2412TC has a conductive fiber optic connector port as opposed to the non–conductive fiber optic port of the HFBR–2412T. The conductive port option may be helpful in situations where extreme electrical noise in the vicinity may cause a false trigger with the HFBR–2412T. The ”T” in the part nomenclature signifies a threaded port, allowing the transmitters and receivers to have a solid front panel connection to the BUG enclosure. These transmitters and receivers are constructed with ATT ST type connectors. They are bayonet style connectors that provide a simple and accurate fiber connection. Both the electronics and connectors are compatible with 50/125μm, 62.5/125μm, or 100/140μm fiber optic cable. 62.5/125μm is being used in the APS BITBUS fiber optic subnet. With the HFBR–1414T transmitters, and the 62.5/125μm optical fiber guaranteed distances of 1.2km between nodes can be obtained.

Essentially, the fiber optic BITBUS interface card is very similar to that of its opto–isolated brother, however, instead of opto–isolators, fiber optic transmitters and receivers fill that function. Instead of differential data over a twisted pair, the data is transmitted and received over a pair of optical fibers, one for incoming data to the BUG node, and the other for outgoing data from the BUG node. The optical fiber is essentially a shared data line which connects the BUG nodes. When one node transmits data on this line, it is received by the next node, examined by the CPU, and also passed on to the follow-

ing node on the line. If a receiving node wishes to respond, the logic state of the CPU I/O pin will change. This causes a tri–state inverer directly after the BUG's fiber optic receiver to switch to a high impedance output, thereby disconnecting the data receiver from the data line and the DATA pin of the CPU. This allows the BUG node to transmit data unaffected by any data coming in on the fiber. This method of data line sharing allows the BITBUS fiber optic interface card to be built for two different methods of fiber interconnects.

The first is a serial highway configuration, which uses one transmitter and one receiver per BUG node. This method is directly related to the above description. A single, or simplex fiber, is run from the BITBUS master fiber optic transceiver to the first BUG node, then from the first BUG node to the second BUG node, then from the second to the third, and so on. The last BUG node must have its output run back to the BITBUS master fiber optic transceiver in a typical ring fashion.

The second method is a daisy chain configuration. In this configuration BUG nodes are linked together, one after the other with duplex (two fibers per cable) fiber optic cable. This method requires two fiber optic transmitters and receivers per node and is actually a variation on the serial highway method. The first set of transmitters and receivers are linked together with one of the fibers in the duplex cable and the data is passed in an identical manner to that of the serial highway configuration. The second set of fiber optic transmitters and receivers are simply fiber repeaters, which accomplish the loopback process back to the BITBUS fiber optic transceiver. The last node in the daisy chain configuration must have its back end fiber receiver and transmitter linked together with a short piece of simplex (single fiber) fiber optic cable, or a serial highway BUG used in its place.

The CPU Board

The CPU board is the middle board of the BUG three board sandwich. It contains the 8044 BITBUS Enhanced Microcontroller, a watchdog timer, address latch, data memory, code memory, node configuration and node address multiplexers, and an address decoding PLA for chip enables.

The 8044 BITBUS Enhanced Microcontroller

The Intel 8044 is the basic building block of a BITBUS control node. The 8044 provides both the computational and communication ability of the BUG. The 8044's dual processor architecture contains an Intel 8051 microcontroller, dual–port RAM, and a serial interface unit (SIU). The 8051 provides the computational power, and the SIU the majority of the communication functions. The 8044's firmware implements the BITBUS message structure and protocol, and the pre–defined I/O command set. Depending upon the hardware interfaced to the 8044, Basic or Extended firmware environments are utilized. In the case of the BUG, this is extended firmware. Although the 8044 has internal data and code memory, the firmware uses the internal code space and most of the internal data space, therefore the BUG is constructed with both external code and data memory. The Extended firmware provides four major functions, power up diagnostics, BITBUS communications, parallel communications and user software services (RAC commands), The status of the power up diagnostics provided by the firmware are indicated by the red and green LEDs mounted on the BITBUS interface board, interfaced to the 8044 through the Viking connector. If a problem is found, the

self test halts, with the state of the LEDs indicating the trouble area. The indications for the corresponding test sequences are listed below:

Test Sequence	State of LEDs	
	Red	Green
Power On State	**On**	**On**
Prior to Start of Tests	**Off**	**Off**
Test 1 – Instruction Set	**On**	**On**
Test 2 – ROM Checksum	**On**	**Off**
Test 3 – Internal RAM	**Off**	**Off**
Test 4 – External RAM	**Off**	**On**

A discussion of BITBUS communication protocol is not warranted here, however, part of the task of the firmware is to set up the BITBUS node address and interface configuration by reading two external 8 bit jumper or switch locations. These two sets of jumpers are multiplexed in to the 8044's port 0, AD[0..7] address lines and enabled by an address decoding PLA. Since the BUG does not use all of the node configuration jumper points a single 10 bit DIP switch (labeled 1 – 10) for the node address and node mode configuration is used. On the 10 bit DIP switch, switch 8 corresponds to bit 0 and switch 1 bit 7 of the BUG node address. All switches open selects node address 00H, all switches closed selects address FFH. Switch 10 corresponds to bit 0 of the mode configuration register and switch 9 bit 1. Bits 0 and 1 establish the BITBUS mode and communication speed during power up in the firmware. The bit rates and modes are as follows: 00 – synchronous, 01 – self clocked 375 Kb/sec, 10 – reserved, 11 – self clocked 62.5 Kb/sec. These are active (1) upon switch closure. The BITBUS subnet in the APS control system will use the self clocked 375 Kb/sec mode exclusively. The firmware also provides parallel communications for an interface to other processors or busses. The BUG uses this interface for communication to the personality board, for interface to the controlled / monitored signals. This will be detailed in a later section.

For more information refer to the Distributed Control Modules Databook, copyright Intel Corporation, Order number 230973–004, and the 8–Bit Embedded Controllers manual, copyright Intel Corporation, Order number 270645–003. Refer to the sections on the 8044, and 8051 microcontrollers.

Watchdog Timer

The controller board contains a watchdog timer which can trigger upon the absence of any of the following; ALE, jumper pins 3 and 1 on the configuration jumper JMP1. DATA, jumper pins 3 and 4. P1.2, a pre–defined signal on pin 3 (port 0, signal 2) of the 8044, jumper pins 3 and 5. To activate the watchdog timer, pins 7 and 9 on the configuration jumper JMP1 must be jumpered together. The absence of the configured signal

will cause the watchdog to send a reset pulse to the 8044 and peripheral boards. The watchdog timer also issues a reset pulse upon power up.

External Data Memory

The external data memory of the BUG uses a 32K x 8 RAM chip. The external RAM takes up the lower half of the external data space, with the I/O addressing taking up the upper half. See the memory map on the following page.

External Code Memory

The external code memory of the BUG uses either a 32K x 8 RAM chip, or the identical size PROM chip. The type of memory is selected by the configuration jumper JMP2. Pins 1 – 2 and 3 – 4 are jumpered together for ROM, and pins 2 – 3 and 4 – 5 are jumpered together for RAM. ROM be used for normal operation of a personality board, RAM is generally for BUG code development work. The external data RAM is enabled when address bit 15 is low, and the external code RAM/ROM is enabled when address bit 15 is high. Note that in the memory map on the following page, there is a gap in the external code memory address space from FF00H – FFDFH. This is to protect an external code RAM from having parts of its address space written over when data is sent out to any of the I/O or control sections of the external data memory between FF00H and FFDFH.

The Personality Board

The personality board is the BUG's interface to the controlled environment. It can be an IEEE–488 interface, RS232 interface, or basic analog and binary I/O points. The personality board interface was chosen to be the SBX (single board extension) bus. The SBX bus is an Intel and IEEE standard (IEEE 959–88) therefore, there are many such I/O boards commercially available. This provides the convenience of using inexpensive commercially available I/O boards to customize the Bug's I/O interface.

There are two types of board supported by the SBX bus. The standard SBX MULTIMODULE boards, and the SBX MULTIMODULE boards with DMA support. These boards contain DMA controllers which give the capability to perform direct I/O to memory or memory to I/O operations. In addition, the SBX standard allows for 8 or 16 bit data words and two board sizes, the single and double wide boards. The BUG supports only the 8 bit data word, non–DMA, single wide boards. The SBX board is the interface to the external controlled / monitored hardware. Therefore, the interface signals are connected through a short length of cable from the SBX board to a connector on the rear of the BUG.

The signals on the SBX bus can be grouped into six different classes. Control lines, address and chip select lines, data lines, interrupt lines, option lines, and power lines. The three control lines are the (pin 5) reset line, (pin 13) write line, and (pin 15) read line. The reset line operates off the watchdog timer or an address sequence written to external data space, this provides a method for manual peripheral reset. The read and write lines are for specifying the type of data transfer between the SBX card and the 8044.The three address lines AD[0..2] pins 11, 9, and 7 respectively, and the two chip select lines, CS0 (pin 22) and CS1 (pin 20) are used to establish the I/O port being accessed. The data lines AD[0..7] are brought through pins 33, 31, 29, 27, 25, 23, 21, and

19 respectively. Two interrupt lines INT0 (pin 14) and INT1 (pin 12) are provided to make interrupt requests from the SBX board to the 8044 board on the BUG. All of the above signals are TTL level. The specialized user option lines, OPT0 (pin 30) and OPT1 (pin 28) are not used on the BUG. Power (+5V) is available on pins 4, 18, and 36, with the ground pins being 3, 17, and 35. The data transfer I/O read and I/O write operations to and from the SBX board are straight forward. The BUG 8044 board will generate a valid address and chip select, then activate the read line causing the SBX board to generate valid data from the addressed I/O port. The 8044 board will read the 8 bit data and then remove the read command, address and chip select. The write command is similar, the 8044 will generate 8 bit data and hold the write line active for a specified time. As evident from the pin outs of the SBX connector, the BUG can handle two levels of interrupts from a given SBX board.

There are a multitude of third party vendors that carry SBX MULTIMODULE boards. Including the afforementioned IEEE–488, RS232/RS422, Binary I/O, and Analog I/O boards. Essentially a good variety of I/O support. A Multimodule Expansion Boards Reference List is available from Micronetics International, Inc.

An advantage to the SBX system is that it allows for easy custom modules to be built. Prototyping modules are available, for example the ZBX–391 from Zendex Corporation, Dublin, CA. However, the connectors are also commercially available and can be paired with prototyping boards of the designers preference, as long as board size, connector, and mounting hole location SBX standards are met.Custom SBX boards have an additional advantage. Boards similar to that of commercially available products can be made, with support for only the types of devices and protocol the user requires. For example, an IEEE–488 SBX card without DMA support was developed for use in the APS BITBUS subnet. Often these boards can be made at the fraction of the cost of commercially available products, as was the case with the APS designed IEEE–488 SBX module.Another plus to the BUG system is that it is small enough to potentially be built into various instruments for BITBUS control. For example there are numerous vacuum monitoring systems with option cards based on a bus, utilizing plug in modules for external control. A BUG unit could conceivably be built into such a plug in module creating, in effect, a BITBUS interfaced vacuum monitor.

4.2 **Physical Size**

The size constraint of the unit was dictated by the SBX (Single Board Extension) board, as the iSBX interface is already an Intel and Institute of Electrical and Electronics Engineers (IEEE 959–88) standard. The physical specifications dictate the size of the SBX board to be 3.70 width x 2.50 length, and also dictate the placement of the 36 pin (18x2) connector (width in this case is the distance along the axis of the 2 rows of connector pins with the length being the distance perpendicular to that axis). The SBX standard also dictates the placement of the single mounting hole for the SBX modules. The SBX board has a male 36 pin (18x2) header type connector, actually called an SBX connector (Viking VSP01VT18A01) this protrudes from the bottom (no parts) side of the SBX board and mates with a female SBX connector (Viking VSR01VT18A01) mounted on the top (parts side) of the 8044 board. These two connectors are mounted at the far end of a length of their respective boards. The other side of the length of the 8044 board has a male SBX connector

mounted protruding from the bottom (no parts) side. This connector mates with a female SBX connector mounted on the top (parts) side and at one end of a length of the BITBUS interface board. Note that the connection between the 8044 board and the BITBUS interface board is not actually an SBX connection, however an SBX connector is used as it contains a sufficient number of pins for this interface, provides for a solid mechanical connection between the two boards, and allows for ease of procurement and stocking of parts. Since this is not an SBX interface these connectors will be referred to as VIKING connectors. These three boards form the BUG three board sandwich with the width conforming to the SBX 3.70 inch standard and the length being that of the longest board, in this case the 8044 board at 4.75 inches. The three BUG boards are held together by the SBX and Viking connectors as well as nylon standoffs. The completed three board BUG fits neatly into a PAC–TEC K–CM5–200 enclosure, with the completed unit measuring 2.25H x 5.08W x 5.25L. Power is supplied to the BUG by a 5V wall adapter type power supply.

5. Assembly and Testing

5.1 Assembly

BUG assembly is fairly straight forward. The BUG CPU board should be assembled as indicated by the silk screen part layout, and the part layout diagram included in appendix B of this manual. Note that the male VIKING connector should protrude from the bottom (no parts) side of the board, and the female SBX connector should protrude from the top (parts side) of the board.The address and mode DIP switches should be set according to the directions given in the section on the 8044 BITBUS Enhanced Microcontroller. The EPROM or ROM containing the code for the desired personality board should be inserted in to the socket for Uxx, and the configuration jumper set JMP2 should have pins 1 – 2 and 3 – 4 jumpered together. If the BUG is to be used for code development or a similar situation where a RAM is desired, a 32K x 8 RAM chip should be inserted into the socket for Uxx (a recommended RAM chip is included in the parts list included in appendix C of this manual). If a RAM chip is used jumper set JMP2 should have pins 2 – 3 and 4 – 5 jumpered together. If no code space is desired such as a situation where the BUG will operate entirely on RAC commands or if the simple RAC diagnostics are to be performed on a BUG, no chip need be inserted into the socket for Uxx, and the setting of jumper set JMP2 is irrelevent.

If a BITBUS opto–isolated interface is desired, a BUG BITBUS opto–isolated interface board should be assembled as indicated by the silk screen part layout, and the part layout diagram included in appendix B of this manual. If a BITBUS fiber optic interface is desired a BUG BITBUS fiber optic interface board should be assembled as indicated by the silk screen part layout, and the part layout diagram included in appendix B of this manual, note that the female VIKING connector protrudes from the top (parts side) of this board. If the BUG is to be operated as a daisy chain BUG node, all of the parts that appear on the part layout diagram should be included. If the BUG is to be operated as a serial highway bug node, the following parts should be excluded from the circuit: XMTR2, RCVR2, Rxx, Rxx, and Cxx.The front and rear panels of the PAC–TEC K–CM5–200 enclosure must be punched and labeled in accordance with the type of BUG being constructed. Directions for this are available in appendix D of this manual. Note that the front panel may be completely punched and labeled simply by knowing if the BUG has a BITBUS interface of opto–isolated, fiber–optic daisy chain, or fiber–optic serial highway variety. The rear panel

must be punced and labeled in accordance with the type of personality board being used. Directions for this are included in the specific personality board manual. Note, however, that the power input may be placed and labeled regardles of the type of personality board.Assemby of the BUG unit should begin with the placement of the power input wires on the BITBUS interface board. There are holes with solder pads for this. The power input jack should be soldered to the other end of these two wires, with the length of the two wires being about 4.0". Next two 0.5" nylon 4–40 threaded spacers on the BITBUS interface board. They should be placed on the board so that they are facing up with the components on the board. The BITBUS interface board may now be placed inside the enclosure. Orientation at this point is not important, as the case is symmetrical, however the BITBUS interface board should be attached to the half of the case with the holes for the two long case closure screws. Attach the BITBUS interface board to this half of the enclosure via the 4 mounting holes with 4, .25" 4–40 steel machine screws. The steel screws should be used for this process as opposed to the nylon screws for the spacers as the mounting platforms on the enclosures are self taping. The process of attaching the BITBUS interface board to the enclosure should be done concurrently with the placement of the front panel in the panel slots of the enclusure. If the BITBUS interface board is an opto–isolated type, the two 9 pin D type connectors should protrude through the rectangular slot in the front panel. The mounting hardware for the 9 pin D type connectors should be placed on the connectors at this time. If the BITBUS interface board is a fiber optic type, the fiber optic transmitters and receivers should protrude through the proper holes, and the 0.5" mounting nuts should be placed on the transmitters and receivers so as to provide a solid mechanical interface to the front panel.The BUG CPU board should be assembled with one 0.5" nylon spacer for the SBX board mounted face up (with the components on the board) in the proper mounting hole. The CPU board should then be snaped into the female VIKING connector on the BITBUS interface board, and two nylon 0.25" 4–40 machine screws should be inserted through the CPU board into the two nylon spacers attached to the BITBUS interface board. The personality board SBX module may now be plugged into the CPU board and attached with a 0.25" 4–40 nylon mounting screw. Refer to the instructions included with the various personality boards for more detailed instructions on this, and the mounting of an interface connector on the back panel of the BUG. Remember to also attach the power jack to the back panel of the BUG.

5.2 Testing

Testing of the completed BUG unit, with or without a personality board installed, can be accomplished by simply attaching the BUG to the plug in power supply unit, thereby applying power to the BUG. The RED and GREEN CPU diagnostic LEDs should go through a quick flashing sequence corresponding to the sequence refered to in the section on the 8044 microcontroller. The sequence should terminate with only the GREEN LED being illuminated. To test the communication interface the BUG should be attached to to a BITBUS network, and the controlling computer should issue a RAC command (task 0) number 0x06, this is the RAC write command. The first byte sent will be the address of the 8 diagnostic LEDs offset by 0x8000, which is 0x40 or 0x41, and the second byte is the data that will be displayed by the LEDs, 0x00 turning them all off, and 0xFF turning them all on.