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by

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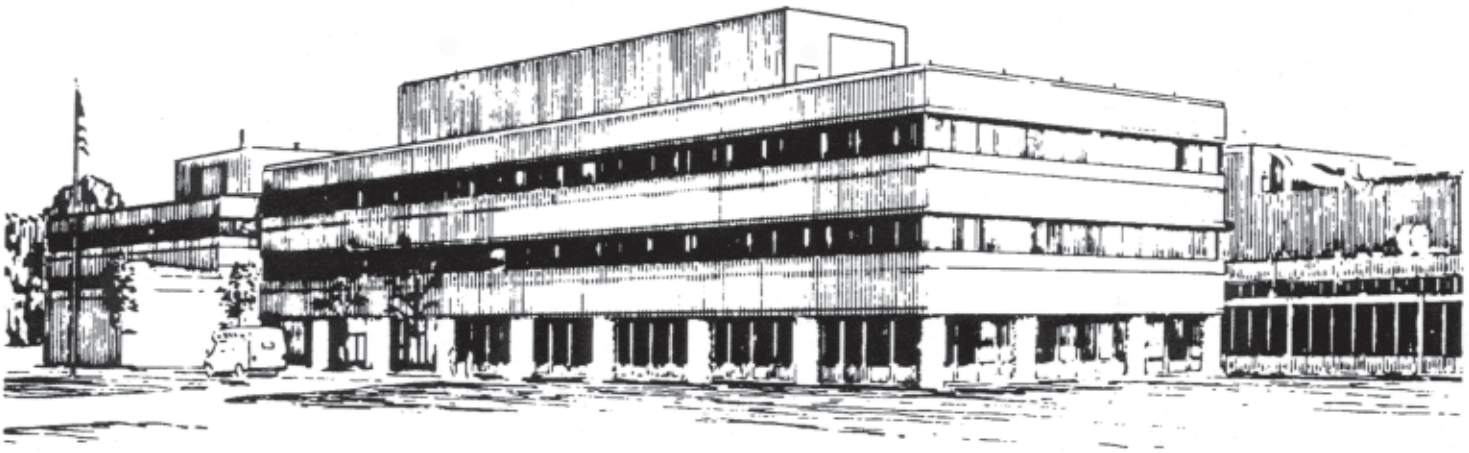

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Developments to Supplant CAMAC with Industry Standard Technology at NSTX *

P. Sichta, J. Dong, R. Marsala, G. Oliaro, J. Wertenbaker
Princeton Plasma Physics Laboratory, P.O. Box 451, Princeton, New Jersey 08543

Abstract - **NSTX, like other research programs, is facing an inevitable crisis due to end-of-life issues for its 20-year-old CAMAC instrumentation. In many cases replacement components are not available, effectively rendering a CAMAC module unusable after a failure. The proliferation of high-performance, reliable, low-cost commodity computing hardware and software based on industry standard technology can provide the basis for a new generation of instrumentation. At NSTX there have been several advances towards developing a PCI-based model for data acquisition and control systems. New hardware developments include a High Performance Signal Conditioning board and an FPGA-based Multifunction Timing System. Extensible software interfaces have been developed to integrate these boards into the NSTX computing environment [1]. This paper will illustrate these developments and how they could be used to benefit collaborative fusion research.**

I. INTRODUCTION

One of the roles of the NSTX Central Instrumentation and Controls (I&C) group is to provide transient digitizing capability for the NSTX experimental program. NSTX's CAMAC digitizers were initially used on the Tokamak Fusion Test Reactor [TFTR] and are almost 20 years old[2]. Replacement parts are often not available. New transient digitizers with higher digitizing rates and greater memory depth are available in popular bus formats such as CAMAC, VME, PCI, CompactPCI, Industry Pack, and PMC. The I&C group at NSTX has decided to pursue a PCI-based solution to transient digitizing. Recent advancements toward an economical PCI-based I&C system will be presented.

The development effort has produced two new components, a High Performance Signal Conditioner board (HPSC), and a Multifunction Timing System (MTS). These products enable the transient digitizer to be effectively used in the NSTX environment, specifically addressing synchronization and the harsh electrical environment.

II. HIGH PERFORMANCE SIGNAL CONDITIONER

High-channel density PCI digitizers (16+ channels/slot) typically have single-ended analog inputs, which can limit performance in NSTX's electrically volatile environment. The HPSC conditions raw signals for the digitizer's single-ended inputs. Fig. 1 shows the HPSC.

Some of the HPSC specifications are:

- 16 differential inputs (SE out).
- 200 volt common mode voltage.
- 2 MHz bandwidth.
- Configurable gain, 0.25 - 4.0.
- Compact size: 3" x 4.5".

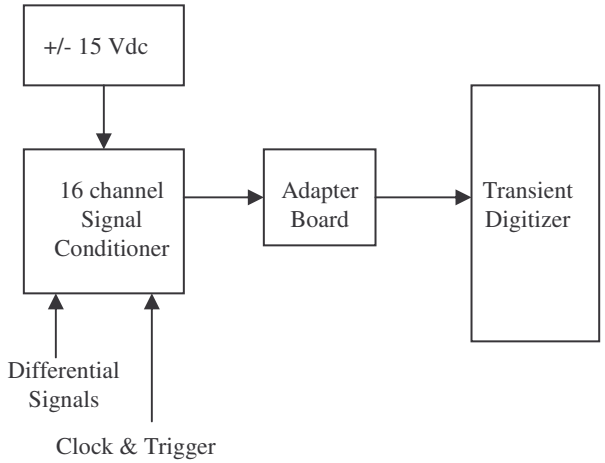

Fig 1: Typical Digitizing System using the HPSC

To make the HPSC compatible with various digitizer types an Adapter Board (AB) concept was adopted. One end of the AB connects with the HPSC outputs, the other side of the AB mates with the transient digitizer. The initial adapter board targeted a variety of DATEL PCI transient digitizers that use DB25 or DB37 connectors. To accommodate transient digitizers with a different connector types, new AB (boards) can be designed and procured quickly using free PCB CADD tools.

The swift development of the HPSC and AB was made possible through extensive use of CADD. The CADD programs included:

- OrCAD (schematic and parts list).
- SPICE (circuit simulator).
- ExpressSCH (schematic entry).
- ExpressPCB (PCB design/order).

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III. MULTIFUNCTION TIMING SYSTEM.

The NSTX Facility Clock, which is built from CAMAC components used on the TFTR Facility Clock [3], is distributed throughout the NSTX experimental complex and is used to provide a (common) 1 MHz time base and to encode 'events', such as Start-of-Discharge. The Multifunction Timing System (MTS) is a set of PCI hardware and software components that accept the clock link and produce synchronized timing signals for data acquisition and control systems. The MTS can also produce timing signals from external trigger inputs and software commands.

The MTS hardware is made up of two boards, a PCI board XC2S_EVAL from CeSys GmbH and an NSTX-designed Interface Board (IB). Fig. 2 depicts the typical hardware arrangement. The software is modular, as depicted in fig. 3.

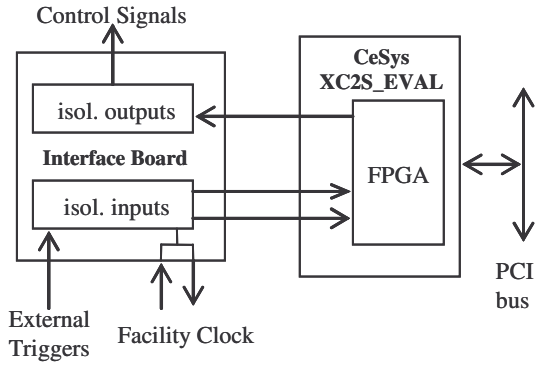

Fig. 2: MTS Hardware Arrangement

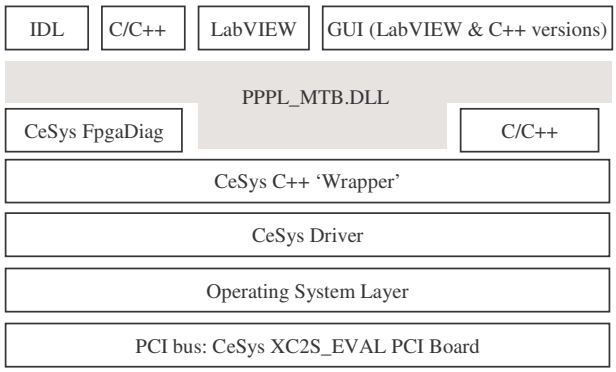

Fig. 3: MTS Software Arrangement

A. Functional Description

A multitude of timing functions are provided by the MTS. The board's six channels are independently programmable, so that one board can provide several different timing functions. The MTS was designed to emulate the timing capabilities provided by several types of NSTX CAMAC modules. Brief descriptions of the functions are provided below.

- *Function 1: Event Decoder and Delay*

This emulates the CAMAC H404 Timing module. In this mode (EDD), a timing channel will respond to an event or trigger, delay a programmable time, and output a timing pulse.

- *Function 2: Timed Gate*

This emulates the CAMAC H409 and H305 Timed Gate modules. In this mode (TG), a timing channel will respond to an event or trigger, delay a programmable time, then output a 'gate' of programmable duration.

- *Function 3: Programmable Pulse Generator*

This emulates the CAMAC H412 Timing and Sequencing module. In this mode (PPG), a timing channel will respond to an event or trigger by producing a programmed sequence of output pulses.

- *Function 4: Serial Time Interval Counter*

This emulates the CAMAC H408 Serial Time Interval Counter module. In this mode (STIC), a timing channel will respond to a 'start' event or trigger, and then record the number and relative time of subsequent pulses received at the 'stop' input.

- *Function 5: Clock Generator*

This emulates the CAMAC H904 Clock Generator module. In this mode (CG), a timing channel will output a continuous, fixed-frequency clock whose phase can be synchronized with an NSTX clock event.

B. Performance Upgrade

The NSTX timing architecture is based on the TFTR system, and has been operational for over twenty years. Over that time a few operational constraints and timing anomalies have been identified. That knowledge has been incorporated into the design of the MTS to provide better performance and enhanced capability while remaining totally compatible with the existing NSTX clock system. The upgrades include:

- Simultaneity reduced to ~5 µS between systems (was ~20 µS).
- Supports 10 MHz link carrier.
- 100 nS delay resolution.
- 256 event codes (was 16).
- Link integrity detection.

C. MTS Hardware

The CeSys XC2S_EVAL PCI board contains a Field Programmable Gate Array (FPGA) and a 37-pin I/O connector. The on-board FPGA is the Xilinx SpartanII XC2S200. The board provides a PCI bus interface using

separate circuitry, so the entire FPGA is available for the user's configuration.

The timing signals used with CAMAC have a long history of good performance. The Interface Board (IB) uses the same I/O circuitry as the CAMAC timing modules. Each timing channel has five I/O signals, whose purpose is dependent upon the programmed function for that channel.

The interface points are:

- Two opto-isolated trigger inputs.
- Pulse transformer output.
- Opto-isolator output.
- Line Driver output[1].

The IB also receives and retransmits the NSTX Facility Clock link via pulse transformers.

D. MTS Software

The MTS development was primarily a software engineering effort. There are three elements of the MTS software, the FPGA configuration file, a Microsoft Windows DLL, and National Instruments LabVIEW support.

- *FPGA CONFIGURATION*

The FPGA configuration (file) represents the program that is loaded into the FPGA device. The FPGA performs all facility clock event decoding, trigger masking, timing, and output control. Xilinx provided an integrated development environment to create the configuration for the FPGA. The Xilinx product used was Foundation Series ISE (3.1).

The MTS software effort began by drawing the CAMAC timing module schematic diagrams (TTL logic) using a Xilinx *schematic editor* tool. Each CAMAC module that is emulated in the MTS was drawn into the multi-page schematic. The schematic diagram was then converted to the FPGA industry's standard language, VHDL. Finally, ISE was used to compile the VHDL source code into an *exo* (format) configuration file. The final step, downloading the *exo* file to the CeSys PCI FPGA board, was done with a CeSys-provided utility called FpgaDiag.

About 65% of the FPGA's resources have been used in implementing the first two MTS functions. There is some concern that the remaining three functions may not fit onto the FPGA. There are several solutions to this potential problem, so the design team is not overly concerned.

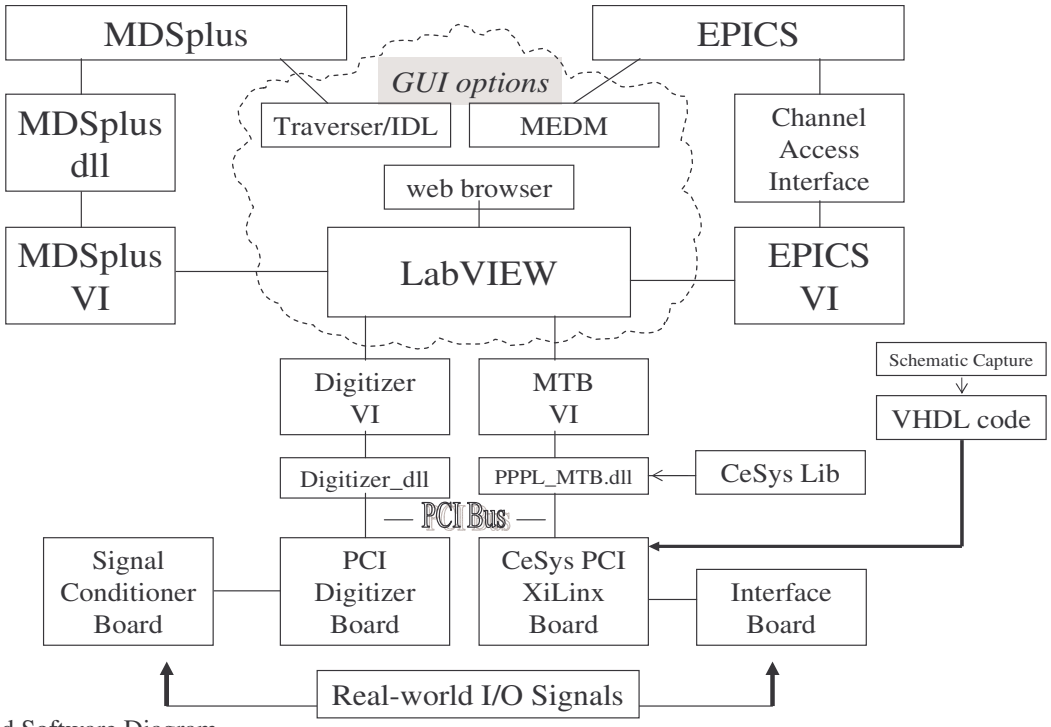

Fig. 4: Integrated Software Diagram

[1] Not an isolated signal.

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The (MTS) DLL is a suite of C++ functions that read/write/control the MTB. The 'top half' of the DLL can be accessed from programs coded in IDL, LabVIEW, Visual Basic, etc... The 'lower half' of the DLL calls the CeSys-supplied C++ functions, which in turn communicate with the FPGA.

A general purpose Graphical User Interface (GUI) was written in C++. The GUI was constructed using Microsoft Foundation Class and the Visual C++ ClassWizard. The initial version of the GUI called CeSys' C++ wrapper. The GUI was later revised to use the MTS DLL.

- *LabVIEW*

LabVIEW is a popular programming language used for I&C systems. LabVIEW's ability to interface with the MTS DLL, EPICS, and MDSPlus was exploited to integrate the MTS into the NSTX computing environment (fig. 4). LabVIEW programs were produced for the MTS, a general-purpose GUI and a LabVIEW library (LLB).

The GUI is a built application (.exe) that duplicates the functionality of the aforementioned C++ GUI, but with a more attractive look-and-feel. The LLB provides 20 subVI's that can be 'dropped' into a user's LabVIEW program. All LabVIEW programs call the MTS DLL.

IV. FUTURE PLANS

The MTS' first application will be the NSTX Lithium Pellet Injector (LPI) project. This project was a catalyst in bringing the MTS to fruition. The MTS can support the LPI, but there are plans for enhancements:

- Linux/Linux_LabVIEW support.
- Implement functions 3-5.
- Optimize packaging and terminations.
- Combine MTS hardware (IB and PCI) on single, unified circuit board; custom design.
- VME and CompactPCI support.

V. CONCLUSION

The High Performance Signal Conditioner and the Multifunction Timing System are two products that can pull I&C systems out from the CAMAC era. The skills acquired through these developments have diversified and extended the capabilities of the NSTX engineering staff. Enhancements will make these products more useful to NSTX and its collaborators in the future. The outlook for designing a low-cost, reliable, and maintainable I&C system based on commodity hardware and software is promising. NSTX is committed to the exploration of emerging industry trends and open software environments and their applications to energy research.

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