Process-Induced Morphological Defects in Epitaxial CVD Silicon Carbide

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Silicon carbide (SiC) semiconductor technology has been advancing rapidly, but there are numerous crystal growth problems that need to be solved before SiC can reach its full potential. Among these problems is a need for an improvement in the surface morphology of epitaxial films that are grown to produce device structures. Various processes before and during epilayer growth lead to the formation of morphological defects observed in SiC epilayers grown on SiC substrates. In studies of both 6H and 4H-SiC epilayers, atomic force microscopy (AFM) and other techniques have been used to characterize SiC epilayer surface morphology. In addition to the well-known micropipe defect, SiC epilayers contain growth pits, triangular features (primarily) in 4H-SiC, and macro step due to step bunching. In work at NASA Lewis, it has been found that factors contributing to the formation of some morphological defects include: defects in the substrate bulk, defects in the substrate surface caused by cutting and polishing the wafer, the tilt angle of the wafer surface relative to the basal plane, and growth conditions. Some of these findings confirm results of other research groups. This paper presents a review of published and unpublished investigations into processes that are relevant to epitaxial film morphology.

1. Introduction

The recent advances of SiC semiconductor technology have been greatly aided by the commercial availability of SiC wafers of reasonable size and quality. Bulk crystals of various SiC polytypes (e.g. 4H, 6H, and 15R) are now being grown by vapor sublimation processes at various institutions. The 4H and 6H polytypes are available commercially as polished wafers. Currently, both of these polytypes are actively being developed, but recent emphasis has shifted to the 4H polytype because of the larger electron mobility (800 versus 370 cm^2/Vs) and lower donor activation energy (45 versus 90 meV) of 4H-SiC compared to 6H-SiC [1, 2]. These commercial wafers typically contain dislocations at a density greater than $10^4 \, cm^{-2}$ and a defect known as micropipes at a density of about 100 cm^{-2} [3, 4]. The micropipes are tubular voids, approximately a micrometer in diameter, that extend along the crystal c-axis (the $\langle 0001 \rangle$ growth direction). The micropipes propagate from the SiC substrate into the subsequently grown epitaxial films [5]. These micropipes can negatively impact devices that are fabricated from the epitaxial films [4].

Chemical vapor deposition (CVD) is currently the method of choice to produce SiC device structures consisting of thin doped epitaxial films. Step-controlled epitaxy has been used to obtain homoepitaxial growth (i.e. film and substrate are the same polytype) on SiC substrates [6]. This epitaxy takes place by the lateral growth of atomic-scale steps that are present on the substrate whose growth surface has been tilted "off-axis" from the (0001) basal plane as shown schematically in Fig. 1. The steps on the
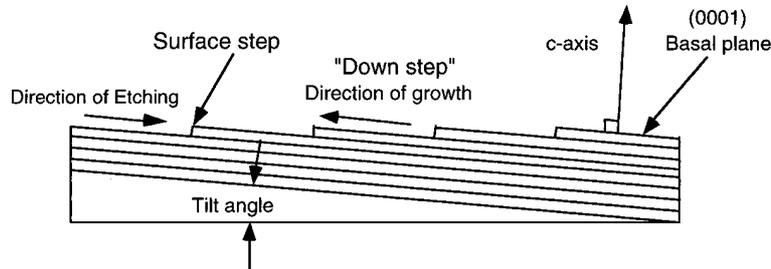
Fig. 1. Cross-sectional schematic diagram illustrating step flow growth on the surface of an "off-axis" SiC substrate

surface contain the polytype stacking sequence of the substrate. In this process, growth occurs at steps rather than at sites of two-dimensional nucleation on atomically-flat terraces between steps or at other unwanted nucleation sites caused by defects or contamination [7]. The polished growth surface of SiC substrates used for device fabrication is typically tilted "off-axis" from the (0001) plane by approximately 3° to 8°. The term "vicinal" (0001) SiC surface is often used for surfaces that are "off-axis" by an angle of up to a few degrees. The precise definition of "vicinal" means "in the neighborhood of", so any angle from zero up to a few degrees is included. The use of the term in the literature is somewhat ambiguous. In this paper, substrates with tilt angles less than 1° will be designated as "on-axis" and substrates with tilt angles greater than 1° will be designated as "off-axis". Also, the "down-step" direction will refer to the direction of the lateral growth of the steps (refer to Fig. 1). The "up-step" direction is the opposite of "down-step".

It has been found that the actual step height of steps on smooth vicinal epitaxially-grown (0001) SiC surface are not equal to 0.25 nm, which is the height of a single double-layer of Si and C atoms that are stacked in the c-direction to form the various polytypes. For example, Tyc [8] observed by atomic force microscopy (AFM) that the average step height on a 3° off-axis, 10 μm thick, 6H epitaxial film grown by Cree was approximately 15 nm high, which is ten times the unit height (i.e. 6×0.25 nm $= 1.5$ nm) of the 6H polytype. Tyc attributed the large steps to a process known as "step bunching" whereby small steps on the surface coalesce into larger steps during the growth process. He also suggested that the large steps could affect the electrical conductivity in different directions parallel to the surface in thin channels of field effect transistors (FETs). Others have shown that step bunching can affect the distribution of dopants that are added during the growth of GaAs and Si device structures [9]. These and other effects of the large surface steps may negatively impact the fabrication of high density SiC integrated circuits.

Commercial fabrication of SiC semiconductor devices is vitally dependent on the achievement of reproducible control over the magnitude and uniformity of epitaxial film thickness and doping. However, the growth rate and dopant incorporation are functions of many growth parameters. The recent NASA-Lewis developed site-competition epitaxy process [10, 11] has enabled reproducible doping of SiC epitaxial films over a much wider range (10^{14} to $>10^{19}$ cm^{-3}) than previously possible (10^{16} to 10^{18} cm^{-3}), and also the ability to produce "ohmic as deposited" electrical contacts. However, growth parameters associated with the use of this process remain to be optimized. For example, this

process involves the variation of the Si/C ratio in the gas phase during growth to achieve different doping levels. Since the site-competition epitaxy process has been found to be most effective on the Si-face of (0001)SiC wafers, we have mostly used Si-face wafers in our epitaxial film growth research and to fabricate SiC semiconductor devices.

An essential requirement of commercial SiC CVD processes is that the resulting films be consistently free of defects and morphological features that would negatively impact either the device fabrication processes or the operation of resulting devices. In the case of current SiC epilayers, a variety of defects and features have been observed in addition to the large steps mentioned previously. In this paper, the term "morphological defect" will be used to denote any structural defects (e.g. dislocation, micropipe, etc.) or any unwanted surface features (e.g. pit, hillock, large steps, etc.). This paper will review morphological defects observed in SiC wafers and epilayers and will discuss processes that contribute to the formation of the defects.

2. Characterization of Wafers and Epilayers

The crystal structure and quality of selected wafers and epilayers were determined by low temperature photoluminescence (LTPL) [12] and transmission electron microscopy (TEM) [13] as described previously. Topographical maps of defects in selected wafers and epilayers were produced by Synchrotron White Beam X-Ray Topography (SWBXT) [14]. The surface morphologies of the epilayers in this study were characterized by Nomarski differential interference contrast (NDIC) optical microscopy and atomic force microscopy (AFM) [15]. The latter technique allowed the observation of features down to near atomic scale. The AFMs used were a Park Scientific Instruments Auto-Probe LS and a Digital Instruments Dimension 3000, each with a lateral scan range of up to 100 μm. The vertical noise level of the AFMs were usually less than 0.1 nm which was sufficient to distinguish between atomic step heights that were single or multiples of the unit bilayer SiC step height (0.25 nm) in the c-axis stacking direction.

3. Commercial Wafer Quality

The SiC substrates used in the NASA work were obtained from 6H-SiC and 4H-SiC wafers up to 35 mm in diameter that were produced by two commercial suppliers from sublimation-grown boules. In this article, the vendors will be identified as source A and source B. The wafers were sliced "on-axis" (less than 1° tilt) or "off-axis" (3° to 8° tilt) from the (0001) basal plane in the $\langle 11\bar{2}0 \rangle$ direction with the Si-face side of the wafers polished to form the growth surface. The SiC wafers were usually cut into either four equal-sized pie-shaped pieces, or into smaller 7.5×6 mm^2 pieces to reduce the substrate cost of epilayer growth experiments.

In some wafers, the as-received polished surface was specular but exhibited faint parallel ridges and random scratches when viewed with NDIC. We believe that the parallel ridges are remnants of the process of slicing wafers from the boule and that the scratch marks are due to the polishing process. The ridges were shallow undulations in the surface and the scratches were narrower in width, but both had depths up to about 5 nm (measured by AFM). Also, by adjusting the contrast while observing with NDIC, very small "white dots" against a darker background could be seen. Some of these white dots were revealed by AFM to be small holes in the surface with diameters in the range 0.5
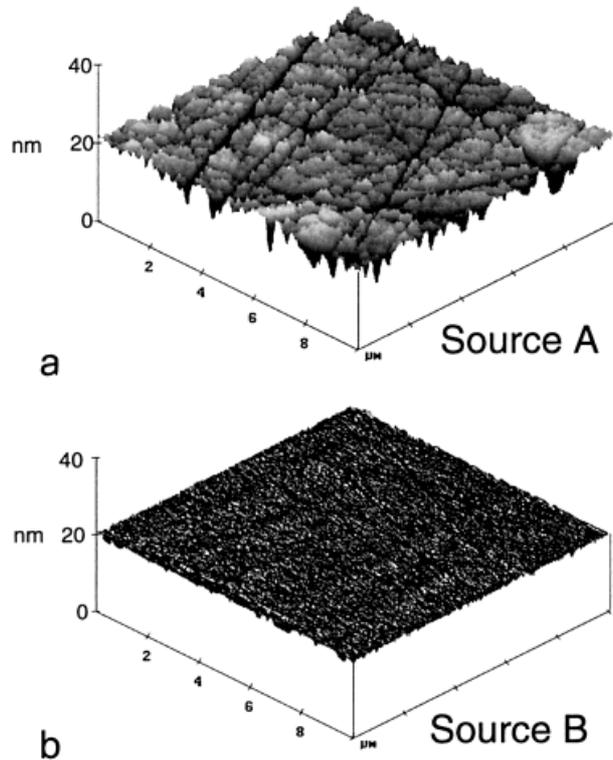
to 1 μm. We did not determine whether these holes as seen by AFM were actually micropipes, but it appeared that the density of the white dots was an order of magnitude higher than the micropipe density of about $100 \, \text{cm}^{-2}$. It is believed that these holes are caused by plasma etching by the vendor which was used to reduce polishing damage. Occasional irregular-shaped voids of various sizes intersected the surface. Compared to 6H-SiC, 4H-SiC as-received generally had more of the larger irregularly shaped voids as revealed by optical microscopy. Fig. 2 illustrates the surface of wafers from two commercial sources. Most of the work reported in this paper were carried out on wafers from source A (Fig. 2a) because more wafers were available from this source. Only a few wafers from source B (Fig. 2b) were obtained; this was not sufficient to allow definitive conclusions regarding the impact of the better surface of source B wafers on growth morphology.

4. Typical Epilayer Growth Processes

The epilayer growth experiments were carried out in a CVD system that has been described previously [12, 15, 16]. The horizontal fused silica CVD chamber was water cooled with an inside diameter of 50 mm. All pregrowth etching and epitaxial growth was carried out at atmospheric pressure. The substrates were heated by an rf-heated SiC-coated graphite susceptor, 80 mm long × 30 mm wide × 10 mm thick. The susceptor was held horizontally in the chamber by a fused silica carrier that blocked the flow in the lower half of the chamber forcing the process gases over the top of the susceptor and
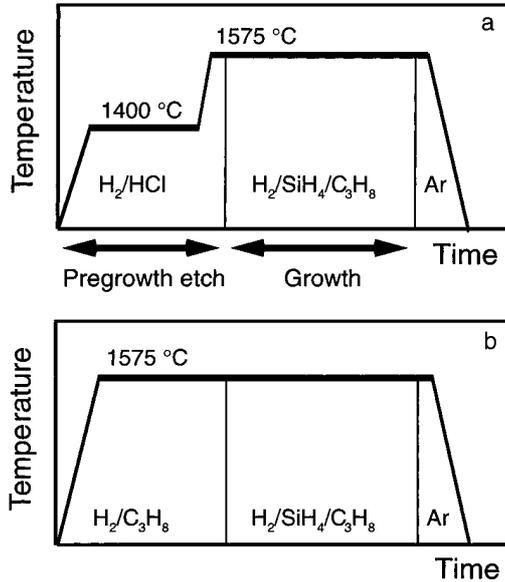
Fig. 3. Two CVD processes used in growth of SiC epilayers on SiC substrates. a) Typical pregrowth etch using H_2/HCl and b) investigated pregrowth etch using H_2/C_3H_8

substrates. Before loading into the CVD chamber, substrates were sequentially cleaned with organic solvents, hot H_2SO_4, scrubbed with liquid detergent, rinsed with $18\,M\Omega\,cm$ water, and then blown dry with nitrogen.

During etching and growth, the H_2 carrier gas flow was maintained at $3\,l/min$. Prior to growth, the substrates were typically subjected to a 4 min HCl etch (3% in H_2) at $(1400 \pm 25)\,°C$ in order to remove unintentional contamination and to reduce the surface damage caused by the wafer cutting and polishing process. A pregrowth etch in H_2 was also investigated and will be discussed in Section 8. Epilayer growth was carried out at a fixed temperature in the range 1450 to 1600 °C with SiH_4 (3% in H_2) and C_3H_8 (3% in H_2) as the sources of Si and C. The temperatures given in this paper are those of the substrate; the susceptor surface temperature was determined to be about 50 °C higher than the substrate. The temperature was measured with an automatic optical pyrometer which was calibrated by observing the melting point of a small amount of previously melted Si on both the susceptor and SiC substrate. The actual temperature was known to within 25 °C, but the reproducibility of the temperature control was better than 2 °C. Typically, the SiH_4 concentration in the growth chamber was held at about 200 ppm and the C_3H_8 was varied to produce Si/C atomic ratios in the gas in the range 0.1 to 0.8. Epilayer growth rates were 3 to 4 $\mu m/$h. Two CVD process schedules that were used in the growth of the epilayers in this study are shown in Fig. 3. If, during CVD, the substrate/susceptor is heated in H_2 above the melting point of silicon (1410 °C), silicon droplets are produced on the SiC substrate. It is believed that the Si droplets contribute to the formation of morphological defects in SiC epilayers. Hence, the CVD process must minimize the time of heating in pure H_2. During the startup portion of the CVD process (Fig. 3a), the presence of HCl inhibits the formation of Si droplets. During cool-down, an inert gas flow, instead of H_2, inhibits the formation of Si droplets. The process shown in Fig. 3b will be discussed in Section 8.

5. Localized Defects (Growth Pits, Triangles)

Epilayers of both 6H and 4H, with thickness in the range 1 to 10 μm, were grown and characterized. Typically, the epilayers appeared specular and free of gross features when examined by eye. When examined by optical microscopy using NDIC illumination, the epilayers exhibited small isolated triangular features and, in the case of 4H, larger trian-
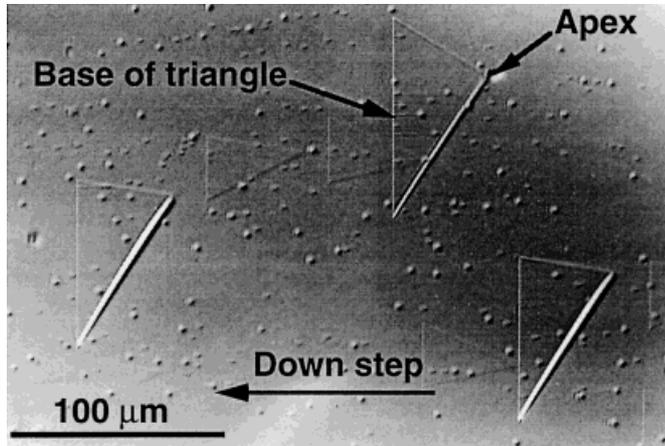
Fig. 4. NDIC optical image of the surface morphology of a 4H-SiC epilayer with isolated morphological defects

gular features as shown in Fig. 4. Both small and large triangular features were always oriented in the same direction, with one corner always pointed in the up-step direction. The distribution of the small features was nonuniform and the density varied widely, often greater than $10^5 \, \text{cm}^{-2}$. Often these features were observed to form along scratches present in the as-received substrate. A typical 4H epilayer, grown under the same conditions as a 6H epilayer would exhibit the same small triangule features, but also the larger triangular features with a size extending to a few tens of micrometers. The distribution of the large triangles, which were only observed in the 4H epilayers, was also very nonuniform. They often were observed to be clustered along scratches in the substrate.
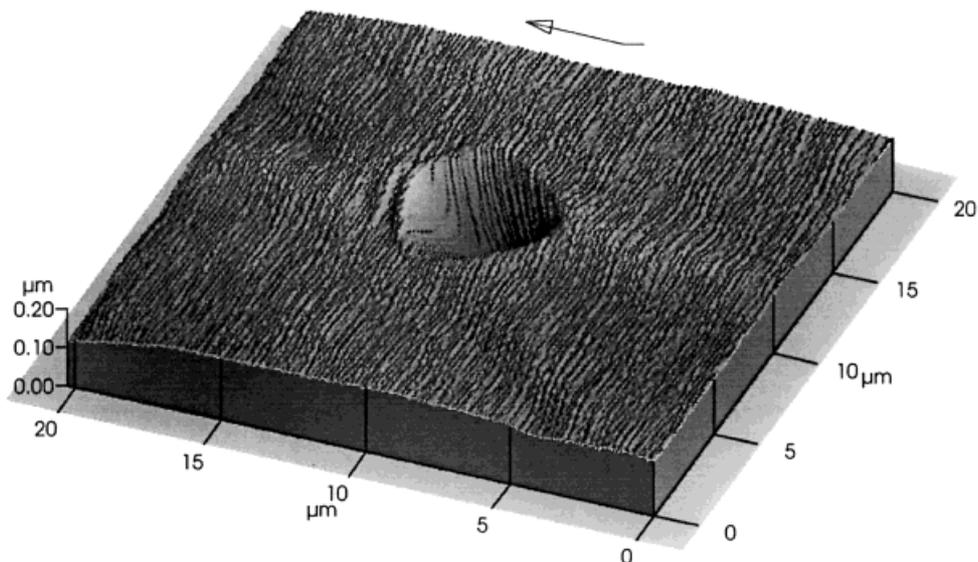

Fig. 5. AFM image of a shallow growth pit produced in a 6H-Si epilayer

Observations of the smaller triangular features with AFM revealed that they were shallow growth pits and that the shape of the pits was somewhat dependent on the specific conditions of the CVD process. An example of the more common of the observed pits is shown in the three-dimensional (3D) AFM image in Fig. 5. The size of the growth pits increased with film thickness. The diameter and depth of the growth pits were approximately 2 μm and 15 nm, respectively, in 1 μm thick epilayers and were larger, about 6 μm and 150 nm, respectively, in 10 μm thick epilayers. The growth pits (sometimes called amphitheaters) are thought to be caused by interruptions in the desired step flow growth.

As seen in Fig. 4, the large triangular features in the 4H epilayers were oriented with an apex at the up-step end and a straight-line base at the down-step end. AFM observations demonstrated that the triangular features were slightly depressed regions. The triangle base was a very straight deep groove and this groove usually extended beyond the corners of the base. The other two sides of the triangle were either straight or curved; these two sites were shallow grooves. In some of the large triangle, the area within the triangle was a depressed facet that was parallel to the (0001) basal plane. The growth on this basal plane area usually was the 3C-SiC polytype.

5.1 Source of growth pits

An investigation [17] was carried out with the purpose of distinguishing which morphological defects were caused by bulk defects in the substrates such as dislocations, micropipes, low-angle grain boundaries, etc. in the original boule crystal and which were caused by surface defects that had been generated by processes involved in cutting, polishing, and preparing the wafer for growth. The following approach was used. First, a typical epilayer (designated as epilayer 1) was grown on some selected commercial 4H and 6H boule-grown substrates (all 3.5° off-axis, Si-face substrates). The epilayer surfaces were characterized with NDIC optical microscopy. Second, epilayer 1 was then polished off to below the original growth surface. The final step of this repolishing used a chemical mechanical polishing (CMP) procedure that will be described in Section 7. A second epilayer (2) was then grown on the same repolished samples. Epilayer 2 was also characterized by NDIC optical microscopy. Specially placed laser-etched markers on the backside of the transparent samples enabled NDIC photographs to be taken of identical locations on epilayers 1 and 2. The purpose of this procedure was to compare the morphology of these two epilayers. We would expect that a) features common to both epilayers would be caused by defects that are present in the original boule crystal, and b) features that were common to only one of the epilayers would be caused by defects at the surface of the wafer (features caused by processes related to preparing the wafer surface for growth).

The results of the repolishing/regrowth experiments are shown in Fig. 6 and 7. NDIC photographs of epilayers 1 and 2 for each of two samples are shown in these figures. Photographs of the same locations on the 4H and 6H boule-derived samples are shown. The "dot-like" features seen in these photographs are the growth pits that we have observed in all of our SiC epilayers. The results can be summarized as follows:

a) In the 4H epilayers (Fig. 6), the growth pit density is much less in epilayer 2 (Fig. 6b). Also, new triangular features appear in epilayer 2, apparently the result of scratches that were produced in the repolishing. There does not appear to be any correlation between any features seen in these two 4H epilayers.
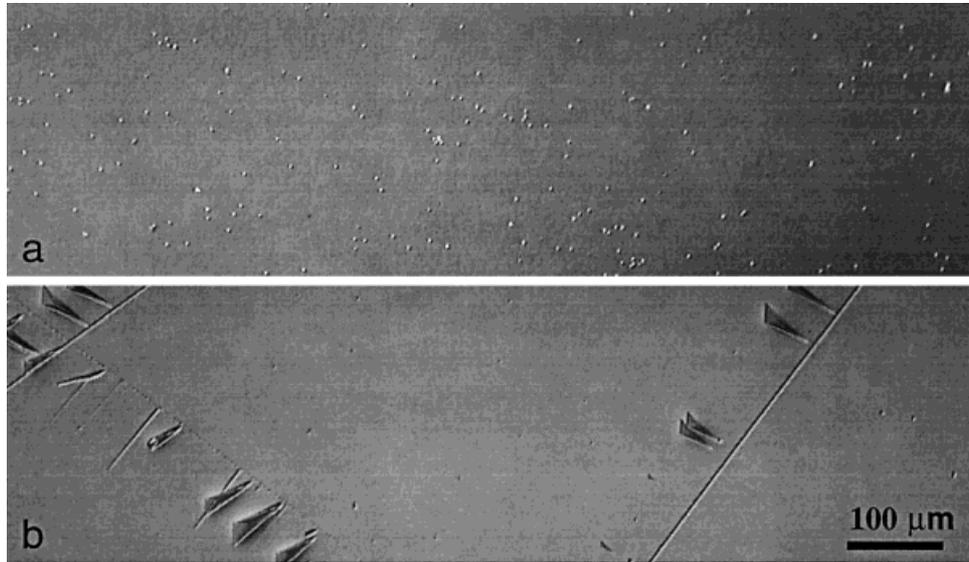
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Fig. 6. NDIC optical images of the same area of a 4H-SiC sample with two different epilayers. a) First epilayer, b) second epilayer, after the first was removed. Note triangular features growing from scratches
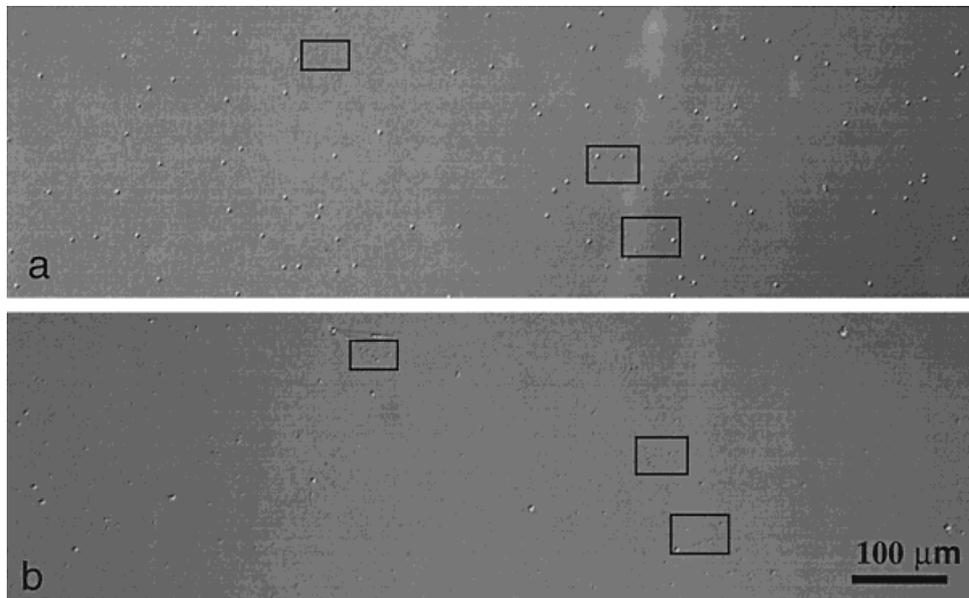

Fig. 7. NDIC optical images of the same area of a 6H-SiC sample with two different epilayers. a) First epilayer, b) second epilayer, after the first was removed. Boxes indicate growth pits common to both epilayers

b) In the 6H epilayers (Fig. 7), there are two groupings of growth pits: large and small. There does not appear to be any correlation between the large pits seen in the two 6H epilayers. Also, the density of large pits is much smaller in epilayer 2; whereas the density of the small pits is about the same. For convenience of comparison, we have put boxes around three groupings of small pits. These small pits are present in both epilayers 1 and 2.

The immediate first conclusion from Figs. 6 and 7 is that all features in the 4H epilayers and the large growth pits in the 6H epilayer are caused by surface defects; that is, from the polishing. The second conclusion is that many of the small pits the 6H epilayer are caused by bulk defects in the substrate.

The above procedure of removing epilayers, repolishing the surface, regrowing epilayers, and making before and after comparisons is very useful in tracking the source of epilayer defects. In the past, comparing epilayers grown on different samples was frustrating because of the variability of the results. The reason, in retrospect, is that poor polishing procedures probably contributed to variable surface quality.

As mentioned in Section 3, micrometer-sized holes, probably due to plasma etching, were observed in as-received wafers. In one experiment, three specific $0.5\,\mu m$ diameter holes were identified by AFM in an as-received substrate, and then in the subsequent epitaxial film grown on this substrate. These holes were deeper than the detection limits of the AFM probe tip. A shallow growth pit occurred at each of these three holes and the holes were located at the up-step end of each pit. This demonstrates that holes produced by post-polishing etching can play a role in the formation of epilayer growth pits.

Based on the above observations, it appears that growth pits can be caused by different sources. We are not at the point where we can identify the source of each and every pit. For example, we do not know the cause of the specific pit shown in Fig. 7. As stated in the previous section, holes in the surface cause some pits. Polishing damage causes some pits, and bulk defects cause some defects. As we eliminate each known cause, the pit density should decrease. The procedure, described above, whereby a given substrate is reused several times (i.e. repolished, followed by a new epitaxial growth), can be used to determine the source of specific growth pits.

5.2 Effect of tilt angle

Epitaxial growth runs were carried out to confirm the effect of larger tilt angle (8° versus 3.5°) on the morphology of 4H epilayers. Transmission electron microscopy (TEM) was used to study structural defects and to confirm the presence of 3C-SiC in the triangular-shaped features.

Epilayers grown on 4H substrates with tilt angles of 3.5° and 8° in the same growth run are shown in Fig. 8. As can be seen, the triangular features are entirely absent in the epilayer grown on the 8°-tilt substrate. In general, the epilayer morphology of the 8° 4H samples exhibited fewer localized defects than the 3.5° 4H samples. However, the pregrowth etches used to remove scratches were less effective for samples with larger tilt angles; hence, remnants of polishing scratches seen in the epilayer in Fig. 8b is a typical result.

The growth results with the 3.5° and 8° 4H samples do confirm that the triangular features (3C-SiC inclusions) can be largely eliminated by growing on 4H substrates with large tilt angles. It remains to be seen if there will be a price to be paid for using large tilt angles. For example, an electrical anisotropy resulting from large tilt angle could be
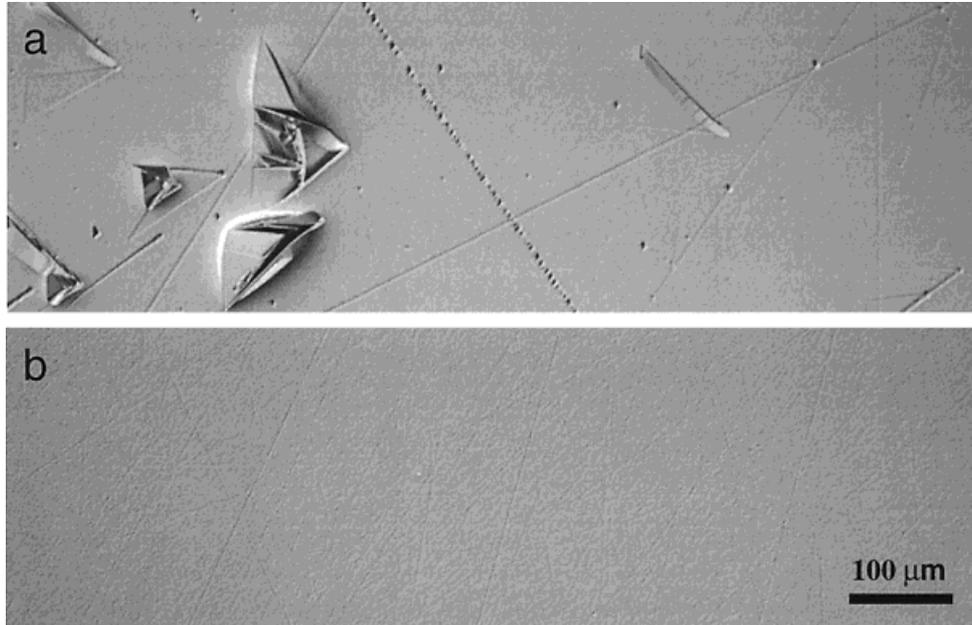
Fig. 8. NDIC optical image of 12 μm thick 4H-SiC epilayers grown on 4H-SiC substrates with tilt angles of a) 3.5° and b) 8°

a negative factor in the operation of some devices. One can speculate that perhaps such large tilt angles will not be necessary when the 4H substrates are polished and prepared in a manner that does not leave surface defects which can cause 3C inclusions.

5.3 Effect of polytype (6H versus 4H)

Epilayer of 4H were more susceptible than 6H to 3C inclusions. For example, triangular patterns frequently seen [15] in 4H epilayers, but seldom in 6H, were characterized by oxidation [18] and found to contain surface layers of 3C-SiC within some of the triangular areas. Cross section TEM demonstrated the presence of thin planar 3C sections parallel to the (0001) plane in 4H epilayers containing a high density of the triangles. Also, we attempted to grow homoepitaxial films of 4H and 6H on 0.4° tilt 4H and 6H substrates, respectively, in the same growth runs. In every case, no continuous films of 4H were achieved, only 3C films with a high density of double positioning boundaries (DPBs) [7] and isolated 4H hillocks were obtained. In contrast, continuous 6H films on 6H substrates were achieved in most cases. At present, we do not know why 4H is more susceptible than 6H to 3C inclusions.

5.4 Effect of precursor concentration

The result of a series of three 6H-SiC epilayer growth runs with different silane and propane concentrations, but constant Si/C ratio, is shown in Fig. 9. In these runs, the Si/C ratio was constant at 0.19. The silane concentration for the three runs was Fig. 9a (run 2120): 170 ppm, Fig. 9b (run 2121): 200 ppm, and Fig. 9c (run 2119): 220 ppm.
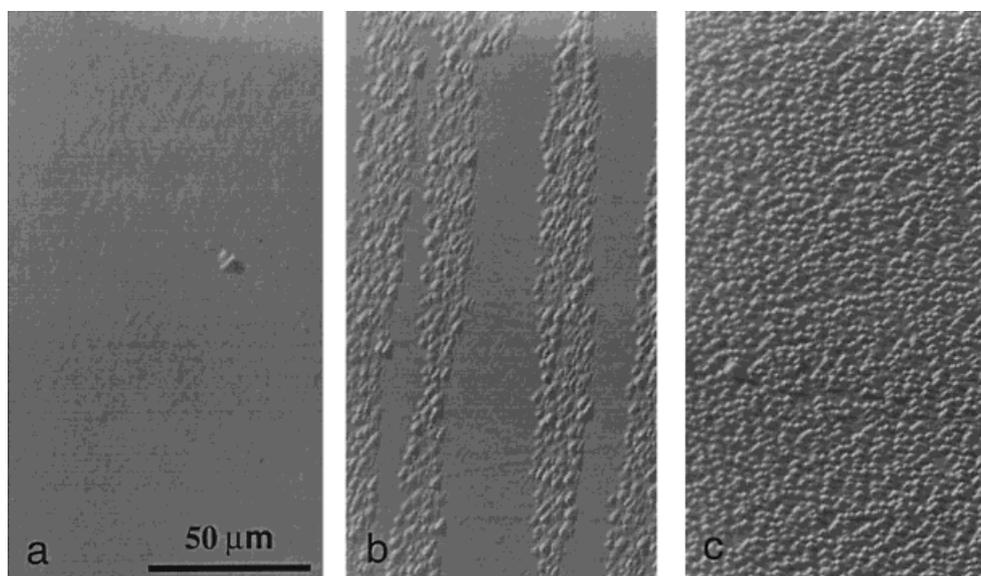
Fig. 9. NDIC optical image of 6H-SiC epilayers grown with an Si/C ratio of 0.19, but with different SiH_4 and C_3H_8 concentrations. Silane concentrations were a) 170, b) 200, c) 220 ppm

Note that the first run in the sequence was Fig. 9c, then Fig. 9a, and then Fig. 9b. This demonstrates that increasing the concentration of the precursors increases the probability of the formation of growth pits. Apparently, the step flow cannot keep up with the higher flux or Si-containing and C-containing species at the surface.

The epilayer results shown in Fig. 9 demonstrate that growth conditions can also be a factor in the formation of growth pits. This is important because, in the application of site-competition epitaxy [11] to dope SiC epilayers, a large range of Si/C ratios (and perhaps large concentrations of either precursor) may be desired.

5.5 Substrate edge effects

We found that the size and position distribution of substrates within the CVD reactor were also factors in determining the growth pit density. For example, when substrates of size $7.5 \times 6\,mm^2$ and about four times larger (i.e. a quarter wafer) were included in the same growth run, the larger substrates consistently yielded epilayers with a lower pit density. When four $7.5 \times 6\,mm^2$ substrates were arranged on the susceptor in a closely-spaced 2×2 array, the resulting films tended to have a lower pit density than with a single isolated $7.5 \times 6\,mm^2$ substrate. The resulting growth pit density was typically higher near the edges of an isolated substrate or near the outside edge of a closely-grouped set of substrates. We suspect that contamination from the susceptor plays a role in this edge effect.

6. Step Bunching

As mentioned previously, the thickness of a single SiC double-layer in the c-axis stacking direction in SiC polytypes is 0.25 nm, and the unit heights (c-axis repeat distance) of
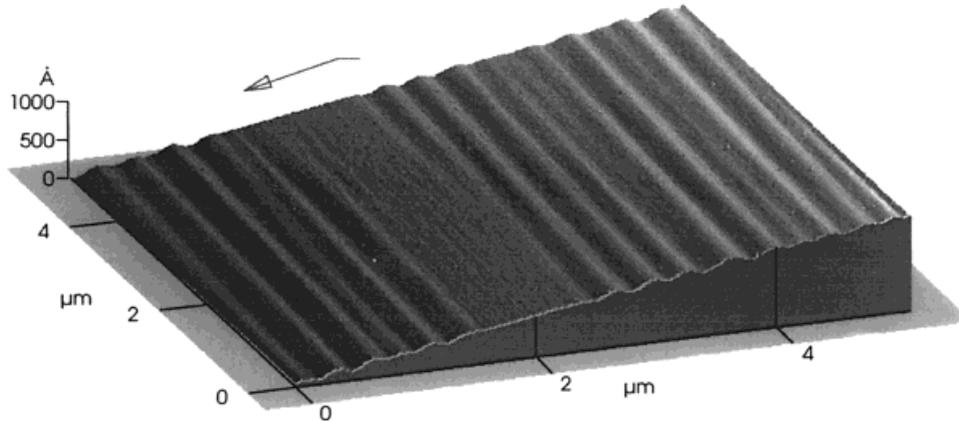
Fig. 10. AFM image of large steps on a 6H-SiC epilayer illustrating the nonuniform distribution of steps. Step height: approximately 25 nm

the 6H and 4H polytypes are 1.5 and 1.0 nm, respectively. AFM observations of SiC epilayers confirmed Tyc's observations that steps much larger than these values can occur in epitaxial films grown on SiC substrates. Our observations revealed that step heights and morphologies varied widely for the SiC films studied. Large steps were evident over some millimeter-sized regions, but were absent over other millimeter-sized regions. Step heights ranged from less than 1 nm to greater than 24 nm. For large steps, some had fairly flat terraces and sharp edges, others had very rounded edges. Fig. 10 illustrates the occurrence of a relatively flat area next to periodic arrays of large steps. We have not yet observed any correlation between step height, morphology, and the growth conditions.

6.1 Anisotropic step bunching

Isolated hexagonal hillocks were observed in both 4H and 6H epilayers grown on substrates with tilt angles less than $0.5°$. Step bunching on the hillocks was quite different from the typical behavior shown in Fig. 10. Multiple spiral patterns of growth steps, assumed to be caused the by screw dislocations, propagated from the peak of each hillock. An example is illustrated in Fig. 11, which shows two spirals of 0.5 nm high steps propagating from the peak of a hillock grown on a 4H substrate. Each 0.5 nm step is a doublet step of the basic 0.25 nm high SiC bilayer step. The spiral evolves into a hexagonal pattern as shown. Since the total height of the two steps is 2×0.5 nm $= 1.0$ nm, the repeat height (Burgers vector) for this screw dislocation is equal to the repeat height of the 4H polytype. Thus, each 0.5 nm step is one of the two doublet steps of the 4H stacking sequence. As can be seen from Fig. 11, the doublet steps bunch to form a wide step, narrow step combination step with a height of 1.0 nm in the $\langle 1\bar{1}00 \rangle$ directions (e.g. $[10\bar{1}0]$ and $[01\bar{1}0]$). As the growth direction rotates to the next $\langle 1\bar{1}00 \rangle$ direction, the step pattern undergoes a transition at the $[11\bar{2}0]$ direction. At this transition direction, the step heights revert back to a doublet step height, i.e. 0.5 nm. This demonstrates that step bunching is dependent on the growth direction (i.e., it is anisotropic with respect to growth direction).
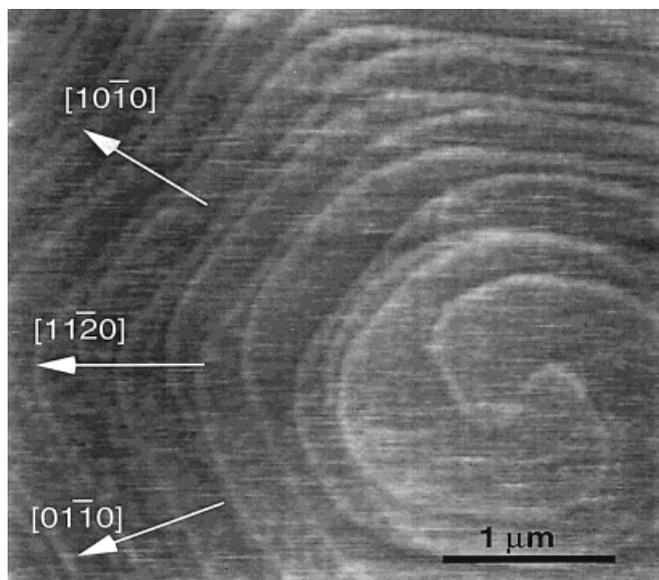
Fig. 11. AFM image of spiral steps propagating from the center of a 4H-SiC hillock

6.2 Model for anisotropic step bunching

The following is a model which we have proposed [19] to explain the anisotropic nature of the step bunching. First, a few aspects of SiC polytypism must be recalled. The 6H structure consists of the stacking of alternate triplet-step layers of the 3C polytype and these are usually designated as ABC and ACB. The difference in structure between these two triplet-step layers is a rotation of 60° about the stacking axis (the c-axis). Similarly, the 4H structure consists of alternate doublet-step layers of the 3C polytype and are designated AB and AC. Sakamoto et al. [20] pointed out that for steps on a Si(111) surface, there are either two dangling bonds per atom or one dangling bond per atom on the step riser depending on the crystallographic direction of the step. Because of threefold symmetry of Si(111), the number of bonds per atom alternates every 60° between one and two as the direction rotates about the surface normal. They suggested that faces (steps) with two dangling bonds per atom grow faster than faces with one dangling bond per atom. We applied these ideas to SiC with the following result. For a given $\{1\bar{1}00\}$ face of 6H-SiC, there is a particular pattern of one and two dangling bonds per atom; if we assume, for example, that the ABC triplet-step layers in a stacking sequence have one dangling bond per atom on this given $\{1\bar{1}00\}$ face, then the other triplet-step layers in the sequence (the ACB layers) on this same $\{1\bar{1}00\}$ face will have two dangling bonds per atom. If one examines the pattern of bonds per atom on adjacent $\{1\bar{1}00\}$ faces, the pattern is reversed: the ABC triplet-step layers have two bonds per atom, and the ACB triplet-step layers have one bond per atom.

We use ideas of the previous section to explain the anisotropic step bunching demonstrated in Figs. 11 and 12 (a special case of a super screw dislocation). We will use the 4H hillock depicted in Fig. 11 to describe the model. If, in the case of Fig. 11, we designate the top (wider) doublet steps in the $[10\bar{1}0]$ direction as AB doublet steps and as-
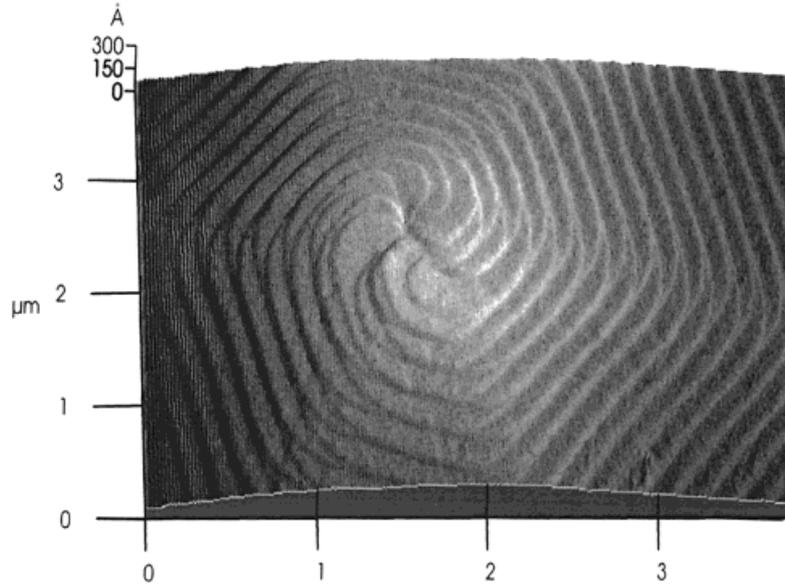
Fig. 12. AFM image of spiral steps propagating from the center of a 6H-SiC hillock. Steps are produced by a super screw dislocation

sume that AB steps have two dangling bonds per atom, they will grow faster in this direction than the AC doublet steps which have only one dangling bond per atom; hence, step bunching of doublet-step pairs will occur as shown. If we examine growth in the adjacent $\langle 1\bar{1}00 \rangle$ direction (e.g. the $[01\bar{1}0]$ direction) the AB steps will now be growing slower because they will have only one dangling bond per atom, and the AC steps will now be growing faster; hence reversed step bunching will occur. In this new direction (i.e. $[01\bar{1}0]$), the faster growing AC steps becomes the top (wider) step, overtaking the slower growing AB steps. The transition between these two states causes a localized "debunching" of the paired doublet steps in the $[11\bar{2}0]$ direction between the two adjacent $\langle 1\bar{1}00 \rangle$ directions. The same process occurs for 6H-SiC triplet steps as shown in Fig. 12.

Calculations were recently carried out by Heuell et al. [21] on the lateral growth of steps on a 6H-SiC vicinal (0001) surface tilted in a $\langle 1\bar{1}00 \rangle$ direction. They assumed (1) single bilayer steps on the surface and (2) each successive group of steps consists of one dangling bond per atom on the leading step edge of three successive steps followed by two bonds per atom on the next successive three steps. The result of the calculations indicated that the single bilayer steps structure would evolve into a structure with a step height of six bilayers. Our results are consistent with these calculations. Also, our model explains the occurrence of 0.75 nm height steps when 1.5 nm high steps turn by 60° as observed by Tyc [22] on a sublimation-grown epilayer on a 6H-SiC Lely crystal.

As can be seen in Figs. 11 and 12, the transition between the two bunched-step orientations in adjacent $\langle 1\bar{1}00 \rangle$ directions occurs over a very small angular change in growth direction in the vicinity of the $\langle 11\bar{2}0 \rangle$ direction between these two $\langle 1\bar{1}00 \rangle$ directions. The instability in step bunching in this transition region may be a factor in the macro scale

step bunching that is observed in the SiC epilayers. Any small undulation of the growth surface, or defect on the surface could aggravate the effect of this instability. This may be significant since most SiC epilayer growth is carried out on vicinal (0001) wafers tilted toward a $\langle 11\bar{2}0 \rangle$ direction.

6.3 Super screw dislocation

The unusual hillock shown in Fig. 12 was grown on a 6H substrate. It consists of 16 growth steps propagating from the center of the spiral. The number 16 was determined by following a specific step around one complete revolution and counting the number of steps along the transition region back to the starting point. Each of these 16 steps is a triplet step, $3 \times 0.25\,\text{nm} = 0.75\,\text{nm}$ high. These triplet steps bunch into 8 triplet-step pairs in the $\langle 1\bar{1}00 \rangle$ directions. The bunching forms single large steps rather than wide step, narrow step combination steps as was observed for 4H. Each triplet-step pair has a total height of $2 \times 0.75\,\text{nm} = 1.5\,\text{nm}$, the repeat height of the 6H polytype. The Burgers vector for this screw dislocation is equal to $8 \times$ the repeat height of the 6H polytype (total height: 12 nm). Screw dislocations with such large Burgers vectors have been called super screw dislocations [23]. The step bunching seen for this hillock is similar to that for the 4H hillock of Fig. 11 except that triplet-step pairs form in the $\langle 1\bar{1}00 \rangle$ directions, instead of doublet-step pairs as was observed for 4H.

Previously, we found that dislocations and micropipes propagate from the SiC substrate into the epilayer [5]. We believe that the observed hillocks are produced from screw dislocation that have their origins in the substrate; however, we do not know the cause of these dislocations. Current thinking is that the strain associated with dislocations with large Burger vectors causes some of these super screw dislocations to become micropipes [4, 24, 25]. The above observations demonstrate that AFM images of epitaxially-grown hillocks can be used to make direct measurements of the Burgers vector of super screw dislocations.

7. Chemical Mechanical Polishing

The results described in Section 5.1 indicated that residual damage caused by cutting and polishing SiC wafers was a major source of growth pits observed in SiC epilayers. In an effort to improve SiC substrate surfaces prior to growth, a collaborative effort between NASA Lewis and Case Western Reserve University (CWRU) was initiated to develop a chemical mechanical polishing process (CMP) for SiC. Based on an idea of P. Pirouz, the use of colloidal silica was successfully applied to SiC [26]. The best surfaces were obtained after colloidal silica polishing under conditions that combined elevated temperatures (approx. $55\,°C$) with a high slurry alkalinity (pH > 10) and high solute content. Removal rates of about 200 nm/h were achieved. Crosssectional TEM showed no observable sub-surface damage, and AFM showed a significant reduction in roughness compared to commercial diamond-polished wafers. The effectiveness of CMP for a 4H-SiC sample are shown in the "before" and "after" AFM images in Fig. 13 where a scratch-free surface was achieved (Fig. 13b) after 5 h of polishing. If the as-received surface of the substrate was more like that shown in Fig. 2b, then the CMP time required to reach a scratch-free state would have been much less. The CMP process for SiC is still in an early state of development and much optimization of parameters is required. Growth experiments following colloidal silica polishing have yielded a signifi-
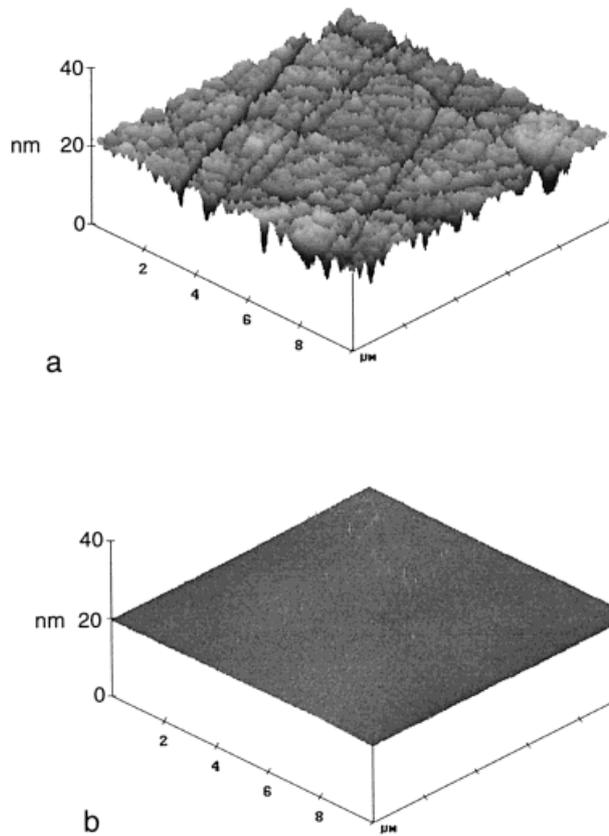
Fig. 13. AFM images of a 4H-SiC wafer, a) as-received surface and b) after chemical mechanical polishing (CMP)

cant reduction in the density of growth pits. For example, the final stage of polishing for the samples in Figs. 6 and 7 was accomplished by CMP. As can be seen in Fig. 6b, several scratches are present in this sample. These were most likely caused by chipping of the sample edge during the CMP. This is a problem that has occurred sporadically in our polishing experiments no matter what type of polishing was being used. Edge rounding prior to the polishing has help reduce this problem.

8. Hydrogen Etching

It has been known for many years that H_2 will etch SiC at elevated temperatures [27] and will produce gaseous hydrocarbons and free silicon. In fact, the growth profile described in Section 4 was developed to reduce the time of heating in pure H_2 to a minimize the formation of free Si droplets on the substrate surface. Recently, H_2 etching prior to SiC CVD growth has been investigated by several research groups. Burk and Rowland [28] reported that Si droplets were formed when SiC was exposed to H_2 at temperatures above the melting point of Si (1410 °C). In addition, they found that Si droplet formation was suppressed over the temperature range 1450 to 1520 °C when there was C_3H_8 present in concentrations of 140 to 1200 ppm. There was indication that etching was taking place at a temperature of 1520 °C and C_3H_8 concentrations below

700 ppm. The SiC CVD of Burk et al. and at NASA Lewis were carried out in cold-wall quartz reactors. In contrast, the SiC research group at Linköping University (LU) has carried out SiC CVD and H_2 etching experiments in a hot-wall graphite reactor and have reported [29, 30] that H_2 can be a useful pregrowth etchant for 4H and 6H SiC substrates. Their reactor environment probably produced an overpressure of hydrocarbons. Their results using pure H_2 as a source gas demonstrated a strong dependence on the tilt angle of the substrate. Etching in H_2 carried out at 1550 °C for 30 min was effective at removing polishing scratches from on-axis (0001) SiC samples. The resulting surface of the 6H samples consisted of parallel steps with a height of 1.5 nm (the *c*-axis repeat distance of the 6H polytype). Under the same etching conditions, scratches were only partially removed from off-axis (3.5°) 4H and 6H SiC samples; the step bunching was less distinct for the off-axis samples. The conditions also produced mesa-like triangular features whose bases were parallel to the steps. The bases of these triangle were much longer (tens of micrometer) than the height of the triangles, producing features that appeared as lines on the surface when viewed with NDIC optical microscopy.
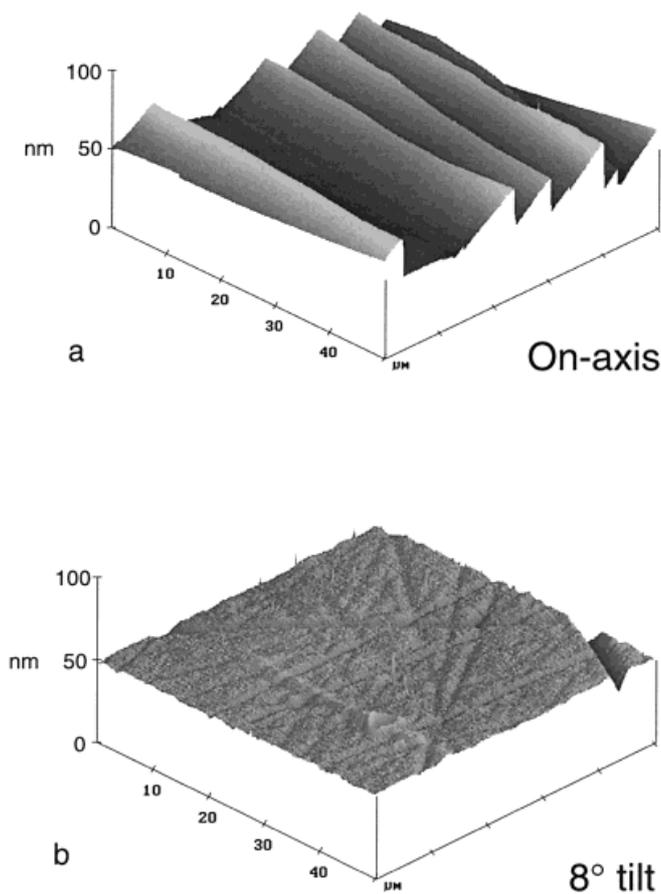

Fig. 14. AFM images of 4H-SiC surfaces after a H_2/C_3H_8 etch at 1575 °C for 30 min. a) On-axis 4H-SiC sample and b) 8° off-axis 4H-SiC sample
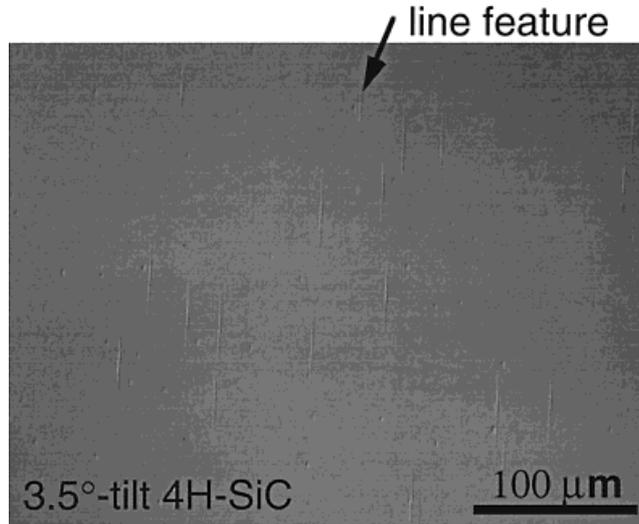
Fig. 15. NDIC optical image of a 3.5° off-axis 4H-SiC surface after a H_2/C_3H_8 etch at 1575 °C for 30 min showing elongated triangular "line" features

An investigation of H_2 etching of 4H and 6H SiC substrates was carried out at NASA Lewis in a cold-wall quartz reactor. In order to suppress Si droplet formation, 100 ppm of C_3H_8 was added to the H_2 carrier gas. Typically, etching was carried out at 1575 °C for 30 min. The NASA results were similar to that of the LU group. For the on-axis samples, the H_2 etching removed polishing scratches and produced steps due to step bunching. While the steps on the on-axis 6H samples were 1.5 nm in height, the steps on the on-axis 4H samples were tens of nm in height as shown in Fig. 14a. This is much larger than the 1 nm height of c-axis repeat distance of the 4H polytype. For the off-axis samples, scratches were only partially removed from 4H and 6H samples. A result for an 8° off-axis 4H sample is shown in Fig. 14b. The "line" features observed by the LU group for 3.5° of-axis 6H samples were also observed in the NASA work as shown in Fig. 15. There was much more of a tendency for the H_2 etching to decorate defects in 3.5° off-axis 4H samples than in the 8° off-axis 4H samples. Growth runs carried out using the schedule shown in Fig. 3b were carried out to compare pregrowth etches of H_2/HCl and H_2/C_3H_8. The typical 4 min, 1400 °C H_2/HCl pregrowth etch was more effective in producing an epilayer free of scratch remnants than a 30 min, 1575 °C H_2/C_3H_8 etch. It appears that H_2/C_3H_8 etching may be useful for on-axis substrates and for decorating defects.

9. Concluding Remarks

From the above sections, it is clear that there are a sequence of processes that can impact the morphology of SiC epilayers. The first (and most important) process is the growth of the bulk crystal since micropipes and dislocations are known to propagate into SiC epilayers. The increasing number of SiC developers who use commercial wafers are at the mercy of the quality of the wafers available from the few commercial SiC bulk crystal growers.

A second set of processes is that of cutting and polishing the wafer. The finding that these processes are having a major impact on morphology was somewhat surprising. It had been assumed that the defects in the bulk crystal were the dominant cause of morphological defects. Wafer users may be forced to repolish wafers to achieve scratch-free and damage-free surfaces. This problem of imperfect wafers surfaces prompted NASA Lewis to develop an in-house polishing capability and to collaborate with others to develop new polishing processes. The lead to the development of a new SiC CMP process. Although in an early state of development, it shows promise of being suitable for the final stage of polishing which will provide a scratch-free surface free of subsurface damage. Our characterization of commercial wafers showed that at least one supplier can produce a nearly scratch-free surface. Hopefully, commercial SiC wafer suppliers will be able to apply this new technology and provide the required polished surfaces that will yield improved SiC epilayers.

Another important process is the pregrowth etch to improve the growth surface, although with improved starting surfaces, this process may not be as important in the future. The H_2/C_3H_8 may prove to be useful in the future in decorating defects in wafers and epilayers.

The final process is the actual epilayer growth procedure. The challenge here will be to grow epilayers with uniform thickness and doping. The growth conditions presented herein cover only a narrow range of possible operating conditions. Much work is still required in order to achieve excellent morphology under the various conditions that will be required to achieve epitaxial films with large area and wide doping ranges.

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