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E787 TN-319

# 500 MHz Transient Digitizers based on GaAs CCDs

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**Abstract**

A system of 500 MHz transient digitizers based on gallium arsenide resistive gate charged coupled devices has been developed for an experiment studying rare K decays. CCDs with dynamic range of 8-bits and 128 or 320 pixels are used as analog pipelines. The CCDs are driven by a single phase transport system. Data readout and manipulation occurs at 15.6 MHz.

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# 1 Introduction

Pipeline digitizing of detector signals is a powerful technique for measuring time, amplitude and shape variations due, for example, to pulse pile-up. Experiment E787 at Brookhaven National Laboratory (BNL) is a measurement of the ultra-rare decay $K^+ \rightarrow \pi^+\nu\overline{\nu}$ which is expected to have a branching ratio in the range $1-3\times10^{-10}$[1]. To achieve effective background suppression at such low signal levels while operating at very high rates, two types of high speed digitizers were developed for sampling fast scintillation counter signals from photomultiplier tubes. Approximately 300 channels of 8-bit 500 MHz digitizers based on flash ADCs are employed in E787 to cover the $10\mu$s time span of the $\pi-\mu-e$ decay sequence[2]. To satisfy the requirement for an additional 1000 digitizer channels covering the time scale of K decay (approximately 100 ns), a new type of 500 MHz digitizer was developed based on gallium arsenide (GaAs) charge coupled devices (CCDs).

GaAs is a suitable material for construction of high speed devices because electron mobility is high; GaAs CCDs have been reported to operate at 4.2 GHz[3]. In our application, an analog signal from a photomultiplier tube (PMT) is presented to the CCD input where it is transformed into charge packets. The packets are sequentially transported as in a bucket brigade to the CCD output. When the external trigger system indicates that an event of interest has occurred, the CCD shift speed is reduced for readout into a lower speed digitizing device.

A layout of the E787 rare K decay spectrometer is shown in fig. 1 . The beam of 800 MeV/c positive kaons is degraded and stopped in a plastic scintillator-fiber target[4] consisting of 400 elements; each 5 mm$\times$5 mm fiber

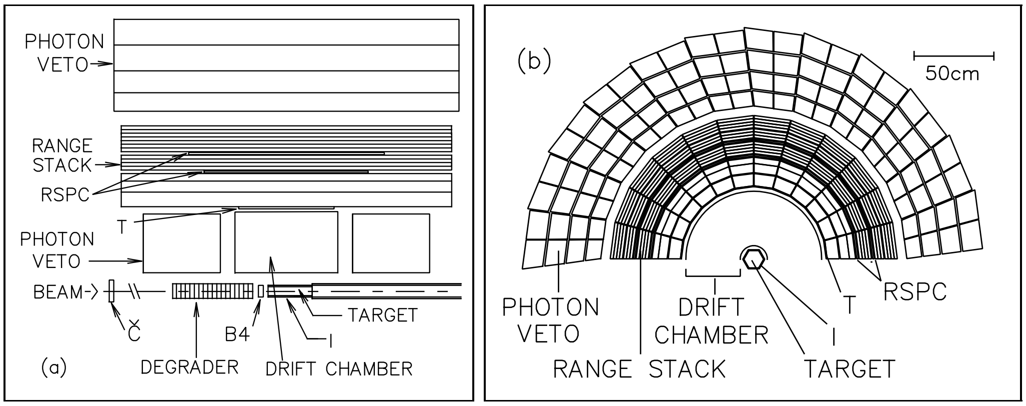


Figure 1: Side (a) and end (b)view schematics of the E787 detector. Č: beam Čerenkov counter; B4: beam hodoscope; I and T: trigger scintillators; RSPC: wire chambers.

is read out by a PMT giving pulses with 3 ns rise times and 15 ns fall times. Charged decay particles are tracked in a 1 T magnetic field through the cylindrical drift chamber and come to rest in the range stack consisting of 2 cm thick plastic scintillation counters which are viewed by PMTs. The PMT output signals are digitized by the 500 MHz FADC transient digitizers. Inside the magnet the detectors are surrounded by a nearly $4\pi$ sr photon veto system consisting of a barrel detector (Pb-scintillator sandwich) and endcap detectors (located upstream and downstream of the drift chamber) made of 143 crystals of pure CsI, read out by high field PMTs[5]. Pure CsI has a fast light output component with a 5 ns time constant and a slow component with time constant of 40 ns. In the initial implementation of the CCD digitizer system to be described in this paper, approximately 700 channels of 8-bit 500 MHz digitizers using 128 pixel or 320 pixel CCDs were deployed to cover the target fibers and the CsI crystals.

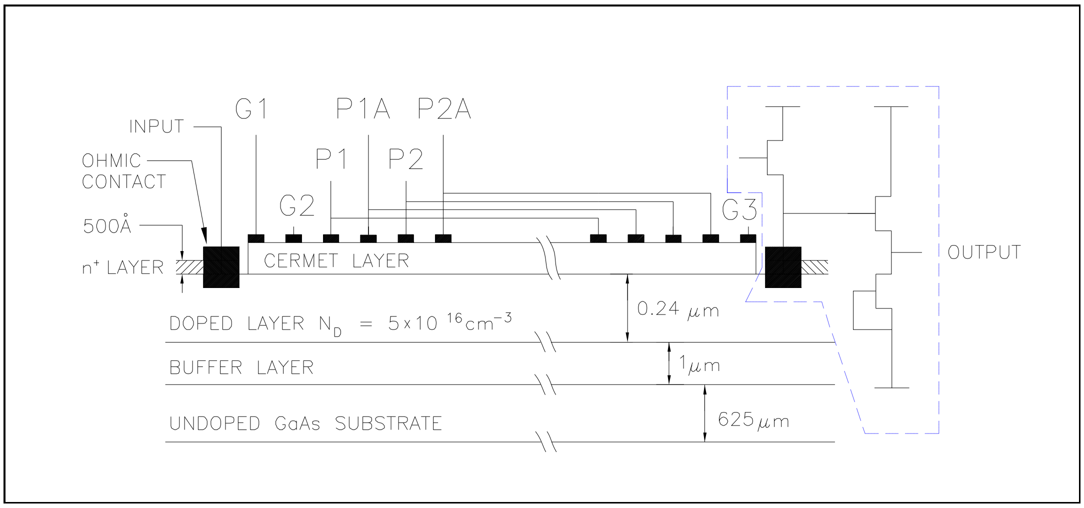


Figure 2: GaAs resistive gate CCD. The layers shown include the cermet layer on which Schottky gates (G1-G3) and the CCD pixels (P1, P1A, P2 and P2A) are deposited, a 500 $\AA$ $n^+$ layer (integrated with the ohmic contacts) with doping density $N_D > 1 \times 10^{18}cm^{-3}$, a $0.24\mu m$ thick n-active layer doped with $N_D = 5 \times 10^{16}cm^{-3}$, a $1\mu m$ thick intrinsic-buffer layer with $N_D < 1 \times 10^{14}cm^{-3}$ and a $625\mu m$ thick undoped semi-insulating LEC GaAs substrate. The dotted lines enclose an integrated switched charge amplifier.

In the following sections, the GaAs CCD, the digitizer and the readout system are described and the initial performance experience with the system is discussed. A report on the prototype CCD digitizers was given in [6].

# 2 CCD

GaAs resistive gate CCDs (RGCCD) were developed by Higgins *et al.*[7]. Figure 2 shows the primary regions of the RGCCD. The input section which is used for waveform sampling and establishment of boundary conditions consists of an input ohmic contact and two Schottky barrier control gates (G1 and G2). Each CCD pixel in the transport region has four resistive gates (P1,P1A,P2 and P2A) which store and transport the charge packets corresponding to the input signal. The output section which converts the charge packets to discrete voltage levels contains a Schottky barrier control gate (G3), an output ohmic contact, a reset MESFET and an output MESFET amplifier.

The RGCCDs described in this work were fabricated at TRIUMF. Conventional contact photo-lithography was used to define the photo-resist patterns for six mask layers used in manufacture: ohmic contacts; proton isolation implants; resistive gates; Schottky gates; interconnect vias, and; interconnect metal. Photo-resist lift off methods were used to pattern the metal features and the resistive gates. A dielectric polyimide layer isolated the Schottky gates from the interconnect metal and plasma etching techniques were used to pattern the interconnect vias. A Cr-SiO film with a sheet resistance of about $1\mathrm{M}\Omega/\Box$ was used for the resistive gates. Proton isolation implants at 35, 100 and 200 KeV with fluences of $2 \times 10^{13}\mathrm{cm}^{-2}$ were used. A micro-graph of a 128-pixel RGCCD is shown in fig. 3.

UHF operation of the RGCCD using a uniphase clock was developed by LeNoble and Cresswell[8] and is illustrated in fig. 4. The electrodes are adjusted so that a potential well is formed under the P1 or P2 electrode on the negative or positive levels of the applied clock waveform. As shown in fig. 4a, the clock voltage is at its minimum at time $t = t_0$. A small signal charge is introduced into the channel as shown in fig. 4b such that the local potential energy is not significantly perturbed. This charge will be drawn towards the energy minima below the P1 electrode. On the positive clock transition occurring at $\mathrm{t}=\mathrm{t}_1$ through to $\mathrm{t}=\mathrm{t}_2$, a potential well forms below the

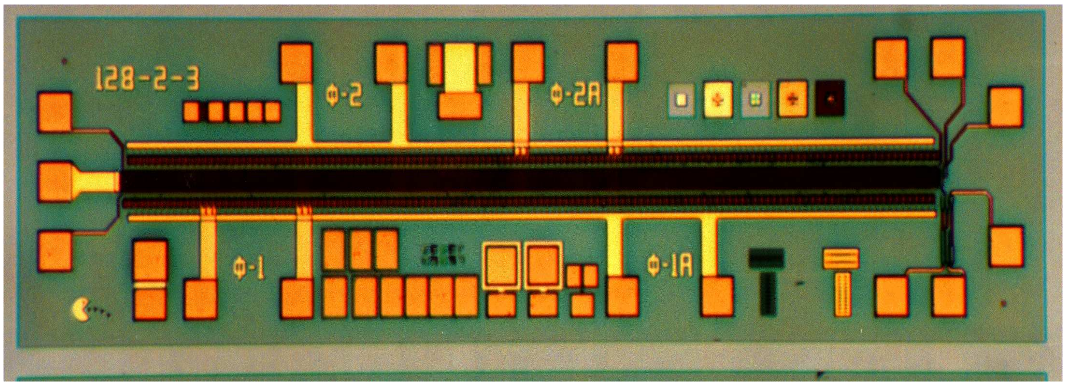


Figure 3: Micro-graph of a 128-pixel GaAs RGCCD. The device is about 3 mm long.

P2 electrode, resulting in the motion of the signal charge along the channel from P1 through P1A to P2. The channel potential varies monotonically between the transmitting and receiving potential wells during the transfer period as a consequence of the surface potential control offered by the resistive gates. This transfer process occurs again on the negative clock transition from P2 through P2A to P1' at $t = t_3$ resulting in the charge packet being shifted along one pixel of the RGCCD. During readout, which occurs at 15.6 MHz, the charge packets contained in the CCD are transformed to a voltage waveform by the output circuits.

Figure 5 shows a CCD digitizer output for an input square wave pulse with amplitude 0.3 V and width 50 ns acquired at 500 MHz. Minimal dispersion of the leading edge of square wave pulses suggests that the RGCCD was operating at the 250 MHz Nyquist frequency limit. The magnitude response of the RGCCD is shown in fig. 6. The data was obtained using a 0.3 V peak amplitude, 50 ns wide pulse applied to the digitizer and incrementally

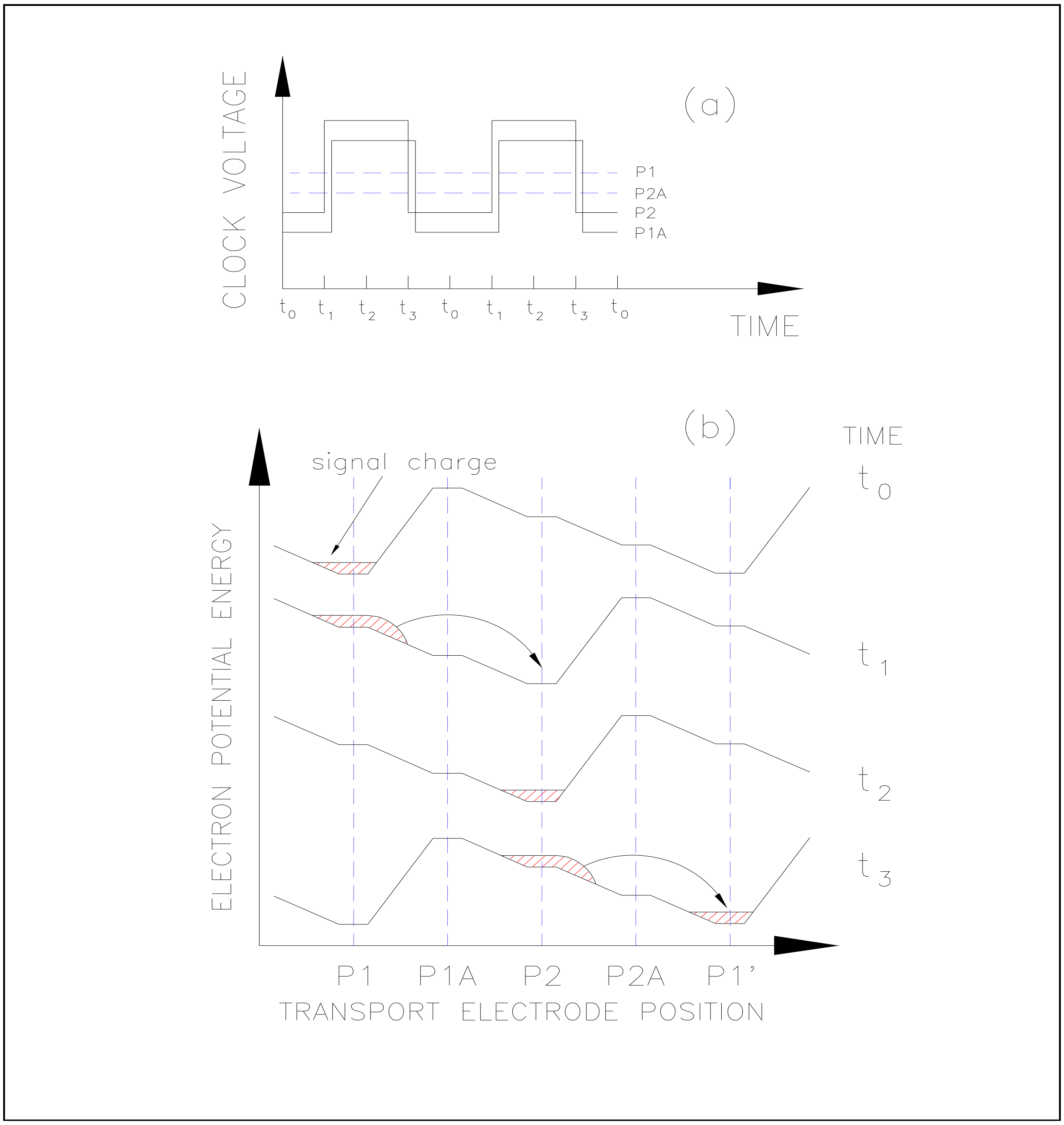


Figure 4: Illustration of the uniphase operation of the CCD as described in the text: a) time progression of clock levels, and b) charge progression within the CCD transport system.

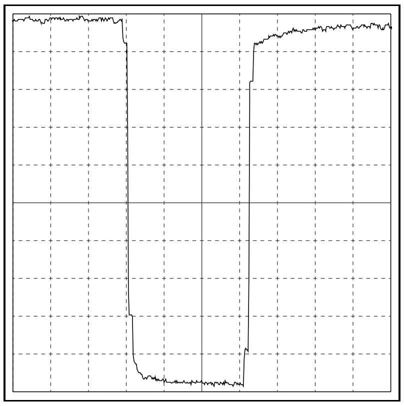

Figure 5: CCD digitizer output for a 0.3 V square wave input pulse with width of 50 ns. This output trace (vertical scale of 100 mV/div and horizontal scale 500 ns/div) was obtained using a digital-to-analog conversion.

attenuated through 48 dB. The data can be well characterized by a 3rd degree polynomial fit.

# 3 Digitizer System

A block diagram of the CCD digitizer system is shown in fig. 7. A 500 MHz synthesizer provides clock signals to a FASTBUS format master trigger module (MT) which feeds slave trigger fanout (ST) boards located on FASTBUS digitizer mother cards (MC). Details of the MT and ST boards are given in Appendices A and B, respectively. The MT module supplies clock signals to 8 (three unit wide) digitizer MCs. Each MC accommodates 16 CCD digitizer cards giving a total of 128 digitizers in each CCD FASTBUS crate.[1] The output of the digitizer card is an 8-bit differential ECL stream which is

[1] Only power lines from the FASTBUS backplane are used in these crates.

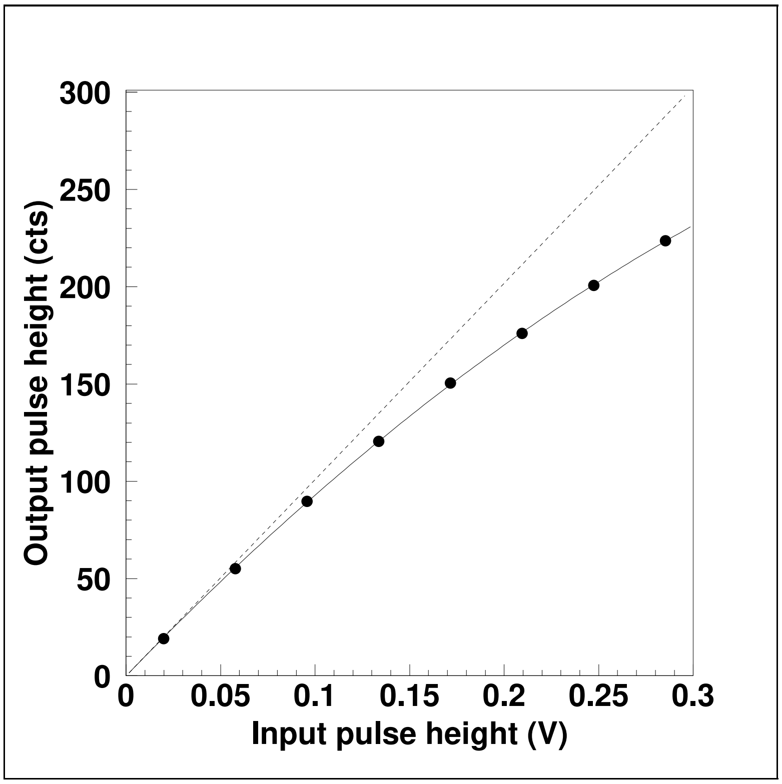


Figure 6: Output pulse height vs. input voltage for a typical CCD digitizer. The data points are fit with a cubic polynomial (solid line) and the dashed line represents the ideal linear response.

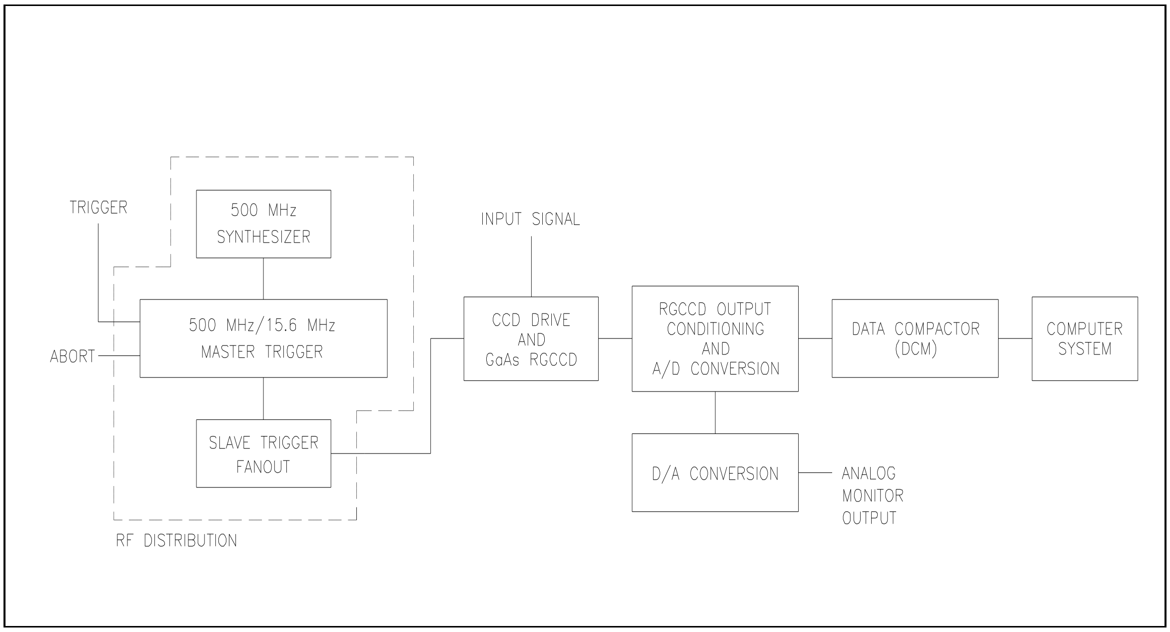


Figure 7: Block diagram of the GaAs CCD transient digitizer system.

transmitted via ribbon cable to data compactor modules (DCM) housed on full-function FASTBUS cards in a separate crate. In data acquisition mode, the digitizer cards receive 500 MHz clock signals via the ST boards. When a system trigger (level 0) signal is received, the MT switches the clock feed from 500 MHz (HIGH) to 15.6 MHz (LOW) initiating the readout cycle of 128 8-bit words from the digitizers to the DCMs. A higher level trigger (level 1) can abort the event, in which case the system returns to acquisition mode at 500 MHz.

The digital outputs from two crates of digitizers (256 channels) are fed to one crate of DCMs. Processed data from the DCMs are read out by a SLAC Scanner Processor (SSP)[9], which performs the function of a FASTBUS system master, and then transferred to the host computer.

The CCD digitizer card is a multi-layer double sided printed circuit board with dimensions of 15 cm x 4 cm employing surface-mount parts with some through-hole parts. The four main elements of the CCD digitizer card are the clock drivers, the input circuit, the output circuit and the analog-to-digital converter (ADC). The clock drivers receive the HIGH/LOW clock from the ST to provide clock pulses to the transport section of the CCD and to the CCD reset circuitry. Since the drivers must faithfully reproduce both the high and low frequency clocks with rise and fall times $<$ 250 ps, wide bandwidth GaAs FET switches are used. The clock drivers are hand assembled ("above" the ground plane to reduce the effects of parasitic capacitances) using leaded parts while some of the remaining components are assembled using automated surface mount techniques.

The analog input circuit provides a means to superimpose the input signal onto a dc bias which biases the CCD into the correct operating region. This circuit also allows for the addition of gain to the signal and the isolation of the input signal source from clock feed-through effects present at the CCD input.

The analog output from the CCD is an amplitude modulated rectangular pulse train which is buffered prior to digitizing. The signal is dc restored, amplified and digitized. An offset voltage control and an ADC range control allow the output signal to be windowed into the operating range of the ADC. Digitizing the analog signal is accomplished using a 8-bit 32 MHz FADC. A strobe received from the ST is used as the "Convert" clock signal for the ADC. The digitized data signals are then passed through front panel connectors and external ribbon cable to the DCM described in the next section.

# 4 Data Compactor Modules (DCM)

## 4.1 Overview

Data from the CCD digitizers consists of signal pulses (events) and noise superimposed on a background level or pedestal. The pedestal is subtracted prior to saving data which exceed a preset threshold. Eight-bit event data must also be formed into 32-bit words for readout via FASTBUS. Each DCM was designed to compact data from a CCD mother card containing 16 digitizer channels. Design criteria for the DCMs included the following: memory size accommodating up to 256 8-bit words, speed up to 32 MHz, data ready for readout in less than 10$\mu$s, pedestal subtraction individually programmable for every CCD pixel of each channel, data threshold individually programmable for each channel, skirt width programmable for each channel (see below), memory-efficient data format in FASTBUS and density of 256 channels per FASTBUS crate.

The method chosen for implementing the data compaction function was the mask-programmable gate array because it offered the required combination of speed, price and function (number of usable gates per chip). One custom gate array is used for each digitizer channel, with a further 3 arrays in the FASTBUS interface (one PCL [10] and two ADIs [11]). Each FASTBUS module supports 16 channels.

## 4.2 DCM System

Figure 8 shows the system interconnections to the DCM. Timing information is derived from the MT, which also generates clocks for the CCD digitizer modules. A 15.6 MHz clock and an accompanying envelope signal are passed from the MT via a Clock Fanout (CF) module to the DCMs. The CF buffers the clock and distributes it using reserved lines on the FASTBUS backplane. The envelope signal indicates that the data are valid, and hence defines the number of CCD pixels for the DCM. If the Level 1 Trigger issues an abort, the CCD clock speed reverts to 500MHz, the envelope signal to the DCM is cleared and the DCM is reset.

## 4.3 Design

### 4.3.1 Physical Construction

The DCM consists of a multi-layer FASTBUS motherboard incorporating a slave interface and ECL receivers populated by 16 daughter boards (one per channel). Each daughter board contains a gate array and associated FIFO memories which form the compactor associated with one CCD digitizer

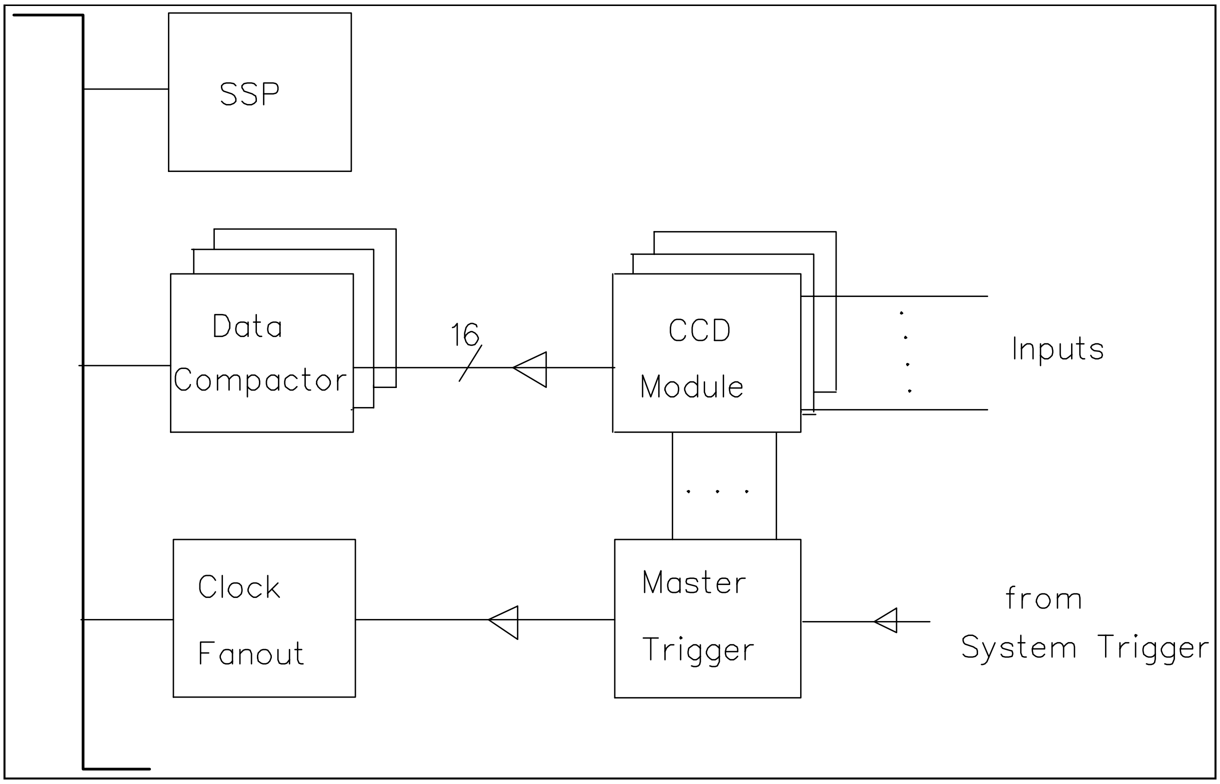


Figure 8: Readout system block diagram

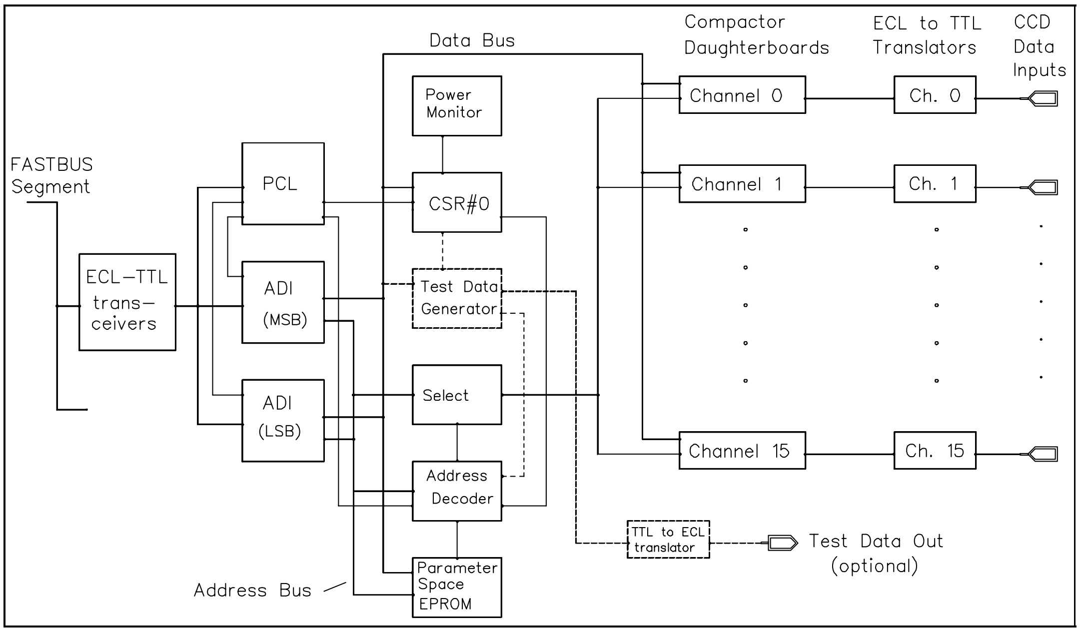


Figure 9: Diagram of the data compactor (DCM) motherboard.

channel. A single-width front panel contains three power supply monitor LEDs and sixteen 16-pin high density (IDC compatible) connectors.

### 4.3.2 Compactor Motherboard

Figure 9 shows the main features of the DCM. The FASTBUS Slave Interface consists of the PCL and ADIs, together with ECL to TTL transceivers. This chip set supports all FASTBUS addressing and data modes and presents a simple TTL interface to the remainder of the board. The PC board is split into separately powered sections each with its own fuse. A power monitor circuit gives an indication of correct supply voltages in each section by an LED, and also by an error bit in CSR#0 (if the FASTBUS interface is functional).

CCD data is fed in at the front panel, translated to TTL, then presented to the daughter boards. Control information is written to the daughter boards via an internal data bus, which is also used to read out the compacted data. Channel select logic allows data from each channel to be individually selected, or data from all channels to be read in a single block transfer operation. A parameter space EPROM is provided, which contains the module serial and asset numbers together with an abbreviated user manual. This information may be read via FASTBUS using standard software. An optional Test Data Generator allows synthetic CCD data to be loaded via FASTBUS and routed to any input channel using a test cable.

#### 4.3.3 DCM Daughter board

Figure 10 shows a block diagram of a DCM daughter board. Most of the functionality of the daughter board is contained in the gate array. External FIFO memories are used to reduce the gate and pin count of the array, so that a smaller array may be used. The 8-bit control bus to the gate array is multiplexed with the 32-bit output data bus from the data FIFOs. Pedestal data is loaded into the pedestal FIFO and clocked into the gate array synchronously with the input data.

#### 4.3.4 Gate Array

Figure 11 shows the main features of the gate array. Operation of the DCM array is controlled by an external clock synchronized with the CCD data. The pedestal is first subtracted from the 8-bit input data. The resulting data are then compared with a preset threshold value. Data which are above threshold are passed to the output where they are assembled into 32-bit

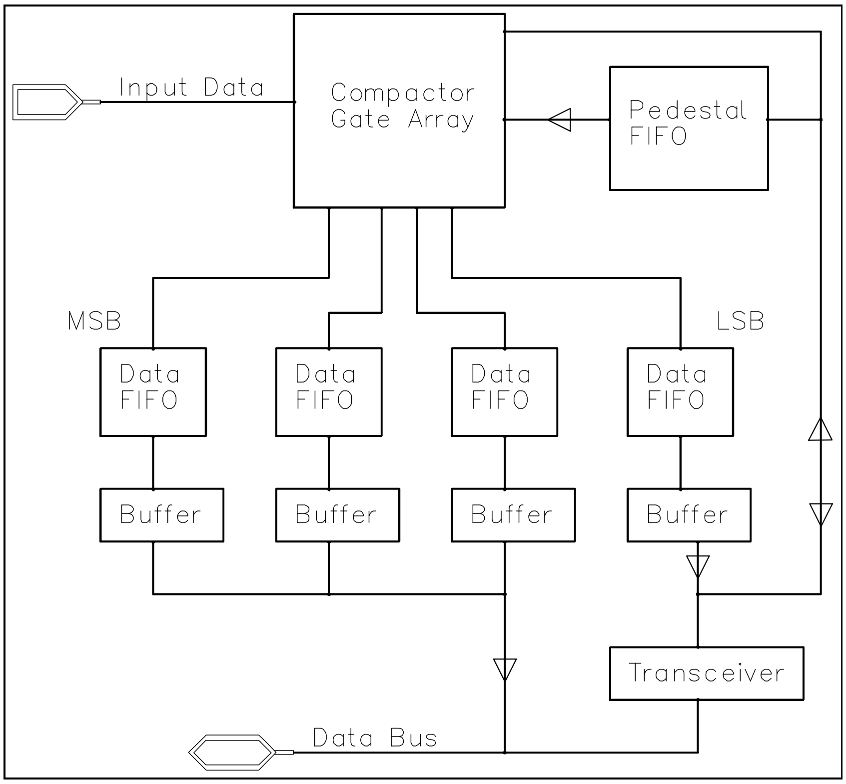


Figure 10: Diagram of the data compactor daughter card.

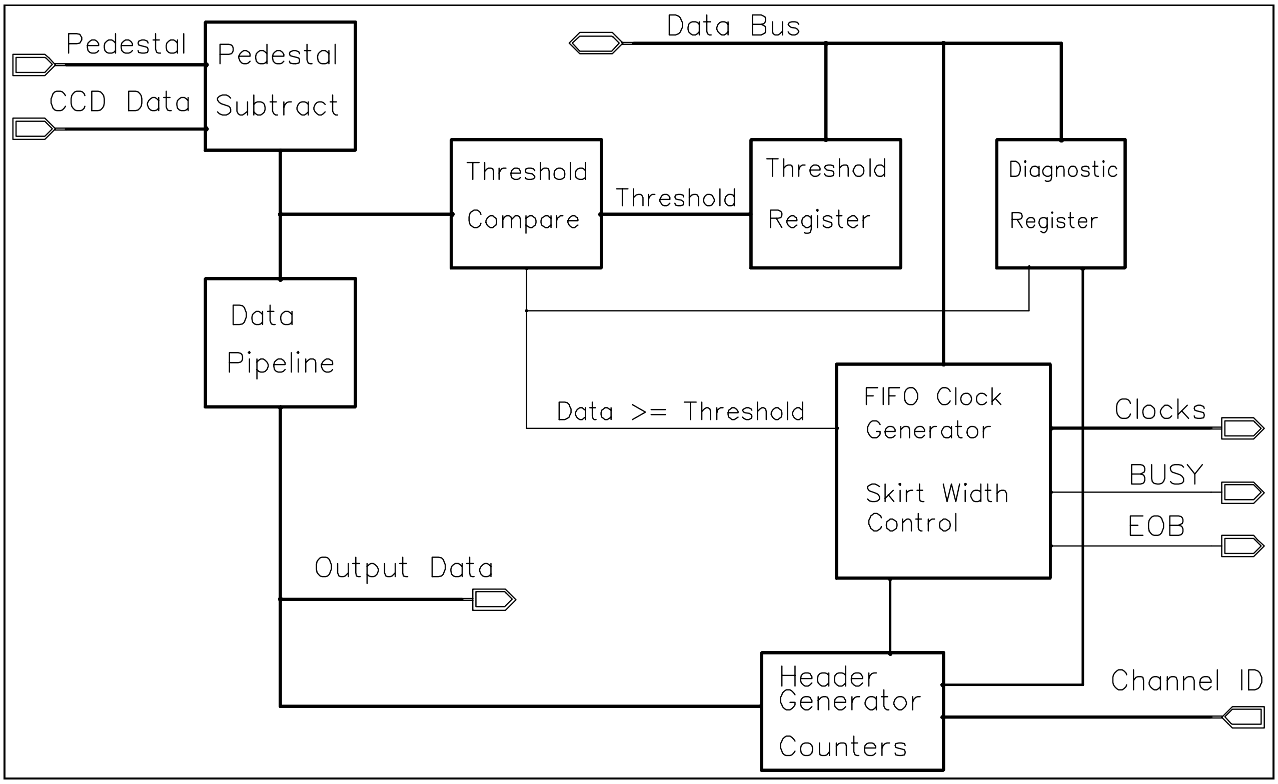


Figure 11: Diagram of the data compactor gate array.

words in the external data FIFOs. The passing of data to the output is also controlled by the Skirt Width logic (see below). The Header Generator inserts pixel and address counts into the output data stream to preserve the timing information. A diagnostic register provides access to internal data paths. This is used for testing the array during manufacture.

## 4.4 DCM Operation

### 4.4.1 Pedestal

The output from a CCD module with no input signal is composed of a DC offset with a possible slope. A Pedestal FIFO is provided on the DCM daughter-board which may be loaded with a unique pedestal value for each CCD pixel. The pedestal data may be obtained by averaging many data sets taken with no input signal.

Figure 12 shows a typical scintillator pulse after digitization. The top plot shows a portion of the raw digital data from the CCD board. The second shows the corresponding CCD pedestal data, and the bottom plot shows the resulting corrected data. The output data are not allowed to go negative for input data that are below pedestal.

### 4.4.2 Skirt and Minimum Pulse Width

Minimum Pulse Width (MPW) control allows for suppression of very narrow pulses, while the Skirt register controls how many data pixels are saved before and after the pulse crosses threshold. Skirt width may vary from zero to three pixels. The MPW value may be from 0 to 3, corresponding to a minimum pulse width of one to four pixels. Figure 13 shows the effect of these controls on the output data; the histograms are reconstructed from the compacted

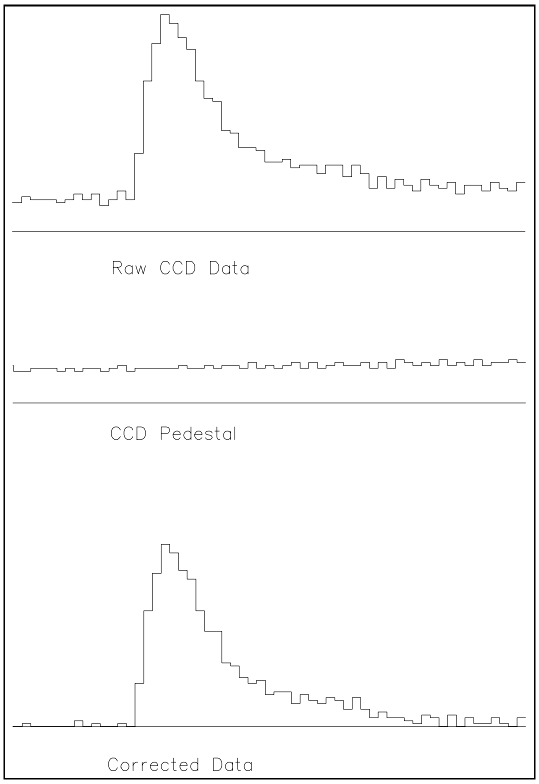


Figure 12: Typical input pulse (top), ccd pedestal (middle) and corrected pulse (bottom).

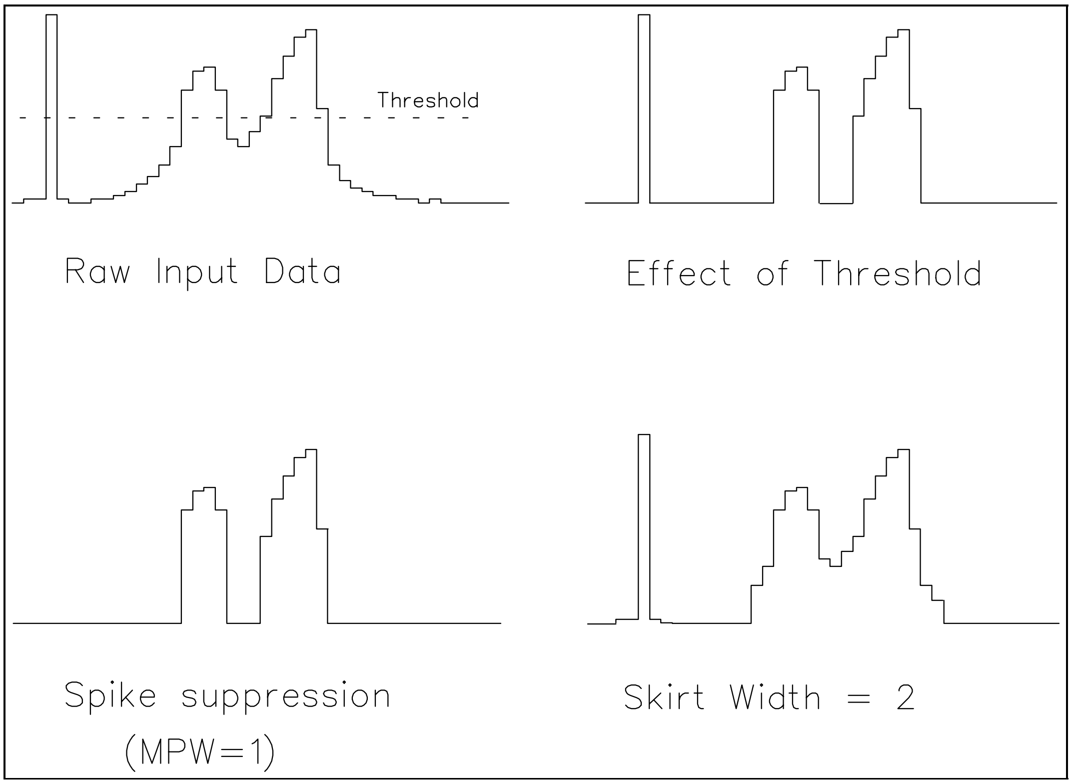


Figure 13: Effect of skirt and minimum pulse width (MPW) registers.

data with zeros inserted where data has been suppressed.

### 4.4.3 Control Register

A control register provides bits associated with the following functions: Disable Pedestal, Disable Threshold, Test Mode, Enable Empty Channel and Channel Disable. The Disable Pedestal and Disable Threshold bits would typically be used to obtain raw data sets from which pedestal values could be calculated. Channel Disable allows a channel to be turned off. Enable Empty Channel creates a channel header even if there are no data in that channel. Test Mode is used for online testing of the module.

### 4.4.4 Data Encoding

Clusters of 8-bit input data, which may represent one or more physical pulses depending on the settings of threshold and skirt width, are passed to a 32-bit output buffer. Each cluster is followed by a 2-byte cluster header, comprised of the pixel address and cluster length. Following the last cluster header, a 4-byte channel header is generated. This contains a word count, cluster count, status and channel ID.

Zeroes are inserted after the last cluster header in order to word-align the channel header. The output data are read via FASTBUS as 32-bit words. Data for all 16 channels may be read with one block transfer operation.

### 4.4.5 Testing

The gate arrays were tested after manufacture using 7000 test vectors generated during design simulation. Each daughter board was tested during production using a PC-based test station. Complete modules are tested using FASTBUS software.[12]

The gate array incorporates a 'test mode' where synthetic input data may be written to each channel via FASTBUS. Using this feature, the complete data path with the exception of the ECL receivers may be tested.

Selected modules have been fitted with a Test Data Generator which enables the injection of synthetic data at the front panel inputs at the full data rate. This method is used for initial testing, and may be used after installation if the input cables are removed.

# 5 CCD digitizers in E787

## 5.1 Application

E787 has used the CCDs initially in two of the detector subsystems, the pure CsI crystal endcaps and the scintillating-fiber target. In each system the signals pass through a network of passive splitters and amplifiers before being sent to the CCDs.

The main function of the CsI endcaps is to veto events in which extra energy is detected in coincidence with a $K^+ \rightarrow \pi^+\nu\overline{\nu}$ candidate event; the signals are produced with a wide range of energy deposits from about 0.5 to 100 MeV. In order to cover this range with at least 6-bit accuracy the charge from the detector element signals is split asymmetrically to provide "high-gain" and "low-gain" inputs. High gain single-crystal inputs ($E < 25$ MeV) occupied 143 CCD digitizer channels and "low-gain" channels containing the sum of signals from four crystals ($E < 80$ MeV) occupied 36 channels.

The target signals are due to kaons coming to rest along the fiber axis depositing up to 80 MeV and to minimum ionizing decay particles which give about 1 MeV when traversing a fiber perpendicular to the axis. The fibers hit in an event can be divided into two categories, "kaon" fibers with large energy deposits at early times, and "pion" fibers with small energy deposits at later times. Figure 14 shows the pattern of hits observed for a typical K decay event in the target. The correct determination of the trajectories of the kaon and pion depends on determining the time and energy of each hit in an event.

The target CCD system was comprised of 512 channels; 413 "high-gain" single-fiber channels ($E < 8$ MeV) and 84 "low-gain" ($E < 80$ MeV) channels with summed inputs from groups of three to six fibers.

## 5.2 Data Processing

The nonlinear response of the CCD digitizers (see fig. 6) required that a linearity correction be applied to the data. Correction functions were obtained off-line for each channel by measuring average CCD pulse heights as a function of input signals of known voltage. The calibrated data were scanned for the presence of pulses defined as a continuous set of at least 4 pixels with at least 5 counts in each. The parameters of the pulses which were determined are the leading edge time (taken at 40% of maximum pulse height), the maximum height, the area, the full width (i.e. total time above threshold), the width at 1/2 maximum height (FWHM) and the rise time (defined as the difference in leading edge times taken at 20% and 60% of the maximum pulse height). In addition, status bits were set for each pulse to indicate various conditions, such as overflow, or if the pulse was above threshold at the start and/or end of the CCD digitizer time range. Another pulse-finding routine

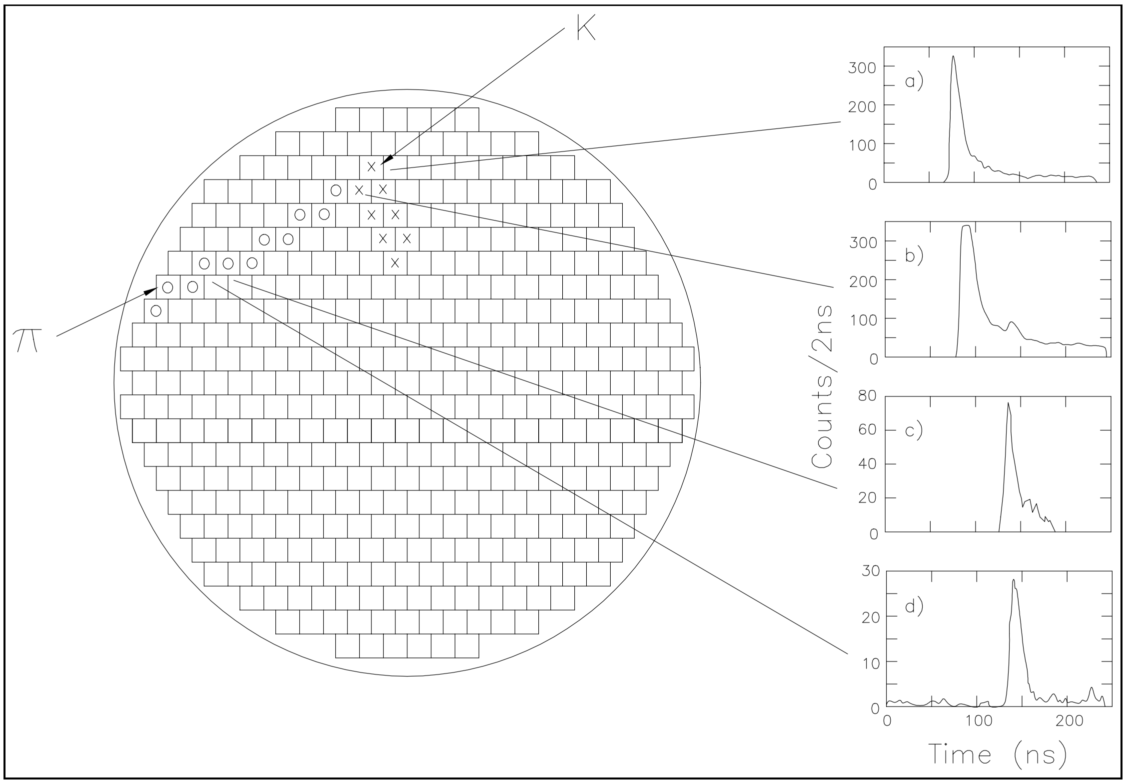


Figure 14: An example of CCD digitizer readout of a $K^+ \to \pi^+$ decay event in the scintillating fiber target. The elements indicated with an X were hit by the incident K traveling along the fiber axis (into the page) and those with an O were subsequently hit by the decay particle. Insets a) and b) show the CCD digitizer output vs. time for two elements hit by the K. Insets c) and d) show two elements hit by the decay product $\pi$. The delayed $\pi$ pulse is also evident in b). Note that the vertical scale is adjusted for each graph.

was used to detect secondary ("pile-up") pulses which may have occurred on the tail of the original pulse.

## 5.3 Performance

### 5.3.1 Timing Resolution

Potential contributions to the timing resolution include the intrinsic resolution of the detector and electronics upstream of the digitizers, jitter in the reference timing signals, errors extracting the pulse times from the data and the intrinsic resolution of the digitizers. To examine the functioning of the CCD digitizers, a signal was split and then recombined with one path delayed by a fixed amount. A measurement of the variance (RMS) of the difference in leading edge times between the delayed and non-delayed signals provides a useful indication of the intrinsic resolution. The channel-to-channel jitter was determined by putting the split signals into different digitizer channels. These tests, performed using pulses from the scintillating-fiber target, resulted in typical RMS variation of 100 ps; this represents a small contribution to the overall timing variations from the detectors themselves, typically 300 ps (RMS) obtained under experimental conditions. The overall timing resolution for CsI endcap pulses of $\geq 5$ MeV was found to be about 650 ps.

### 5.3.2 Double Pulse Resolution

In addition to good timing resolution, an important function of the CCD digitizers is to resolve multiple pulses. Figure 15 shows an example of two pulses piled-up in a CsI crystal; the K decay event occurred at time 0 ns where a small pulse is seen riding on the tail of the larger pulse which appeared 70 ns earlier. For the CsI crystals, the minimum separation of resolved pulses was

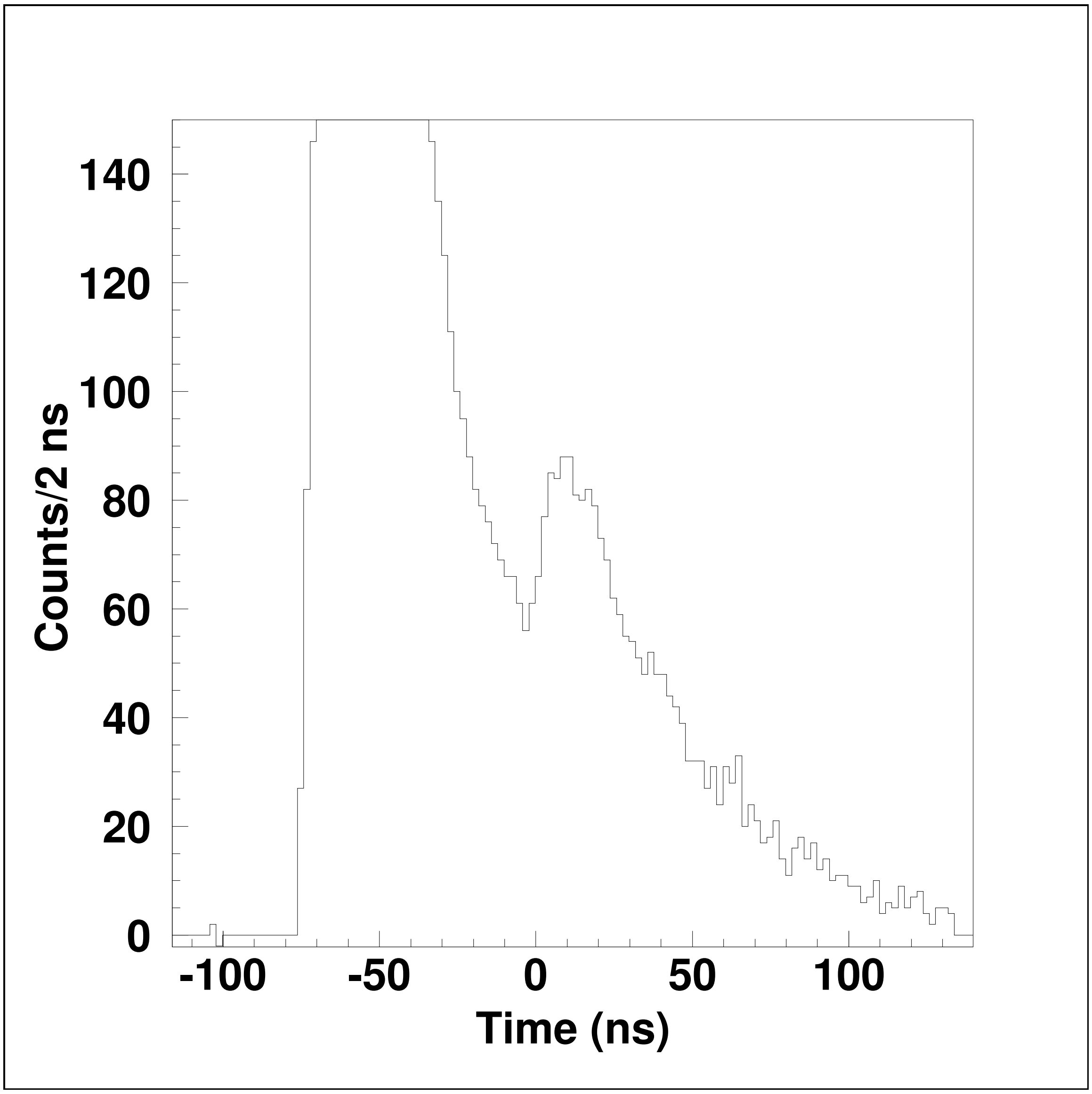


Figure 15: CCD digitizer readout of a "pile-up" event in a CsI crystal.

found to be about 20 ns. For the faster signals from the plastic scintillator fibers, second pulses can be resolved as soon as about 5 ns after the initial pulse. The actual minimum separation of resolved pulses depends on the relative sizes of the two pulses.

## 6 Conclusion

A system of 500 MHz GaAs CCD digitizers with 8-bit dynamic range has been constructed and operated in experiment E787 at BNL. The initial implementation used about 700 channels of digitizers with memory of 128 pixels covering 256 ns. More recently, CCDs with 320 pixels have been manufactured and installed extending the digitizer memory time to 512 ns.[2] Future development could lead to CCD digitizers with sampling speeds exceeding 1 GHz and memory lengths of several $\mu s$. In addition, the GaAs CCD technology developed could be applied to produce ultra-high speed, radiation hard detectors.

## 7 Acknowledgments

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[2] 256 pixels is the current limitation of the data compactor modules (DCM).

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# 8 Appendix A

## 8.1 Master Trigger

### 8.1.1 Overview

The overall function of the Master Trigger (MT) is to generate clocks and strobes for the CCD modules and the Data Compactor modules (DCM). The MT module is a FASTBUS compatible card which provides a mounting platform for two daughter cards, the MT daughter card (MTD) and the Slave Trigger (ST). The mother board also provides the interface to the power systems and the cabling and connector interfaces to other modules. The MTD card uses surface-mount 300 series ECL devices. Control strobes to the CCD modules and the data compactor are distributed using differential ECL drivers and receivers. Most aspects of the clock generation and distribution use GaAs logic which is compatible with ECL logic levels. The Clock signal delivered to the CCD modules with a 50 $\Omega$ coaxial connection has a swing from 0 to -2.5 V. The MT has a 2-unit wide front panel.

### 8.1.2 Operation

The MT receives a stable high frequency (500 MHz) clock signal from the synthesizer (see fig. 7) where it is used to generate a lower frequency clock signal.[3] These two frequencies are combined into one clock signal which is then sent to the ST card which provides an eight-way fan out[4] of the clock signal. These clock signals are connected to the CCD modules to provide the

[3]The low frequency, normally 15.625 MHz, is selectable in factors of two from 0.488 MHz to 31.25 MHz–assuming a 500 MHz high frequency input.

[4]As discussed in the Appendix B, a sixteen way fan out is provided although only an eight way fan out is required for the MT.

HI/LOW frequency clocks to the CCD cards.

During normal operation, a multiplexer on the MT module directs the high frequency clock to the CCD modules. While the CCD system is in this "acquisition" mode, most sections of the MT card are inactive.

When a trigger signal (level 0) is received, the MT initiates the sequencing of clock, strobe and envelope signals for a low frequency readout cycle. Internal strobes lock out any subsequent trigger signals during the readout cycle and reset the low frequency clock generation circuits allowing the low frequency clock and the strobes to start from a known state. In addition, the multiplexer on the MT module directs the low frequency clock to the CCD modules ( although there is effectively no clock sent to the CCD modules during the initialization since the low frequency is in a reset state). Further initialization of the internal flip flops and counters in preparation for the readout cycle also occurs.

After the initialization period, the low frequency clock generation circuits initiate sending of the low frequency clock to the CCD modules, sending of the CCD data conversion strobes (gated by an envelope which was previously initialized) to the FADC, sending of the compactor strobe to the DCM and, after a predetermined count,[5] switching a data compactor envelope to the true state indicating that valid CCD data is present.

When the MT is in the midst of a readout cycle the low frequency clock and the strobes continue until the counters have counted out the required number of cycles to read out all CCD pixels. Then, the multiplexer switches off the low frequency and switches on the high frequency clock to the CCD

[5]This delay in starting the envelope allows for the delay between conversion of the analog signal and output latching of the digital data at the CCD card.

modules. In addition, the envelope gating the CCD data conversion strobes terminates, stopping the delivery of strobes to the CCD. The low frequency clock and the strobe generator continue to operate for another 256 low frequency clock cycles allowing the data compactor control strobe to continue. These extra strobes are required for internal DCM operations.

The DCM envelope ends after 256 data compactor strobes have been counted. Once the system has completed the second group of 256 clock cycles, most sections of the MT return to an inactive state. At this time the MT will be ready to accept another level 0 trigger.

If the MT receives an "ABORT" signal, the readout cycle is terminated. In this case, the multiplexer switches off the low frequency and switches on the high frequency clock to the CCD modules and the strobe generator stops (along with the envelopes gating the CCD data conversion strobes and the data compactor envelope). At the end of the "ABORT" signal, a single strobe is generated to reset the DCM. At this time the MT will be ready to accept another level 0 trigger.

# 9 Appendix B

## 9.1 CCD Mother Card

The CCD mother card (MC) is a FASTBUS compatible card which provides a mounting platform for 16 CCD daughter cards as well as one ST. The mother board also provides the interface to the power systems (through the multi-plane circuit board) and cabling and connector interfaces to and from the CCD cards. The module has a 3-unit wide front panel.

## 9.2 Slave Trigger

The Slave Trigger (ST) accepts and delivers various signals (using 50 $\Omega$ coaxial cables and SMB fittings) and performs several functions. The hi/low clock from the MT is passed to the Slave Trigger input and 16 clock outputs (replicated by the RF fanout) are passed to the CCD cards by cable assemblies. The (differential) ECL strobes from the MT are passed to the ST by a cable assembly mounted on the mother card and by surface circuit traces. 16 (differential) ECL control strobe outputs (replicated by the ECL fanout) are sent to the CCD cards by other cable assemblies.

## 9.3 CCD Card Inputs and Outputs

16 analog signals are sent to the CCDs by a cable assembly mounted on the front panel of the mother card. In addition, the front panel holds 16 analog monitor outputs. The (differential) ECL digital data outputs are passed to the front of the mother card using ribbon cable assemblies. Two potentiometers per channel are mounted on the mother card at the front panel. These provide voltage control of the CCD input bias and offset control of the FADC input signal (prior to digitizing). This bank of 32 potentiometers is powered by a voltage regulator mounted on the mother card.

The CCD card has a simple connector through which the power supplies and the control strobes are delivered.

## 9.4 System Power Requirements

The transient digitizer system uses standard FASTBUS supplies, although the actual output voltages are set about 0.1 V higher than normal to overcome voltage drops across the internal module fuses.

Three 200 A switching supplies are used with each crate to provide 5.0 V ($V_{cc}$), -2.0 V ($V_{tt}$)and -5.2 V ($V_{ee}$). The $\pm$15 V is supplied to each crate by a linear power supply.

Additional voltages are generated as required. 12 V for the CCD daughter cards is generated from the 15 V line using an adjustable IC regulator. Similarly, -3.3 V for the front panel potentiometers is obtained from the -5.2 V line and Zener diodes with an operational amplifier-transistor buffer circuit are used to get -3.4 V for the GaAs logic devices on the MT.