Electrical/Optical Issues in I/O CMOS Interfaces

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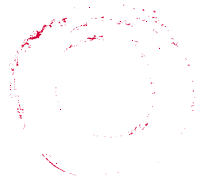
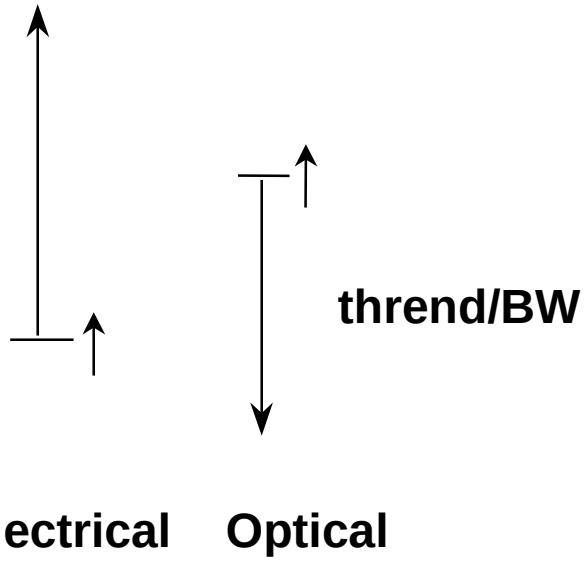


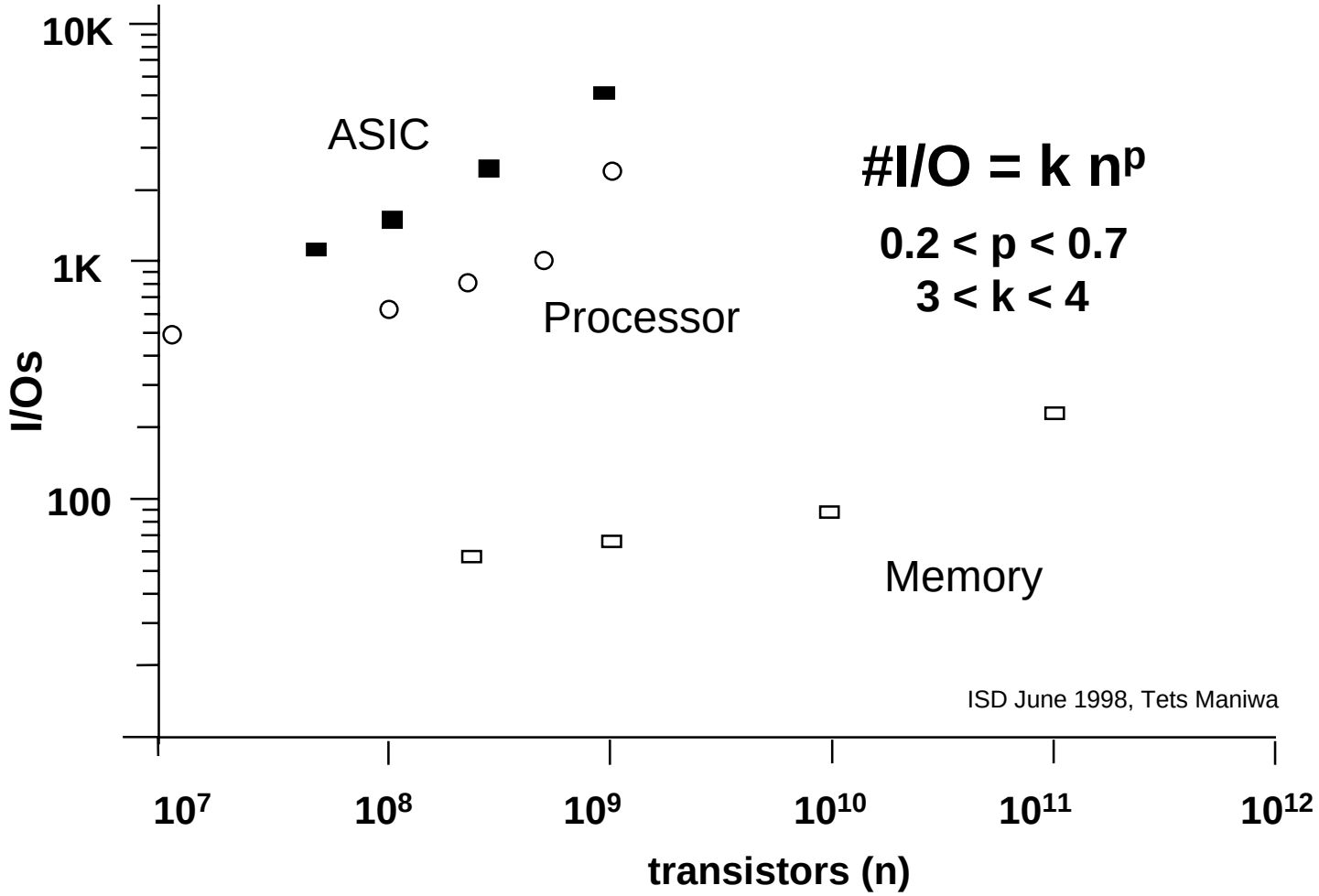
Lucent Technologies
Bell Labs Innovations

Electrical vs. Optical

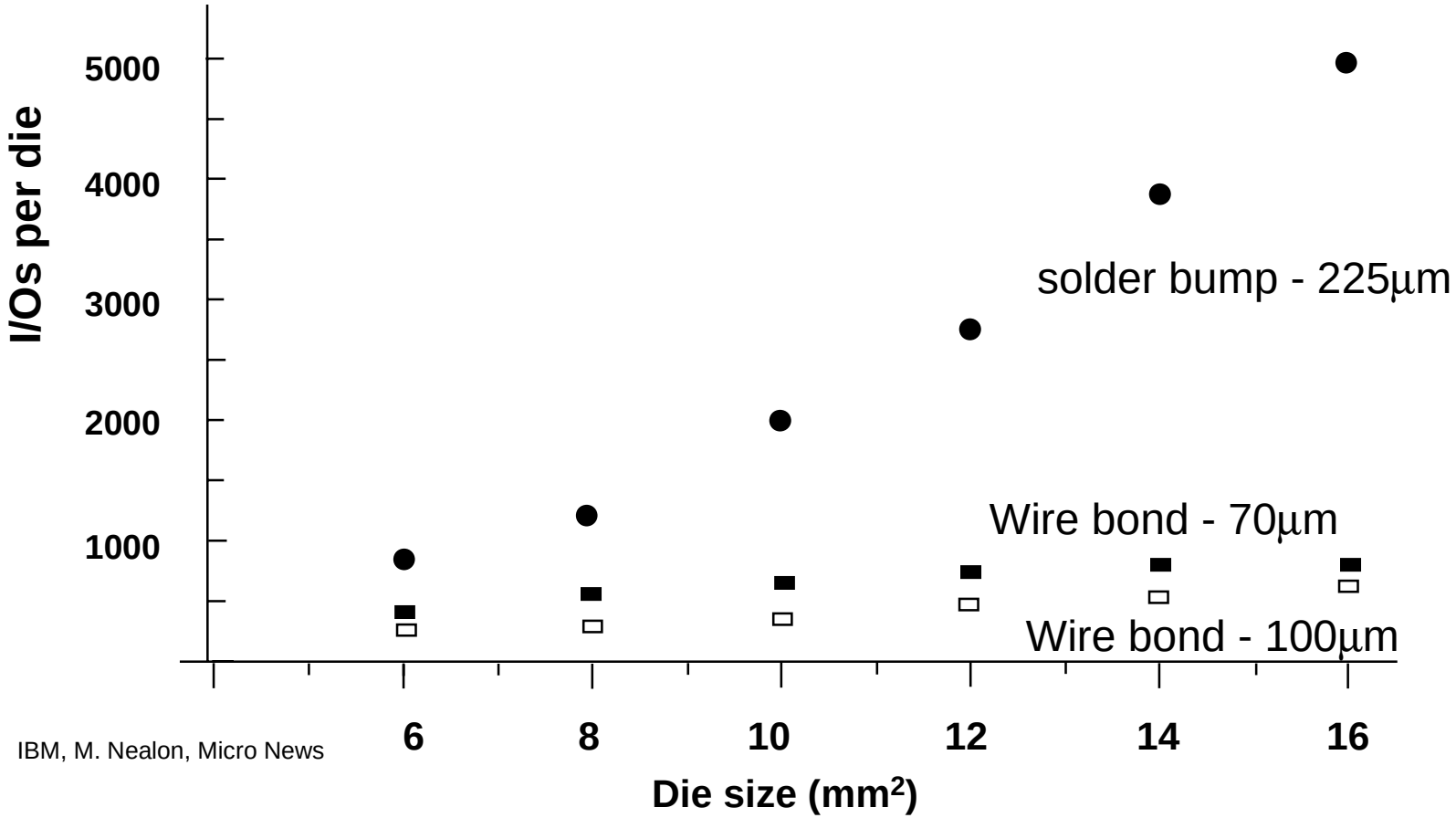
- **Interconnect length is a limiting aspect**
  - **on-chip**
  - **between chips**
  - **between boards**
  - **between cabinets**
  - **between buildings**
  - **cities and countries**



Rent's Rule

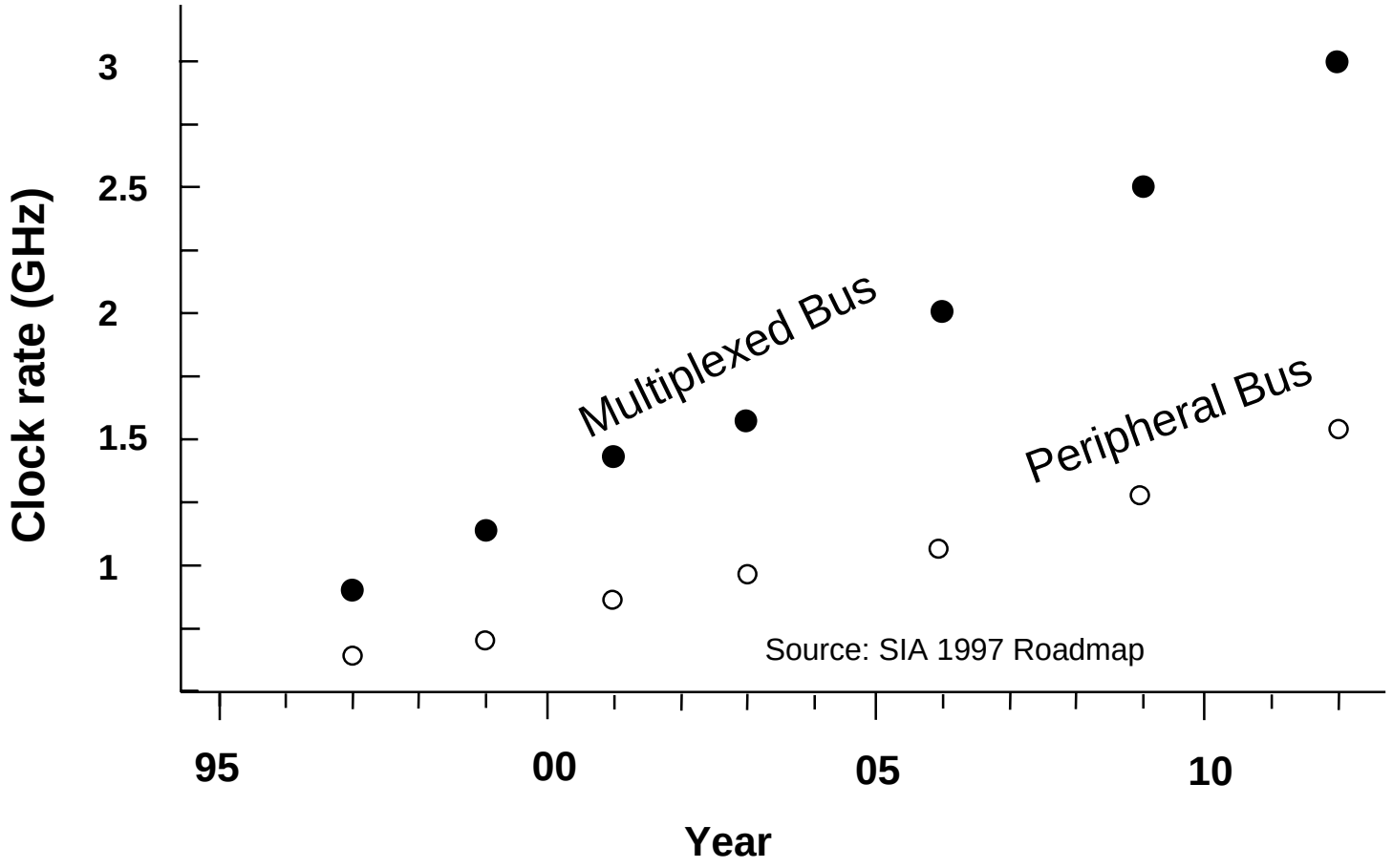

10K
1K
100
I/Os
ASIC
Processor
Memory
#I/O = k n^p
0.2 < p < 0.7
3 < k < 4
ISD June 1998, Tets Maniwa
10^7
10^8
10^9
10^10
10^11
10^12
transistors (n)

Chip Interconnect Density



IBM, M. Nealon, Micro News

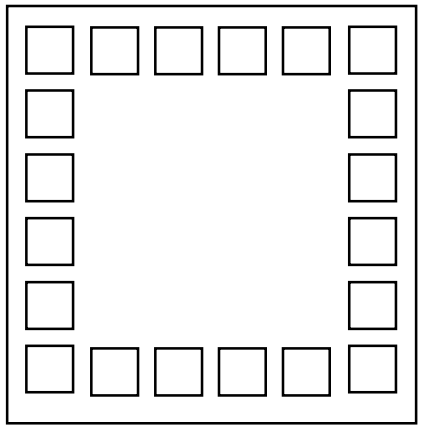
Chip to Board Clock Rate



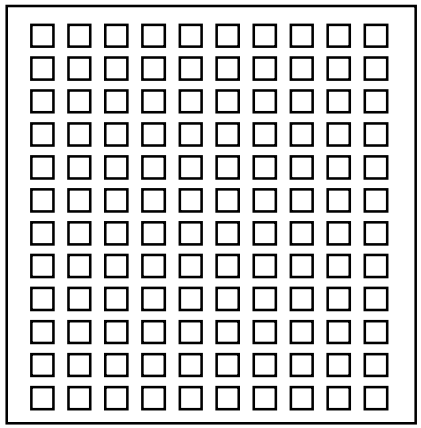
I/O Impact of Scaling CMOS

- **Density in core is increasing**
- **Allows more data to be processed**
- **Need to keep up information transfer to/from core**
- **I/O transfer rates increasing**
- **Rent's rule forces high pin count**

Chip I/O Limitation



Wire bond

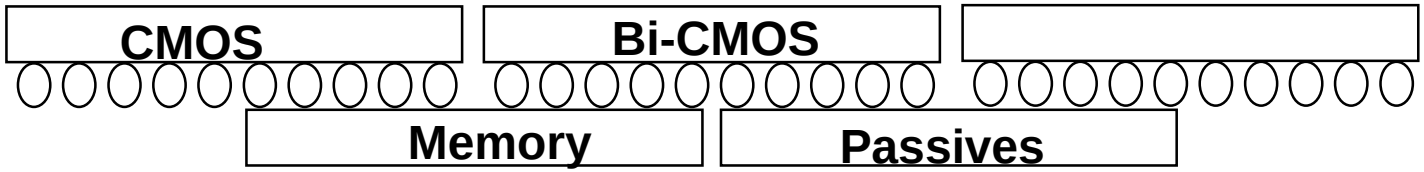


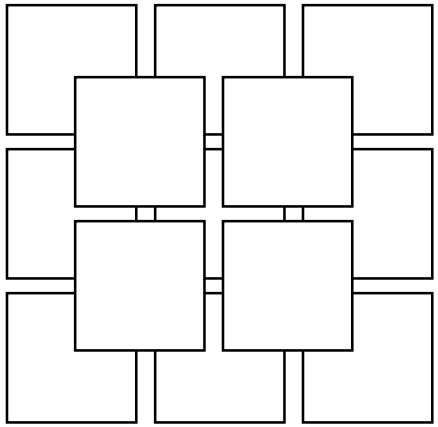
Solder bump

- **Solder bump**

  Process and packaging step differences
  CAD tools for chip partitioning
  Offers new potentials for system growth
  Allows for optimized process attachment

Solder Bump System Possibilities

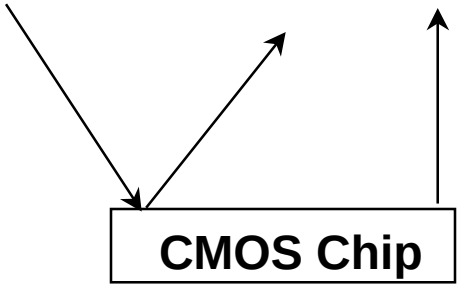


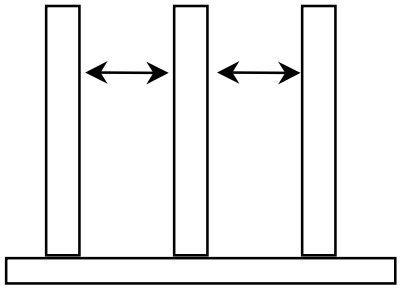


- **Shingling die**
  Combine different optimized die together
  Allows formation of compact systems

Optical Chip Communication

- **Process added step to CMOS**
- **SEED, VCSEL needs to cost compete with solder bump**
- **May offer backplane benefits**
- **Current High BW interfaces may benefit**
  - **CPU-memory**
  - **Switching networks**

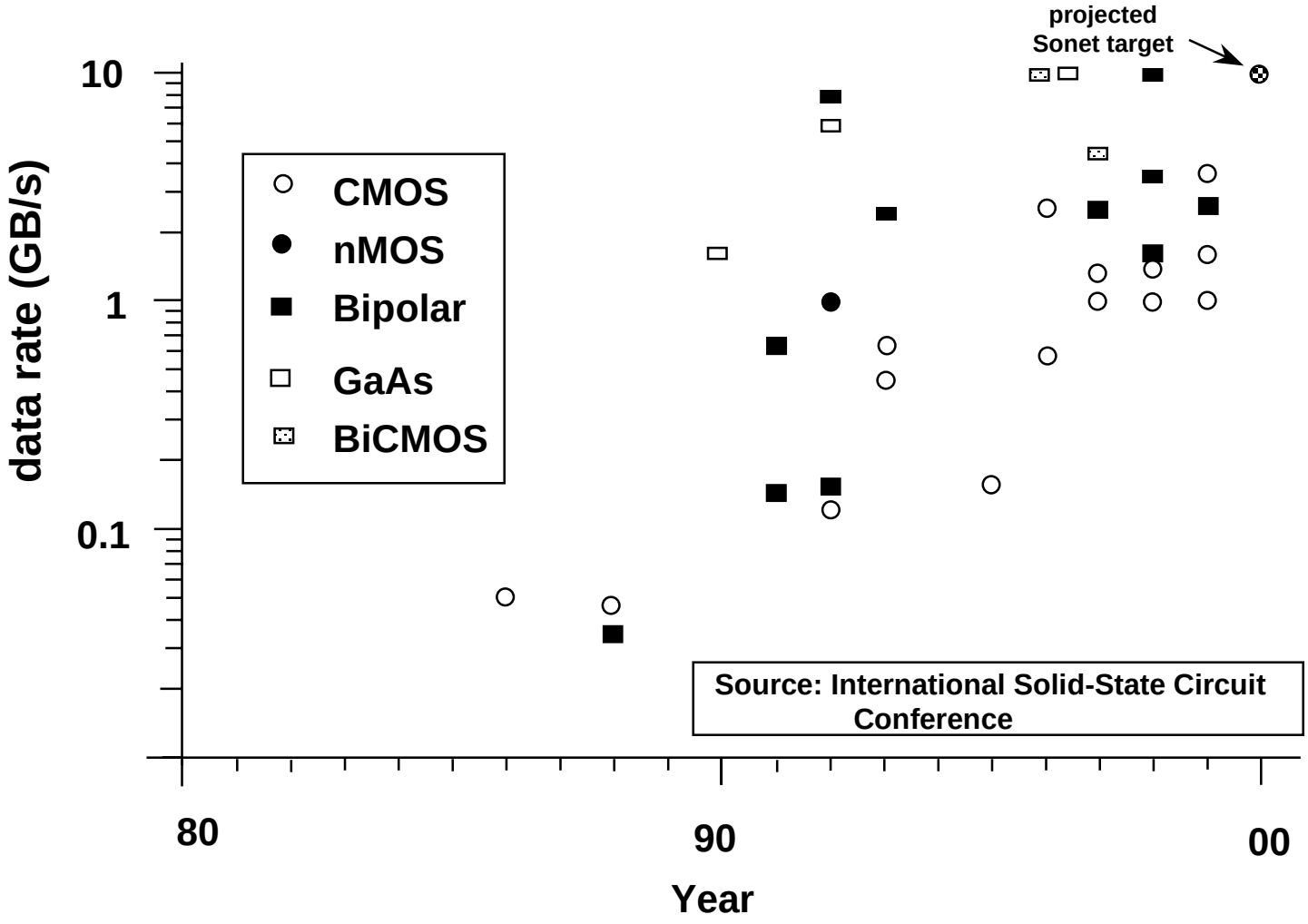




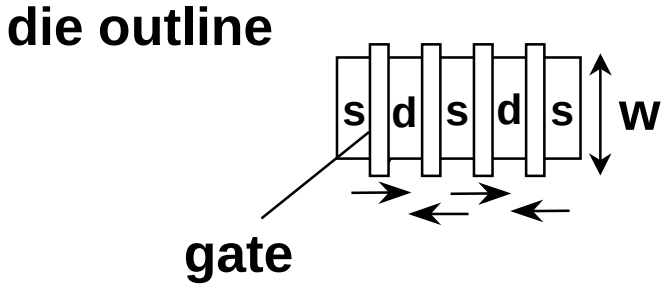
CDR Background

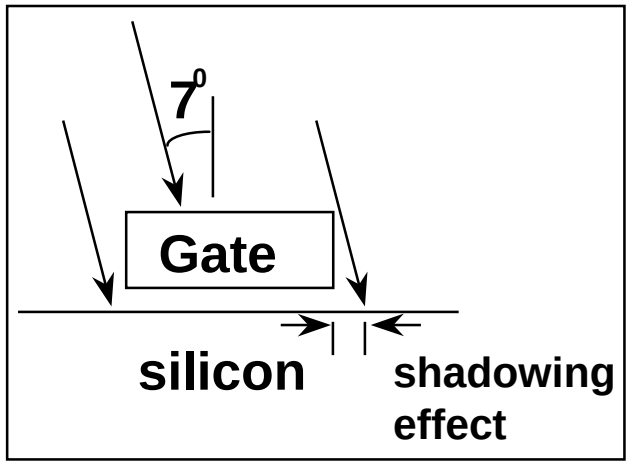
- single interconnect
  - coding schemes
  - contains both clock and data
  - bandwidth efficient connection
- at destination
  - perform post-processing to extract clock from data
- synchronize data at destination
  - using recovered clock

Clock and Data Recovery Performance Trend

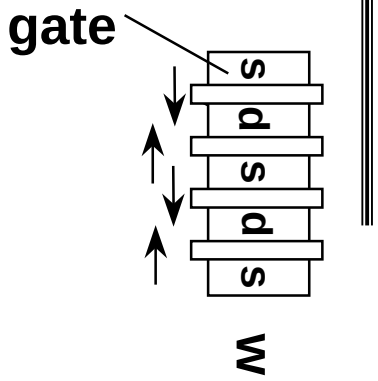


Shadowing





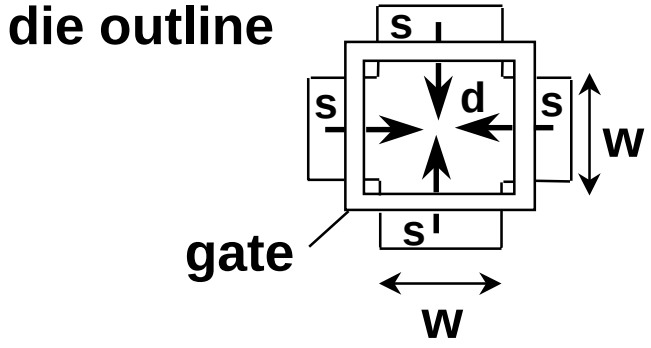
- Digital ASIC technique
- Use same layout around the frame
- Typically use a linear layout
- Small swing buffers are a problem

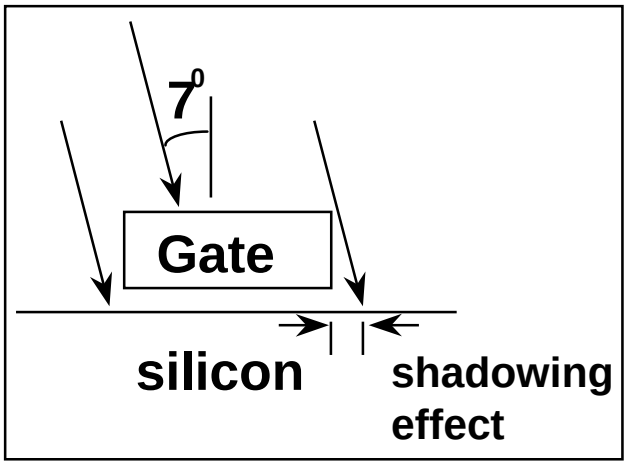


Measured Data of V_{ol} of 800mV swing(over several lots)

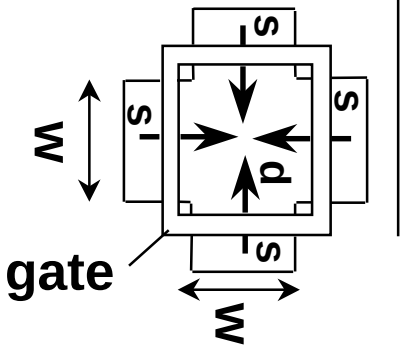
	Avg ΔV	σ
linear	136mV	31.6mV

Rotational Symmetry





- Current matches
- Gate segments match

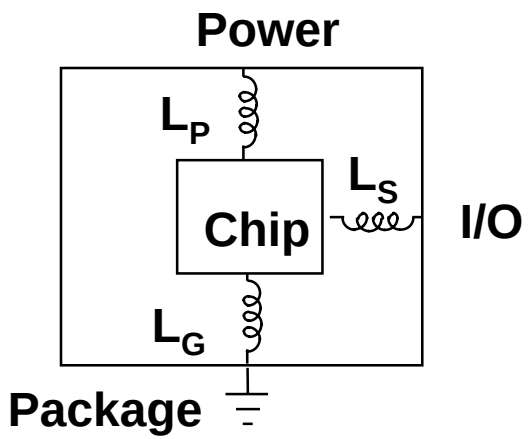


Measured Data of V_{ol} of 800mV swing(over several lots)

	Avg ΔV	σ
linear	136mV	31.6mV
Rot Sym	30mV	8.9mV

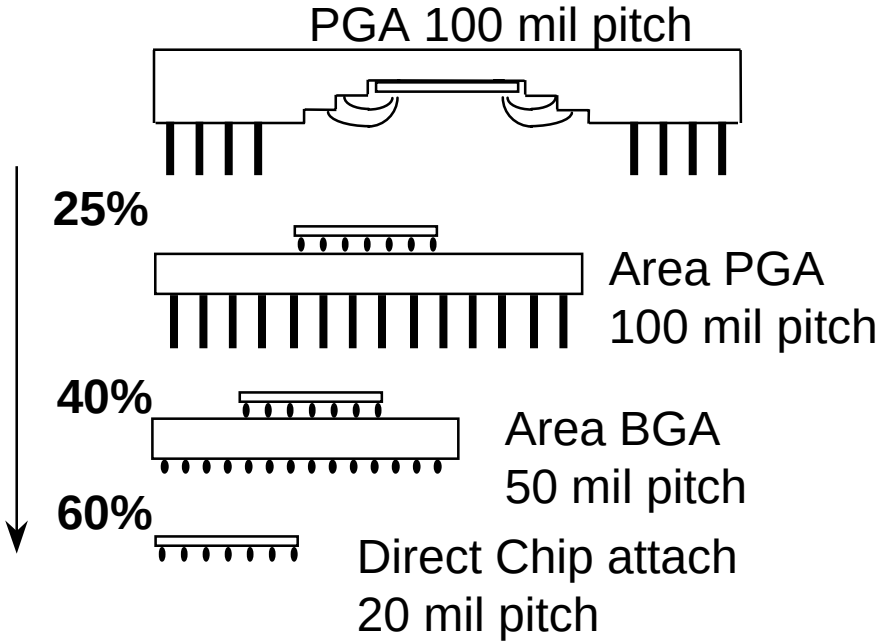
Packaging

- **Need to get power/ground to the chip**



I/O

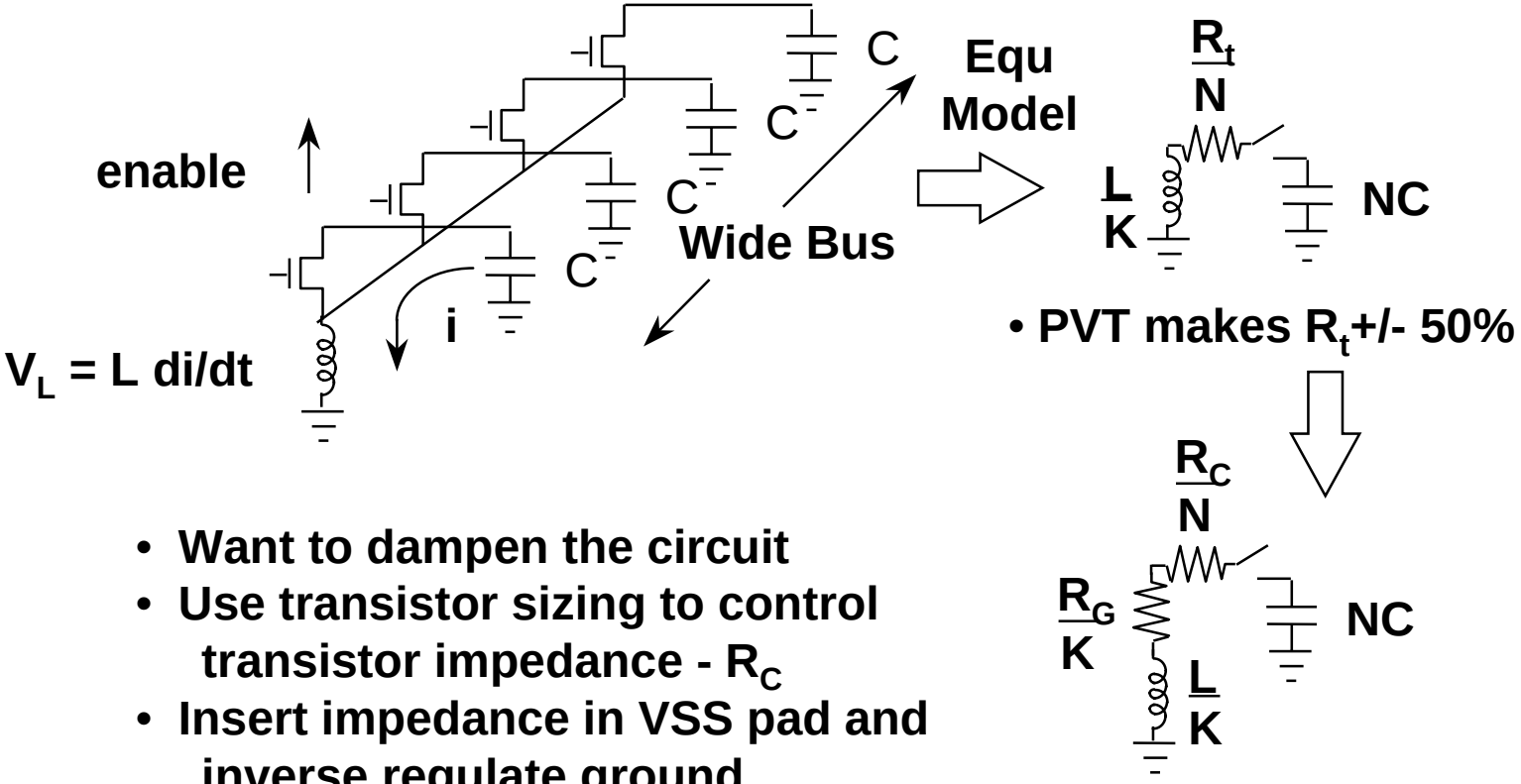
V_L = L di/dt introduces Ground Bounce



IBM, M. Nealon, Micro News

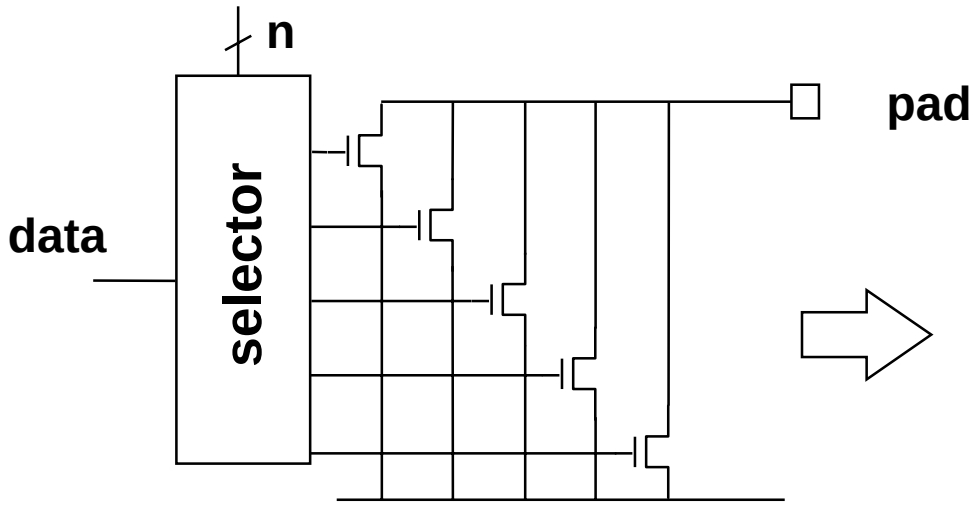
Package size reduction achieves:
Lower L ; smaller board area.

Ground Bounce Reduction



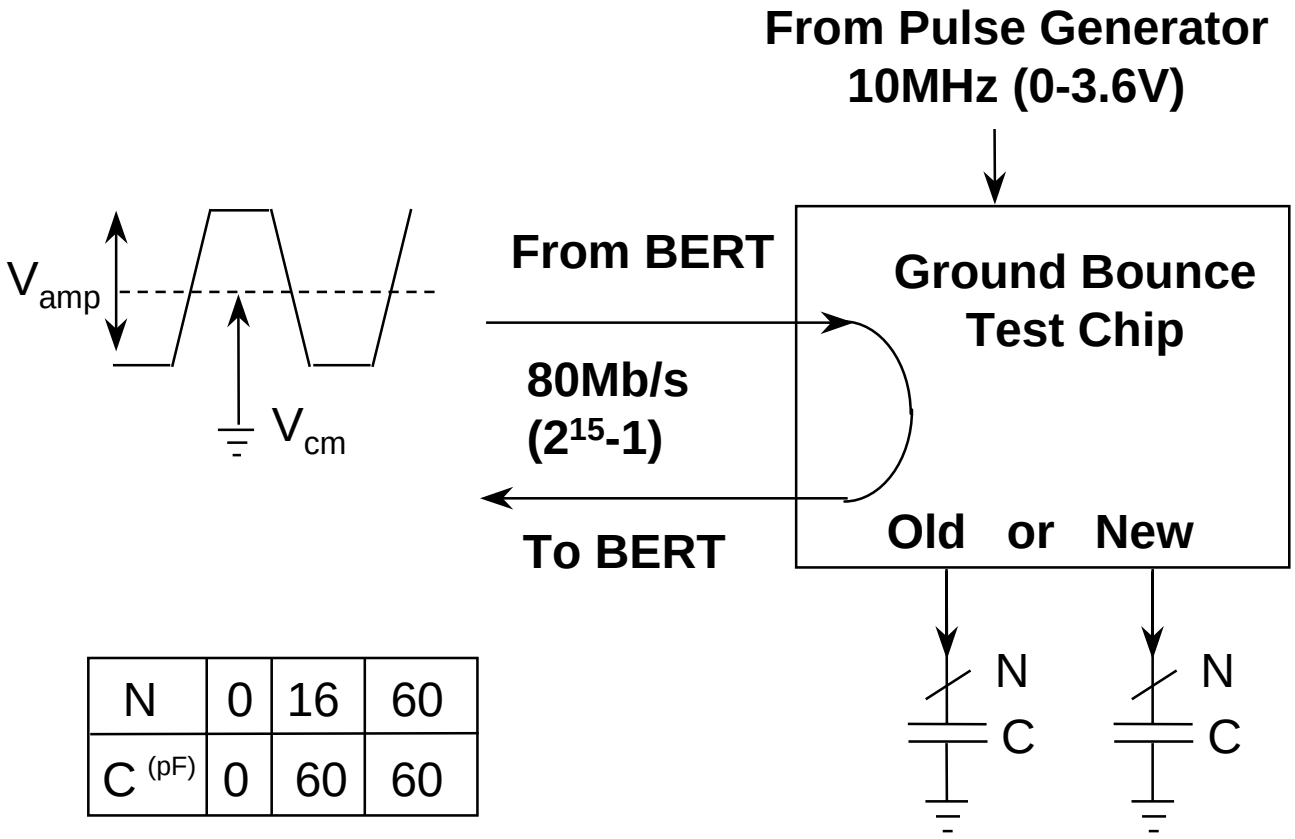
- Want to dampen the circuit
- Use transistor sizing to control transistor impedance - R_C
- Insert impedance in VSS pad and inverse regulate ground impedance - R_G

Digital Transistor Sizing



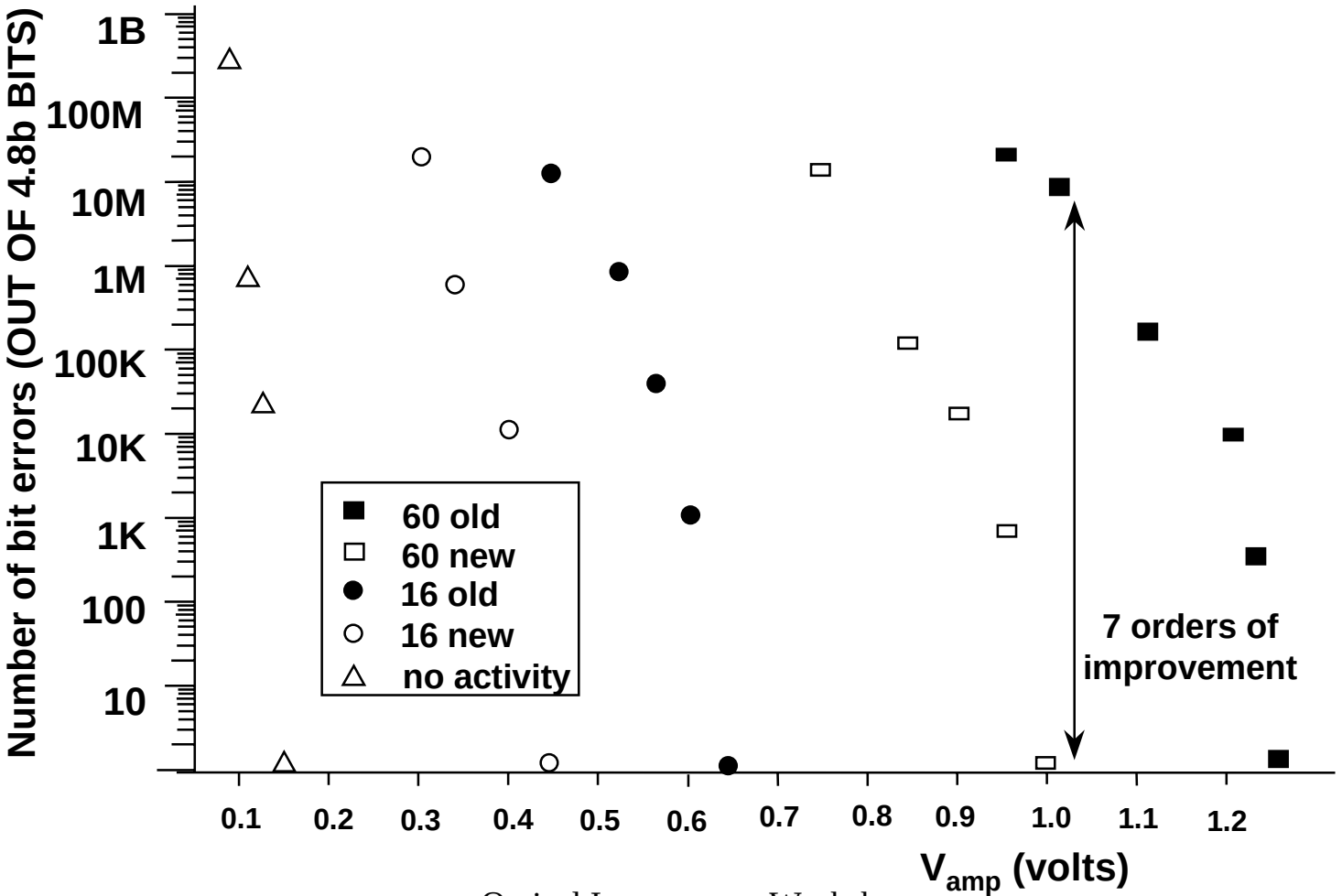
- **Technique used over 2Gb/s**
- **Data path segregated from control**
- **Selector allows dynamic transistor sizing**
- **PVT (Process, Voltage, Temp) compensated (R and I)**
- **Controls impedance, performance, power, etc.**
- **Used in Ground Bounce buffers, HSTL and other buffers**

Test Setup to Measure Bit Errors

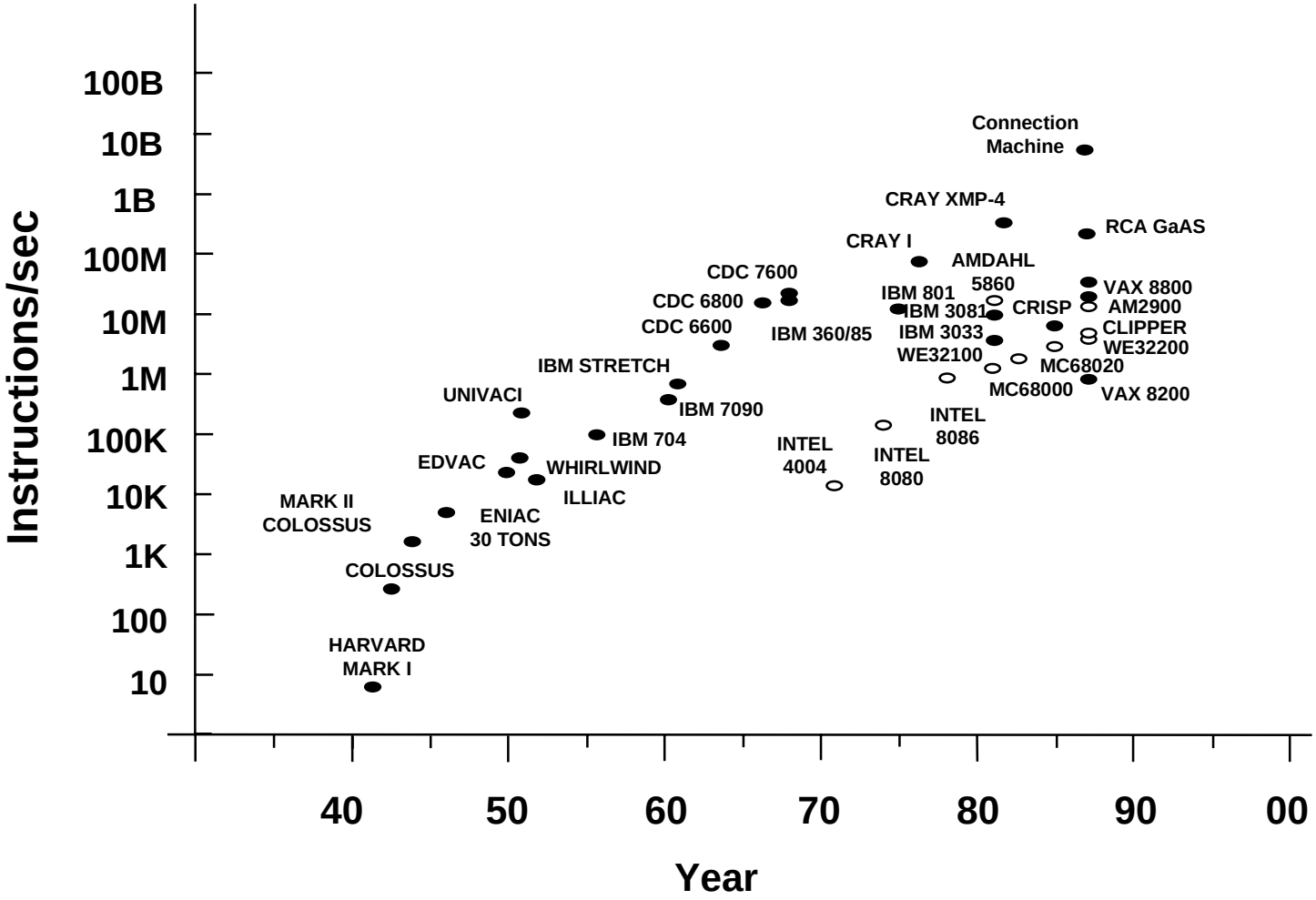


N	0	16	60
C (pF)	0	60	60

Bit Errors Generated

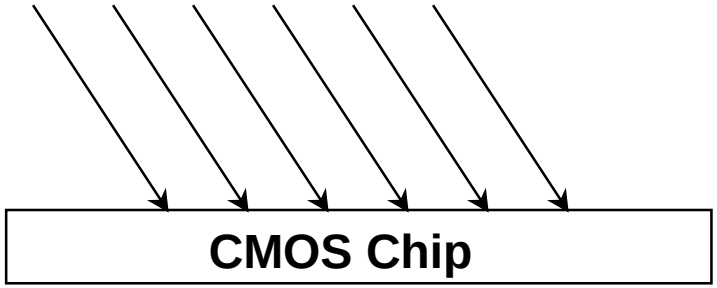


Computer/μProcessor Trends



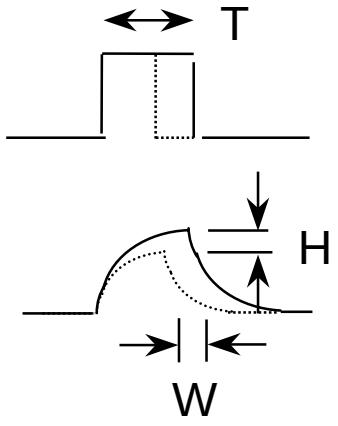
Optical Chip Clocking

- **Process added step to CMOS - maybe?**
- **Reduces skew**
- **Easier to synchronize chip**

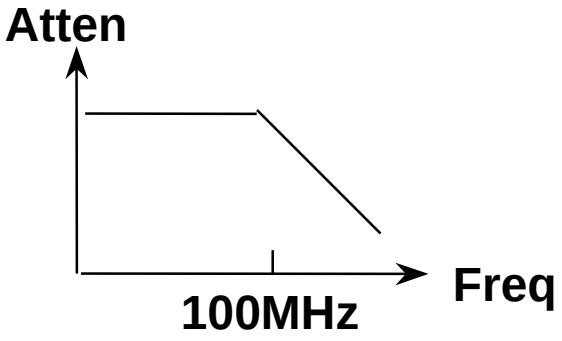


Skin Effect

- **Skin effect** $\delta = (\pi f \mu \sigma)^{-0.5}$
- **Affects the cross-sectional area**
- **The high-frequency components become more attenuated**
- **This causes "pattern dependent" effects which is know as intersysmbol interference**



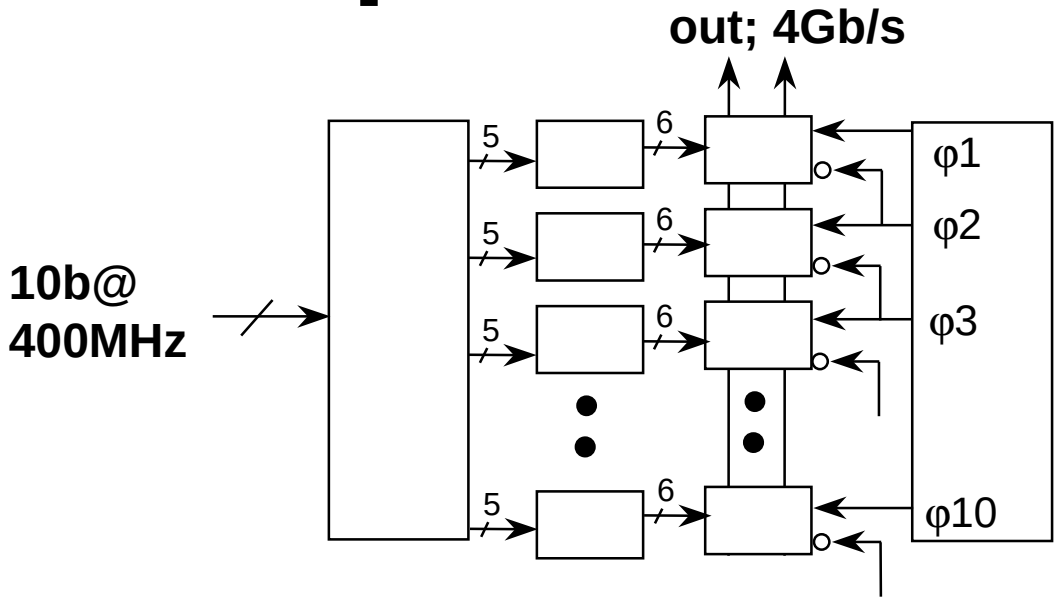
Below some T, the eye diagram of the data degrades in W and H



Optical Communication

- **Skin effect doesn’t occur**
- **Attenuation - 0.2db/km?**
- **Electrical attenuation -5db at a few GHz**
- **Electrical intersysmbol interference gone**
- **This is nice**
- **Circuits and techniques push the envelope**
- **ULSI gives transistors to use for I/O**

Equalization



- Pre-emphasizes signal to compensate for attenuation
- Gives flat attenuation response from 0.2 to 2GHz
- 4Gb/s over 100m

Conclusions

- **Reviewed the SIA roadmap for I/O**
- **I/O Impact of scaling CMOS**
- **Circuit and system techniques**
- **Skin effect**
- **Equalization**
- **CMOS circuit design, infrastructure, CAD tools, ULSI, all favor pushing existing limits**
- **Tends to delay optical entry at the lowest level**