Baseband section

This document provides a description of the baseband section of the MEGA3. Most design decisions are explained, but no detailed calculations are included. Total chip solutions(MT6228, MT6318, MT6120) except for RF Power Amplifier(RF3166) are from MediaTek, Taiwan.

I. MT6228 (GSM/GPRS Baseband Processor)

1. System OverView

The Revolutionary MT6228 is a leading edge single-Chip solution for GSM/GPRS mobile phones targeting the emerging applications in digital audio and video. Based on 32bit ARM7EJ-S^{TM} RISC processor, MT6228 not only features high performance GPRS Class 12 MODEM, but also provides comprehensive and advanced solutions for handheld multi-media. But, the MEGA3 can only support GPRS Class 8.

The Figure 1 is shown Typical Application for MT6228.

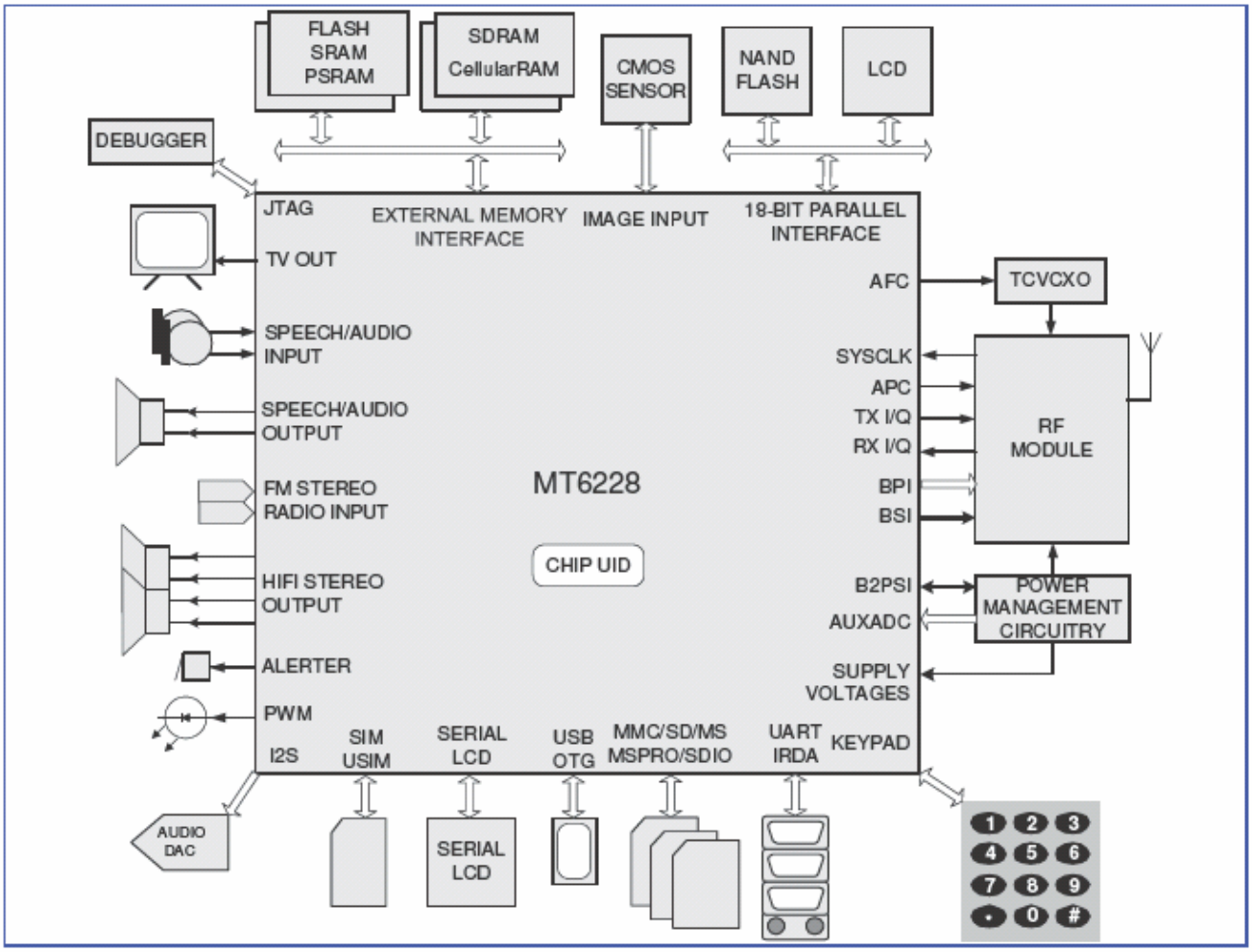


Figure 1 : Typical Application for MT6228

1.1 Platform Feature

- General

-. Integrated voice-band, audio-band and base-band analog front ends.

-. TFBGA 13mm x 13mm, 314balls, 0.65mm pitch package.

- MCU Subsystem

-. ARM7EJ-S 32bit RISC processor

-. High Performance Multi-layer AMBA bus

-. Java hardware acceleration for fast Java-based games and applets.

-.Operating frequency : 25/52/104Mhz

-. Dedicated DMA Bus

-. 14 DMA channels

-. 1M bits on-chip SRAM

-. 1M bits MCU dedicated Tightly Coupled memory

-. 256K bits CODE cache

-. 64K bits DATA cache

-. On-chip boot ROM for factory flash programming

-. Watchdog timer for system crash recovery

-. 3sets of General purpose timer

-. Circuit Switch Data coprocessor

-. Division coprocessor

-. PPP Framer coprocessor

- External Memory Interface

-. Supports up to 4 external devices

-. Supports 8-bit or 16-bit memory components with maximum size of up to 64M bytes each.

-. Supports Mobile RAM and Cellular RAM

-. Supports Flash and SRAM/PSRAM with page mode or burst mode

-. Industry standard Parallel LCD interface

-. Supports Multi-media companion chips with 8/16bits data width.

-. Flexible I/O voltage of 1.8V ~ 2.8V for memory interface.

- User Interface

-. 6-row x 7-column keypad controller with hardware scanner.

-. Supports multiple key presses for gaming.

-. SIM/USIM controller with hardware T=0/T=1 protocol control.

-. Real Time Clock(RTC) operating with a separate power supply.

-. General Purpose I/Os (GPIOs)

-. 2sets of Pulse Width Modulation(PWM) output.

-. Alerter Output with enhanced PWM or PDM.

-. 8 external interrupt lines.

- Security

-. Cipher : supports AES, DES/3DES

-. Hash : Supports MD5, SHA-1

-. Supports security key and 2kit chip unique ID

- Connectivity

-. 3 UARTs with hardware flow control and speed up to 921600pbs.

-. IrDA modulator/Demodulator with hardware framer. Supports SIR/MIR/FIR operating Speeds.

-. Full speed USB 1.1 OTG capability. Support Device mode, limited host mode and dual-role OTG mode.

-. Multi Media Card, Secure Digital Memory Card, Memory Stick, Memory Stick Pro Host Controller with flexible I/O Voltage power.

-. Supports SDIO interface for SDIO peripherals as well as WIFI connectivity.

-. DAI/PCM and I2S interface for Audio application.

- Power Management

-. Power Down Mode for analog and digital circuits.

-. Processor Sleep Mode

-. Pause Mode of 32Khz clocking in Standby state

-. 7 channel Auxiliary 10bit A/D converter for charger and battery monitoring and photo sensing.

- Test and Debug

-. Built-in digital and analog loop back modes for both Audio and baseband front-end.

-. DAI port complying with GSM Rec.11.10

-. JTAG port for debugging embedded MCU.

1.2 Model Feature

- Radio Interface and Baseband Front End

-. GMSK Modulator with analog I and Q channel outputs.

-. 10-bit D/A convert for Uplink baseband I and Q signals.

-. 14bit high resolution A/D converter for downlink baseband I and Q signals.

-. Calibration mechanism of offset and gain mismatch for baseband A/D converter and D/A converter.

-. 10bit D/A converter for Automatic Power Control(APC)

-. 13bit high resolution D/A converter for Automatic frequency Control(AFC)

-. Programmable Radio RX filter.

-. 2 channels Baseband Serial Interface(BSI) with 3-wire control.

-. Bi-Directional BSI interface. RF chip register read access with 3-wire or 4-wire interface

-. 10 pin Baseband Parallel Interface(BPI) with programmable driving strength.

-.Multi-band Support (GSM850, GSM900, DCS1800, PCS1900)

- Voice and Model Codec

-. Dial tone Generation.

-. Voice memo

-. Noise reduction

-. Echo suppression

-. Advanced sidetone Oscillation Reduction.

-. Digital side-tone generator with programmable gain.

-.Two programmable acoustic compensation filters.

-. GSM/GPRS quad vocoders for adaptive multirate(AMR), enhanced full rate(EFR), full rate(FR) and half rate(HR).

-. GSM channel coding, equalization and A5/1 and A5/2 ciphering.

-.GPRS GEA1 and GEA2 ciphering.

-. Programmable GSM/GPRS model.

-. Packet Switched data with CS1/CS2/CS3/CS4 coding schemes.

-.GSM circuit switch data.

-. GPRS Class 12.

- Voice Interface and Voice Front End.

-. Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control(AGC) mechanisms.

-. Voice power amplifier with programmable gain.

-. 2'nd order Sigma-Delta A/D converter for voice uplink path.

-. D/A Converter for Voice downlink path.

-. Supports Half-duplex hands-free operation.

-. Compliant with GSM 03.50.

1.3 Multimedia Feature

- LCD/NAND Flash Interface

-. Dedicated Parallel Interface supports 3 external devices with 8/16 bits NAND flash interface, 8/9/16/18 bit Parallel interface and serial interface for LCM.

-. Built-in NAND flash controller with 1 bit ECC for mass storage.

- LCD Controller

-. Supports simultaneous connection to up to 3 parallel LCD and 2 serial LCD modules.

-. Supports LCM format : RGB332, RGB444, RGB565, RGB666, RGB888.

-. Supports LCD Module with maximum resolution up to 800x600 at 24bpp.

-. Per pixel alpha channel.

-. True colour engine

-. Supports hardware display rotation.

-. Capable of combining display memories with up to 6 blending layers.

- Image Signal Processor

-. 8/10 bit Bayer format image input.

-. YUV422 format image input.

-. Capable of processing image of size up to 3M pixels.

-. Colour correction matrix.

-. Gamma correction.

-. Automatic exposure(AE) control.

-. Automatic focus control.

-. Automatic white balance(AWB) control.

-. Programmable AE/AEB windows.

-. Edge enhancement support.

-. Shading compensation.

-. Defect Pixel compensation.

- Graphic Compression.

-. GIF decoder, PNG Decoder.

- JPEG Decoder

-. ISO/IEC 10918-1 JPEG Baseline and Progressive modes.

-. Supports all possible YUV formats, Including gray-scale format.

-. Supports all DC/AC Huffman table parsing.

-. Supports all quantization table parsing.

-. Supports a restart interval

-. Supports SOS, DHT, DQT and DRI marker parsing.

-. IEEE Std 1180-1990 IDCT standards compliance

-. Supports progressive image processing to minimize storage space requirement.

-. Supports reload-able DMA for VLD stream.

- JPEG Encoder

-. ISO/IEC 10918-1 JPEG baseline mode.

-.ISO/IEC 10918-2 compliance

-. Supports YUV422 and YUV420 and grayscale formats.

-. Supports JFIF.

-. Standard DC and AC Huffman tables.

-. Provides 4 levels of encode quality.

-. Supports continuous shooting.

- Image Data Processing.

-. Supports Digital Zoom.

-. Supports RGB888/565, YUV444 image processing.

-. High throughput hardware scaler. Capable of tailoring an image to an arbitrary size.

-. Horizontal scaling in averaging method.

-. Vertical scaling in bilinear method.

-. Simultaneous scaling for MPEG-4 encode and LCD display.

-. YUV and RGB color space conversion.

-. Pixel format transform.

-. Boundary padding.

-. Pixel processing : hue/saturation/intensity/color adjustment, Gamma correction and grayscale/invert/sepia-tone effects.

-. Programmable spatial filtering : linear filter, non-linear filter and multi-pass artistic effects.

-. Hardware accelerated image editing.

-. Photo frame capability.

-. RGB thumbnail data output.

- MPEG-4/H.263 CODEC

-. Hardware Video CODEC.

-. ISO/IEC 14496-2 simple profile :

Decode @ level 0/1/2/3

Encode @ level 0.

-. ITU-T H.263 profile 0 @level 10.

-. Max decode speed is VGA @15fps.

-. Max encode speed is CIF@15fps.

-. Support VGA mode encoding.

-. Horizontal and vertical de-blocking filter in video playback.

-. Encoder resync marker and HEC.

-. Support visual tools for decoder : I-VOP, P-VOP, AC/DC Prediction, 4-MV, Unrestricted MV, Error Resilience, Short Header.

-. Error Resilience for decoder : Slice Resynchronizaton, Data Partitioning, Reversible VLC.

-. Supported visual tools for encoder : I-VOP, P-VOP, Half-Pel, DC Prediction, Unrestricted MV, Reverible VLC, Short Header.

-. Supports encoding motion vector of range up to -64/+63.5 pixels.

-. HE-AAC decode support.

-. AAC/AMR/WB-AMR audio decode support

-. AMR/WB-AMR audio encode support.

- TV-OUT

-. Supports NTSC/PAL formats(interlaced mode)

-. 10bit video DAC with 2x oversampling.

-. Supports one composite video output.

- Audio CODEC

-. Supports HE-AAC codec decode

-. Supports AAC codec decode

-. Wavetable synthesis with up to 64 tones

-. Advanced wavetable synthesizer capable of generating simulated stereo

-. Wavetable including GM full set of 128 instruments and 47 sets of percussions

-. PCM Playback and Record

-. Digital Audio Playback

- Audio Interface and Audio Front End

-. Supports I2S interface

-. High resolution D/A Converters for Stereo Audio playback

-. Stereo analog input for stereo audio source

-. Analog multiplexer for stereo audio

-. Stereo to mono conversion

Figure 2 is shown the Block Diagram of MT6228 for detailly.

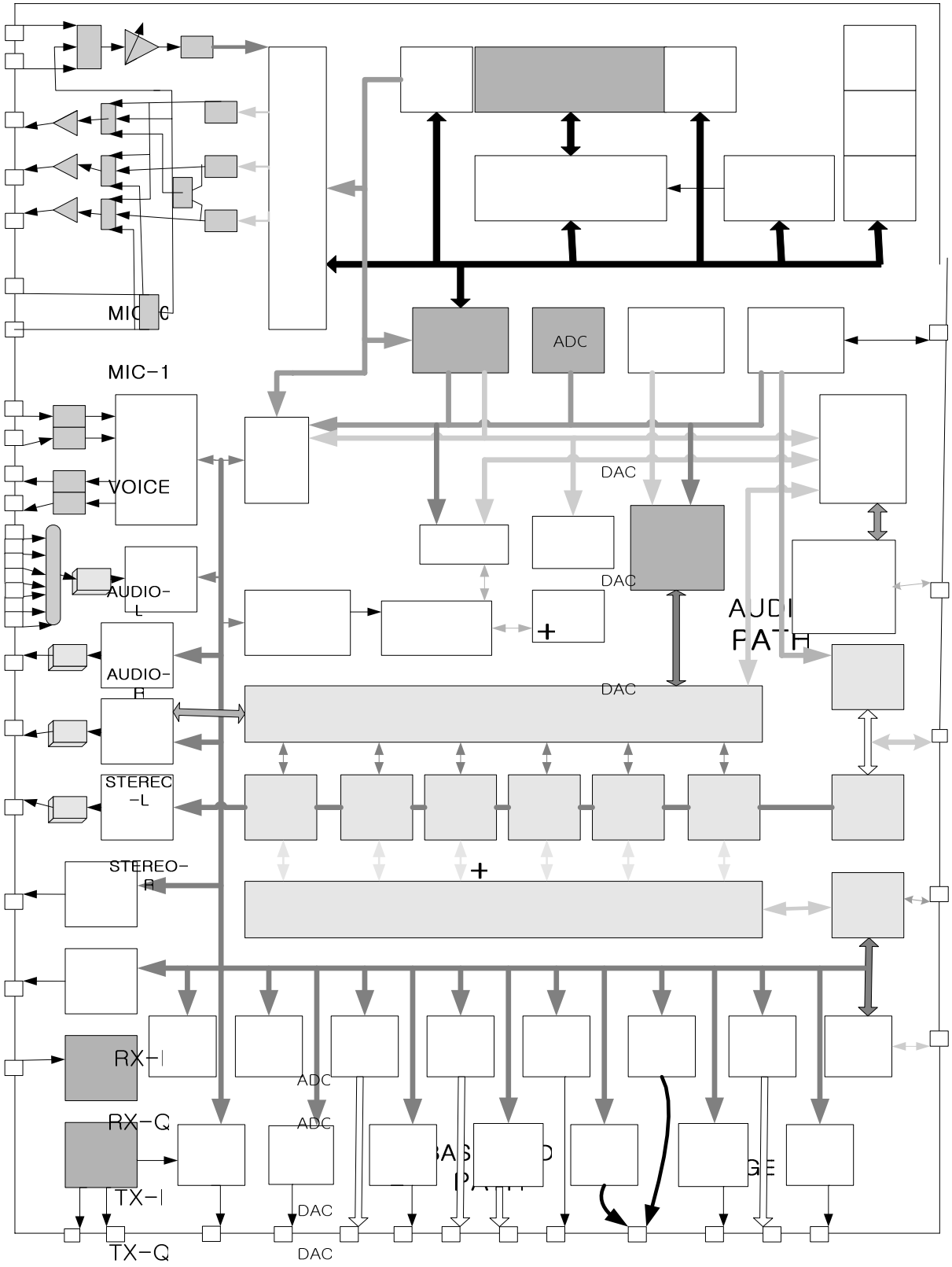


Figure 2 : Block Diagram of MT6228

2. Product Description

Pin Outs

One type of Package for this product, TFBGA 13x13mm, 296balls, 0.65mm pitch package, is offered.

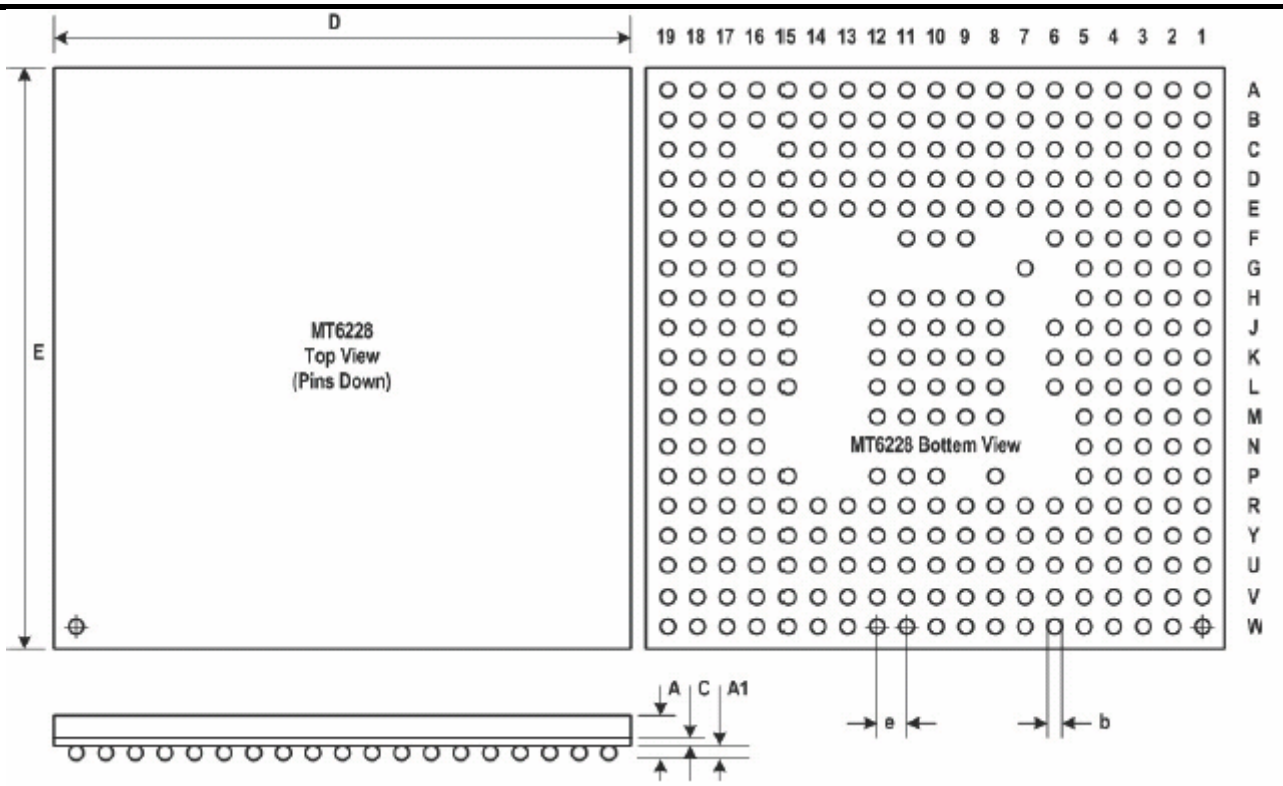
Pin outs and the top view are illustrated in Figure 3,4.

-. Pin Out

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	AVDD_PLL	TVOUT	V8833	AFC_BYP	AUXADIN6	AUXADIN3	AVDD_RFE	BUPAIN	BDLAIN	AU_VIN1_P	AGND_AFE	AU_OUT0_P	AV88_BUF	AU_FMINR	AU_MOUTR	V8833	GPIO9	GPIO8	GPIO6
B	8Y8CLK	AVDD_TV	VDD33	AFC	AUXADIN5	AUXADIN2	APC	BUPAIP	BDLAIN	AU_VIN1_N	AU_VREF_P	AU_OUT0_N	AVDD_BUF	AU_FMINL	AU_MOUTL	V8833	MFIQ	GPIO7	VDD33
C	AV88_PLL	FRE8	AV88_TV	AUX_REF	AUXADIN4	AUXADIN1	AV88_RFE	BUPAQN	BDLAQN	AU_VIN0_N	AU_VREF_N	AU_MICBIAS8_P	AU_OUT1_N	AU_MBYP	AVDD_MBUF	NC	GPIO5	GPIO4	GPIO3
D	XIN	XOUT	AVDD_RTC	VDD33	V8833	AUXADIN0	AVDD_G8MRFTX	BUPAQP	BDLAQP	AU_VIN0_P	AVDD_AFE	AU_MICBIAS8_N	AU_OUT1_P	AV88_MBUF	E8DM_CK	DAIPCMIN	GPIO2	DAI8YNC	DAIR8T
E	BBWAKEUP	V8833	VDDK	JTR8T#	TE8TMODE	VDD33	V8833	AV88_G8MRFTX	AGND_RFE	AV88_AFE	VDD33	V8833	VDD33	V8833	VDD33	KROW1	KROW0	DAICLK	DAIPCMOUT
F	JRTCK	JTDO	JTM8	JTDI	JTCK	PLLOUT			VDD33	V8833	VDDK				KROW4	KROW3	KROW2	VDDK	V8833
G	BPI_BU83	VDD33	BPI_BU82	BPI_BU81	BPI_BU80		NLD17								KCOL3	KCOL2	KCOL1	KCOL0	KROW5
H	V8833	BPI_BU88	BPI_BU87	BPI_BU86	BPI_BU85			CMDAT9	CMPCLK	CMMCLK	CMHREF	CMVREF			IRDA_TXD	IRDA_PDN	KCOL6	KCOL5	KCOL4
J	L8CK	B8I_CLK	B8I_CATA	B8I_C80	BPI_BU89	BPI_BU84		CMDAT8	NLD16	NLD14	NLD11	CMR8T			UTXD2	URXD3	UTXD3	VDD33	IRDA_RXD
K	VDD33	L8CE1#	L8CE0#	L8DA	L8A0	LPCE1#		CMDAT7	NLD15	NLD12	NLD9	CMPDN			URXD1	UTXD1	UCT81	URT81	URXD2
L	LWR#	LPA0	LRD#	LR8T#	LPCE0#	NLD7		CMDAT6	NLD13	NLD10	NLD8	CMDAT0			V8833	8IMCLK	8IMVC	8IM8EL	8IMDATA
M	V8833	VDDK	NLD4	NLD5	NLD6			CMDAT5	CMDAT4	CMDAT3	CMDAT2	CMDAT1				MCWP	MCIN8	MCCK	8IMR8T
N	NRNB	NLD0	NLD1	NLD2	NLD3	MT6228 TFBGA Top_View										VDD33_AUX1	MCDA2	MCDA3	MCPWRON
P	NCE#	NRE#	NWE#	NALE	NCLE			EA11		EA0	EC82#	ERD#			VDDK	VDD33_AUX2	MCCM0	MCDA0	MCDA1
R	VDD33	ALERTER	PWM2	PWM1	EA19	V8833_EMI	EA12	EA8	EA4	VDD33_EMI	EC83#	V8833_EMI	ECKE	EWAIT	ED0	WATCHDOG	V8833_EMI	U8B_DP	U8B_DM
T	8RCLKENAN	8Y8R8T#	8RCLKENAI	8RCLKENA	EA20	EA16	VDD33_EMI	EA9	EA5	EA1	EPDN#	EWR#	EDCLK	ECA8#	ED13	ED10	VDD33_EMI	ED2	ED1
U	GPIO1	EINT0	GPIO0	MIRQ	EA21	EA17	EA13	V8833_EMI	EA6	EA2	V8833_EMI	EC80#	VDD33_EMI	V8833_EMI	ED14	ED11	ED8	ED4	ED3
V	EINT1	EINT3	VDD33_EMI	EA24	EA22	VDD33_EMI	EA14	VDDK	EA7	V8833_EMI	ECLK	EC81#	ELB#	VDDK	VDD33_EMI	ED12	VDD33_EMI	V8833_EMI	ED5
W	EINT2	V8833_EMI	EA25	EA23	V8833_EMI	EA18	EA15	EA10	VDD33_EMI	EA3	EADV#	VDD33_EMI	EUB#	ERA8#	ED15	V8833_EMI	ED9	ED7	ED6

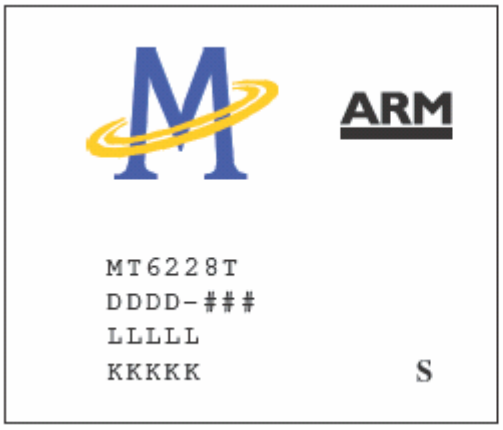
Figure 3 . MT6228(7) Pin Out.

-. Top and Bottom View



Body Size		Ball Count	Ball Pitch	Ball Dia.	Package Thk.	Stand Off	Substrate Thk.
D	E	N	E	B	A(Max.)	A1	C
13	13	314	0.65	0.35	1.2	0.3	0.36

Top Masking Definition



MT6228T: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: U1 Die Lot No.
KKKKK: U2 Die Lot No.
S: Special Code

Figure 5. Top masking definition

Pin Description

			JTAG Port						
E4	**JTRST#**	I	JTAG test port reset input					PD	Input
F5	**JTCK**	I	JTAG test port clock input					PU	Input
F4	**JTDI**	I	JTAG test port data input					PU	Input
F3	**JTMS**	I	JTAG test port mode switch					PU	Input
F2	**JTDO**	O	JTAG test port data output						0
F1	**JRTCK**	O	JTAG test port returned clock output						0
			RF Parallel Control Unit						
G5	**BPI_BUS0**	O	RF hard-wire control bus 0						0
G4	**BPI_BUS1**	O	RF hard-wire control bus 1						0
G3	**BPI_BUS2**	O	RF hard-wire control bus 2						0
G1	**BPI_BUS3**	O	RF hard-wire control bus 3						0
J6	**BPI_BUS4**	O	RF hard-wire control bus 4						0
H5	**BPI_BUS5**	O	RF hard-wire control bus 5						0
H4	BPI_BUS6	IO	RF hard-wire control bus 6	**GPIO16**	BPI_BUS6			PD	Input
H3	BPI_BUS7	IO	RF hard-wire control bus 7	**GPIO17**	BPI_BUS7	13MHz	26MHz	PD	Input
H2	BPI_BUS8	IO	RF hard-wire control bus 4	**GPIO18**	BPI_BUS8	6.5MHz	32KHz	PD	Input
J5	BPI_BUS9	IO	RF hard-wire control bus 5	**GPIO19**	BPI_BUS9	BSI_CS1	BFEPRBO	PD	Input
			RF Serial Control Unit						
J4	**BSI_CS0**	O	RF 3-wire interface chip select 0						0
J3	**BSI_DATA**	O	RF 3-wire interface data output						0
J2	**BSI_CLK**	O	RF 3-wire interface clock output						0
			PWM Interface						
R4	PWM1	IO	Pulse width modulated signal 1	**GPIO32**	PWM1	TBTXFS	DSP_TID2	PD	Input
R3	PWM2	IO	Pulse width modulated signal 2	**GPIO33**	PWM2	TBRXEN	DSP_TID3	PD	Input
R2	ALERTER	IO	Pulse width modulated signal for buzzer	**GPIO34**	ALERTER	TBRXFS	DSP_TID4	PD	Input
			Serial LCD/PM IC Interface						
J1	LSCK	IO	Serial display interface data output	**GPIO20**	LSCK	TDMA_CK	TBTXEN	PU	Input
K5	LSA0	IO	Serial display interface address output	**GPIO21**	LSA0	TDMA_D1	TDTIRQ	PU	Input
K4	LSDA	IO	Serial display interface clock output	**GPIO22**	LSDA	TDMA_D0	TCTIRQ2	PU	Input
K3	LSCE0#	IO	Serial display interface chip select 0 output	**GPIO23**	LSCE0#	TDMA_FS	TCTIRQ1	PU	Input
K2	LSCE1#	IO	Serial display interface chip select 1 output	**GPIO24**	LSCE1#	LPCE2#	TEVTVAL	PU	Input
			Parallel LCD/NAND-Flash Interface						
K6	LPCE1#	IO	Parallel display interface chip select 1 output	**GPIO25**	LPCE1#	NCE1#	DSP_TID0	PU	Input
L5	**LPCE0#**	O	Parallel display interface chip select 0 output						1
L4	**LRST#**	O	Parallel display interface Reset Signal						1
L3	**LRD#**	O	Parallel display interface Read Strobe						1

L2	**LPA0**	O	Parallel display interface address output						1
L1	**LWR#**	O	Parallel display interface Write Strobe						1
G7	NLD17	IO	Parallel LCD/NAND-Flash Data 17	**GPIO11**	NLD17	MCDA4	DSP_TID1	PD	Input
J9	NLD16	IO	Parallel LCD/NAND-Flash Data 16	**GPIO10**	NLD16	MCDA5	DID	PD	Input
K9	**NLD15**	IO	Parallel LCD/NAND-Flash Data 15	**NLD15**	GPIO61		DIMS	PD	Input
J10	**NLD14**	IO	Parallel LCD/NAND-Flash Data 14	**NLD14**	GPIO60		DICK	PD	Input
L9	**NDL13**	IO	Parallel LCD/NAND-Flash Data 13	**NLD13**	GPIO59		SWDBGPKT	PD	Input
K10	**NLD12**	IO	Parallel LCD/NAND-Flash Data 12	**NLD12**	GPIO58		SWDBGWR	PD	Input
J11	**NLD11**	IO	Parallel LCD/NAND-Flash Data 11	**NLD11**	GPIO57		SWDBGRD	PD	Input
L10	**NLD10**	IO	Parallel LCD/NAND-Flash Data 10	**NLD10**	GPIO56		SWDBGROE	PD	Input
K11	**NLD9**	IO	Parallel LCD/NAND-Flash Data 9	**NLD9**	GPIO55		SWDBGA0	PD	Input
L11	**NLD8**	IO	Parallel LCD/NAND-Flash Data 8	**NLD8**	GPIO54		SWDBGA1	PD	Input
L6	**NLD7**	IO	Parallel LCD/NAND-Flash Data 7					PD	Input
M5	**NLD6**	IO	Parallel LCD/NAND-Flash Data 6					PD	Input
M4	**NLD5**	IO	Parallel LCD/NAND-Flash Data 5					PD	Input
M3	**NLD4**	IO	Parallel LCD/NAND-Flash Data 4					PD	Input
N5	**NLD3**	IO	Parallel LCD/NAND-Flash Data 3					PD	Input
N4	**NLD2**	IO	Parallel LCD/NAND-Flash Data 2					PD	Input
N3	**NLD1**	IO	Parallel LCD/NAND-Flash Data 1					PD	Input
N2	**NLD0**	IO	Parallel LCD/NAND-Flash Data 0					PD	Input
N1	**NRNB**	IO	NAND-Flash Read/Busy Flag	**NRNB**	GPIO26	USBSESSVLD	SWDBGD2	PU	
P5	**NCLE**	IO	NAND-Flash Command Latch Signal	**NCLE**	GPIO27	USBVBUSVLD	SWDBGD1	PD	
P4	**NALE**	IO	NAND-Flash Address Latch Signal	**NALE**	GPIO28	USBSESSEND	SWDBGD0	PD	
P3	**NWE#**	IO	NAND-Flash Write Strobe	**NWE#**	GPIO29			PU	
P2	**NRE#**	IO	NAND-Flash Read Strobe	**NRE#**	GPIO30	USBVBUSDSC	SWDBGCK	PU	
P1	**NCE#**	IO	NAND-Flash Chip select output	**NCE#**	GPIO31			PU	
			SIM Card Interface						
M19	**SIMRST**	O	SIM card reset output						0
L16	**SIMCLK**	O	SIM card clock output						0
L17	**SIMVCC**	O	SIM card supply power control						0
L18	SIMSEL	O	SIM card supply power select	**GPIO48**	SIMSEL			PD	Input
L19	**SIMDATA**	IO	SIM card data input/output						0

Dedicated GPIO Interface									
U3	**GPIO0**	IO	General purpose input/output 0	**GPIO0**	CMFLASH		DSP_TID5	PD	Input
U1	**GPIO1**	IO	General purpose input/output 1	**GPIO1**	BSI_RFIN			PD	Input
D17	**GPIO2**	IO	General purpose input/output 2	**GPIO2**	SCL			PU	Input
C19	**GPIO3**	IO	General purpose input/output 3	**GPIO3**	SDA			PU	Input
C18	**GPIO4**	IO	General purpose input/output 4	**GPIO4**	EDICK	URXD2	SWDBGD7		
C17	**GPIO5**	IO	General purpose input/output 5	**GPIO5**	EDIWS	UTXD2	SWDBGD6		
A19	**GPIO6**	IO	General purpose input/output 6	**GPIO6**	EDIDAT		SWDBGD5		
B18	**GPIO7**	IO	General purpose input/output 7	**GPIO7**		USBVBUSON	SWDBGD4		
A18	**GPIO8**	IO	General purpose input/output 19	**GPIO8**	32KHz	USBVBUSCHG	SWDBGF		
A17	**GPIO9**	IO	General purpose input/output 21	**GPIO9**	26MHz	13MHz	SWDBGE		

Miscellaneous									
T2	**SYSRST#**	I	System reset input active low						Input
R16	**WATCHDOG#**	O	Watchdog reset output						1
T1	**SRCLKENAN**	O	External TCXO enable output active low	GPO1	**SRCLKENAN**				0
T4	**SRCLKENA**	O	External TCXO enable output active high	GPO0	**SRCLKENA**				1
T3	SRCLKENAI	IO	External TCXO enable input	**GPIO35**	SRCLKENAI			PD	Input
E5	**TESTMODE**	I	TESTMODE enable input					PD	Input
D15	**ESDM_CK**	O	Internal Monitor Clock						

			Keypad Interface						
H17	**KCOL6**	I	Keypad column 6					PU	Input
H18	**KCOL5**	I	Keypad column 5					PU	Input
H19	**KCOL4**	I	Keypad column 4					PU	Input
G15	**KCOL3**	I	Keypad column 3					PU	Input
G16	**KCOL2**	I	Keypad column 2					PU	Input
G17	**KCOL1**	I	Keypad column 1					PU	Input
G18	**KCOL0**	I	Keypad column 0					PU	Input
G19	**KROW5**	O	Keypad row 5	**KROW5**	GPIO44	ARM CK	TV CK		0
F15	**KROW4**	O	Keypad row 4	**KROW4**	GPIO45	AHB CK	DSP CK		0
F16	**KROW3**	O	Keypad row 3	**KROW3**	GPIO46	FTV CK	SLOW CK		0
F17	**KROW2**	O	Keypad row 2	**KROW2**	GPIO47	FMCU CK	FUSB CK		0
E16	**KROW1**	O	Keypad row 1						0
E17	**KROW0**	O	Keypad row 0						0
			External Interrupt Interface						
U2	**EINT0**	I	External interrupt 0					PU	Input
V1	**EINT1**	I	External interrupt 1					PU	Input
W1	**EINT2**	I	External interrupt 2					PU	Input
V2	**EINT3**	I	External interrupt 3					PU	Input
U4	MIRQ	I	Interrupt to MCU	**GPIO36**	MIRQ	6.5MHz	32KHz	PU	Input
B17	MFIQ	I	Interrupt to MCU	**GPIO63**	MFIQ	USBID	SWDBGD 3	PU	Input

			External Memory Interface						
R15	**ED0**	IO	External memory data bus 0						Input
T19	**ED1**	IO	External memory data bus 1						Input
T18	**ED2**	IO	External memory data bus 2						Input
U19	**ED3**	IO	External memory data bus 3						Input
U18	**ED4**	IO	External memory data bus 4						Input
V19	**ED5**	IO	External memory data bus 5						Input
W19	**ED6**	IO	External memory data bus 6						Input
W18	**ED7**	IO	External memory data bus 7						Input
U17	**ED8**	IO	External memory data bus 8						Input
W17	**ED9**	IO	External memory data bus 9						Input
T16	**ED10**	IO	External memory data bus 10						Input
U16	**ED11**	IO	External memory data bus 11						Input

V16	**ED12**	IO	External memory data bus 12						Input
T15	**ED13**	IO	External memory data bus 13						Input
U15	**ED14**	IO	External memory data bus 14						Input
W15	**ED15**	IO	External memory data bus 15						Input
P12	**ERD#**	O	External memory read strobe						1
T12	**EWR#**	O	External memory write strobe						1
U12	**ECS0#**	O	External memory chip select 0						1
V12	**ECS1#**	O	External memory chip select 1						1
P11	**ECS2#**	O	External memory chip select 2						1
R11	**ECS3#**	O	External memory chip select 3						1
R14	**EWAIT**	O	Flash, PSRAM and CellularRAM data ready					PU	Input
T14	**ECAS#**	O	MobileRAM column address						1
W14	**ERAS#**	O	MobileRAM row address						1
R13	**ECKE**	O	MobileRAM clock enable						1
T13	**EDCLK**	O	MobileRAM clock						
V13	**ELB#**	O	External memory lower byte strobe						1
W13	**EUB#**	O	External memory upper byte strobe						1
T11	**EPDN#**	O	PSRAM power down control	GPO2	**EPDN#**	26Mhz	13MHz		0
W11	**EADV#**	O	Flash, PSRAM and CellularRAM address valid						1
V11	**ECLK**	O	Flash, PSRAM and CellularRAM clock						0
P10	**EA0**	O	External memory address bus 0						0
T10	**EA1**	O	External memory address bus 1						0
U10	**EA2**	O	External memory address bus 2						0
W10	**EA3**	O	External memory address bus 3						0
R9	**EA4**	O	External memory address bus 4						0
T9	**EA5**	O	External memory address bus 5						0
U9	**EA6**	O	External memory address bus 6						0
V9	**EA7**	O	External memory address bus 7						0
R8	**EA8**	O	External memory address bus 8						0
T8	**EA9**	O	External memory address bus 9						0
W8	**EA10**	O	External memory address bus 10						0
P8	**EA11**	O	External memory address bus 11						0
R7	**EA12**	O	External memory address bus 12						0
U7	**EA13**	O	External memory address bus 13						0
V7	**EA14**	O	External memory address bus 14						0
W7	**EA15**	O	External memory address bus 15						0
T6	**EA16**	O	External memory address bus 16						0
U6	**EA17**	O	External memory address bus 17						0
W6	**EA18**	O	External memory address bus 18						0
R5	**EA19**	O	External memory address bus 19						0
T5	**EA20**	O	External memory address bus 20						0
U5	**EA21**	O	External memory address bus 21						0
V5	**EA22**	O	External memory address bus 22						0
W4	**EA23**	O	External memory address bus 23						0
V4	**EA24**	O	External memory address bus 24						0
W3	**EA25**	O	External memory address bus 25						0

			USB Interface						
R18	**USB_DP**	IO	USB D+ Input/Output						
R19	**USB_DM**	IO	USB D- Input/Output						

			Memory Card Interface						
P17	**MCCM0**	IO	SD Command/MS Bus State Output					PU/PD	
P18	**MCDA0**	IO	SD Serial Data IO 0/MS Serial Data IO					PU/PD	
P19	**MCDA1**	IO	SD Serial Data IO 1					PU/PD	
N17	**MCDA2**	IO	SD Serial Data IO 2					PU/PD	
N18	**MCDA3**	IO	SD Serial Data IO 3					PU/PD	
M18	**MCCK**	O	SD Serial Clock/MS Serial Clock Output						
N19	**MCPWRON**	O	SD Power On Control Output						
M16	**MCWP**	I	SD Write Protect Input					PU/PD	Input
M17	**MCINS**	I	SD Card Detect Input					PU/PD	Input

			UART/IrDA Interface						
K15	**URXD1**	I	UART 1 receive data					PU	Input
K16	**UTXD1**	O	UART 1 transmit data						1
K17	**UCTS1**	I	UART 1 clear to send					PU	Input
K18	**URTS1**	O	UART 1 request to send						1
K19	URXD2	IO	UART 2 receive data	**GPIO37**	URXD2	UCTS3		PU	Input
J15	UTXD2	IO	UART 2 transmit data	**GPIO38**	UTXD2	URTS3		PU	Input
J16	URXD3	IO	UART 3 receive data	**GPIO39**	URXD3			PU	Input
J17	UTXD3	IO	UART 3 transmit data	**GPIO40**	UTXD3		DSP_TID6	PU	Input
J19	IRDA_RXD	IO	IrDA receive data	**GPIO41**	IRDA_RXD	UCTS2	SWDBGD15	PU	Input
H15	IRDA_TXD	IO	IrDA transmit data	**GPIO42**	IRDA_TXD	URTS2	SWDBG14	PU	Input
H16	IRDA_PDN	IO	IrDA Power Down Control	**GPIO43**	IRDA_PDN		SWDBG13	PU	Input

			Digital Audio Interface						
E18	DAICLK	IO	DAI clock output	**GPIO49**	DAICLK		SWDBGD12	PU	Input
E19	DAIPCMOUT	IO	DAI pcm data out	**GPIO50**	DAIPCMOUT		SWDBGD11	PD	Input
D16	DAIPCMIN	IO	DAI pcm data input	**GPIO51**	DAIPCMIN		SWDBGD10	PU	Input
D19	DAIRST	IO	DAI reset signal input	**GPIO52**	DAIRST		SWDBG9	PU	Input
D18	DAISYNC	IO	DAI frame synchronization signal output	**GPIO53**	DAISYNC		SWDBG8	PU	Input

CMOS Sensor Interface									
J12	CMRST	IO	CMOS sensor reset signal output	**GPIO12**	CMRST			PD	Input
K12	CMPDN	IO	CMOS sensor power down control	**GPIO13**	CMPDN			PD	Input
H12	**CMVREF**	I	Sensor vertical reference signal input					PD	Input
H11	**CMHREF**	I	Sensor horizontal reference signal input					PD	Input
H9	**CMPCLK**	I	CMOS sensor pixel clock input					PD	Input
H10	**CMMCLK**	O	CMOS sensor master clock output						0
H8	**CMDAT9**	I	CMOS sensor data input 9	**CMDAT 9**	GPIO74			PD	Input
J8	**CMDAT8**	I	CMOS sensor data input 8	**CMDAT 8**	GPIO73			PD	Input
K8	**CMDAT7**	I	CMOS sensor data input 7	**CMDAT**	GPIO72			PD	Input
				7					
L8	**CMDAT6**	I	CMOS sensor data input 6	**CMDAT 6**	GPIO71			PD	Input
M8	**CMDAT5**	I	CMOS sensor data input 5	**CMDAT 5**	GPIO70			PD	Input
M9	**CMDAT4**	I	CMOS sensor data input 4	**CMDAT 4**	GPIO69			PD	Input
M10	**CMDAT3**	I	CMOS sensor data input 3	**CMDAT 3**	GPIO68			PD	Input
M11	**CMDAT2**	I	CMOS sensor data input 2	**CMDAT 2**	GPIO62			PD	Input
M12	CMDAT1	IO	CMOS sensor data input 1	**GPIO14**	CMDAT1			PD	Input
L12	CMDAT0	IO	CMOS sensor data input 0	**GPIO15**	CMDAT0			PD	Input

Analog Interface									
B15	**AU_MOUL**		Audio analog output left channel						
A15	**AU_MOUR**		Audio analog output right channel						
C14	**AU_M_BYP**		Audio DAC bypass pin						
B14	**AU_FMINL**		FM radio analog input left channel						
A14	**AU_FMINR**		FM radio analog input right channel						
D13	**AU_OUT1_P**		Earphone 1 amplifier output (+)						
C13	**AU_OUT1_N**		Earphone 1 amplifier output (-)						
B12	**AU_OUT0_N**		Earphone 0 amplifier output (-)						
A12	**AU_OUT0_P**		Earphone 0 amplifier output (+)						
C12	**AU_MICBIAS_P**		Microphone bias supply (+)						
D12	**AU_MICBIAS_N**		Microphone bias supply (-)						
C11	**AU_VREF_N**		Audio reference voltage (-)						
B11	**AU_VREF_P**		Audio reference voltage (+)						
D10	**AU_VIN0_P**		Microphone 0 amplifier input (+)						
C10	**AU_VIN0_N**		Microphone 0 amplifier input (-)						
B10	**AU_VIN1_N**		Microphone 1 amplifier input (-)						
A10	**AU_VIN1_P**		Microphone 1 amplifier input (+)						
D9	**BDLAQP**		Quadrature input (Q+) baseband codec downlink						
C9	**BDLAQN**		Quadrature input (Q-) baseband codec downlink						
A9	**BDLAIN**		In-phase input (I+) baseband codec downlink						
B9	**BDLAIP**		In-phase input (I-) baseband codec downlink						
B8	**BUPAIP**		In-phase output (I+) baseband codec uplink						
A8	**BUPAIN**		In-phase output (I-) baseband codec uplink						
C8	**BUPAQN**		Quadrature output (Q+) baseband codec uplink						
D8	**BUPAQP**		Quadrature output (Q-) baseband codec uplink						
B7	**APC**		Automatic power control DAC output						
D6	**AUXADIN0**		Auxiliary ADC input 0						
C6	**AUXADIN1**		Auxiliary ADC input 1						
B6	**AUXADIN2**		Auxiliary ADC input 2						
A6	**AUXADIN3**		Auxiliary ADC input 3						
C5	**AUXADIN4**		Auxiliary ADC input 4						
B5	**AUXADIN5**		Auxiliary ADC input 5						
A5	**AUXADIN6**		Auxiliary ADC input 6						
C4	**AUX_REF**		Auxiliary ADC reference voltage input						
B4	**AFC**		Automatic frequency control DAC output						
A4	**AFC_BYP**		Automatic frequency control DAC bypass capacitance						

			VCXO Interface						
B1	**SYSCLK**		13MHz or 26MHz system clock input						
F6	**PLLOUT**		PLL reference voltage output						

			RTC Interface						
D1	**XIN**		32.768 KHz crystal input						
D2	**XOUT**		32.768 KHz crystal output						
E1	**BBWAKEUP**	O	Baseband power on/off control						1
			TV Interface						
A2	**TVOUT**		TV DAC Output						
C2	**FSRES**								

			Supply Voltages						
E3	**VDDK**		Supply voltage of internal logic						
M2	**VDDK**		Supply voltage of internal logic						
V8	**VDDK**		Supply voltage of internal logic						
V14	**VDDK**		Supply voltage of internal logic						
F18	**VDDK**		Supply voltage of internal logic						
F11	**VDDK**		Supply voltage of internal logic						
V3	**VDD33_EMI**		Supply voltage of memory interface driver						
V6	**VDD33_EMI**		Supply voltage of memory interface driver						
T7	**VDD33_EMI**		Supply voltage of memory interface driver						
W9	**VDD33_EMI**		Supply voltage of memory interface driver						
R10	**VDD33_EMI**		Supply voltage of memory interface driver						
W12	**VDD33_EMI**		Supply voltage of memory interface driver						
U13	**VDD33_EMI**		Supply voltage of memory interface driver						
V15	**VDD33_EMI**		Supply voltage of memory interface driver						
T17	**VDD33_EMI**		Supply voltage of memory interface driver						
V17	**VDD33_EMI**		Supply voltage of memory interface driver						
W5	**VSS33_EMI**		Ground of memory interface driver						
R6	**VSS33_EMI**		Ground of memory interface driver						
U8	**VSS33_EMI**		Ground of memory interface driver						
V10	**VSS33_EMI**		Ground of memory interface driver						
U11	**VSS33_EMI**		Ground of memory interface driver						
R12	**VSS33_EMI**		Ground of memory interface driver						
U14	**VSS33_EMI**		Ground of memory interface driver						
W16	**VSS33_EMI**		Ground of memory interface driver						
R17	**VSS33_EMI**		Ground of memory interface driver						
V18	**VSS33_EMI**		Ground of memory interface driver						

P16	**VDD33_AUX 2**		Supply voltage of drivers for USB						
N16	**VDD33_AUX 1**		Supply Voltage of MS/MMC/SD						
G2	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
K1	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
R1	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
J18	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
B19	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
E15	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
E13	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
E11	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
F9	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
E6	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						

D4	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
B3	**VDD33**		Supply voltage of drivers except memory interface, USB and MS/MMC/SD						
W2	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
E2	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
H1	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
M1	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
L15	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
F19	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
B16	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
A16	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
E14	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
E12	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
F10	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
E7	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
D5	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
A3	**VSS33**		Ground of drivers except memory interface, USB and MS/MMC/SD						
A1	**AVDD_PLL**		Supply voltage for PLL						
C1	**AVSS_PLL**		Ground for PLL supply						
B2	**AVDD_TV**		Supply voltage for TV out						
C3	**AVSS_TV**		Ground for TV out						
D3	**AVDD_RTC**		Supply voltage for Real Time Clock						

			Analog Supplies						
C15	**AVDD_MBUF**		Supply Voltage for Audio band section						
D14	**AVSS_MBUF**		GND for Audio band section						
B13	**AVDD_BUF**		Supply voltage for voice band transmit section						
A13	**AVSS_BUF**		GND for voice band transmit section						
D11	**AVDD_AFE**		Supply voltage for voice band receive section						
A11	**AGND_AFE**		GND reference voltage for voice band section						
E10	**AVSS_AFE**		GND for voice band receive section						
E9	**AGND_RFE**		GND reference voltage for baseband section, APC, AFC and AUXADC						
E8	**AVSS_GSMRFTX**		GND for baseband transmit section						
D7	**AVDD_GSMRFTX**		Supply voltage for baseband transmit section						
C7	**AVSS_RFE**		GND for baseband receive section, APC, AFC and AUXADC						
A7	**AVDD_RFE**		Supply voltage for baseband receive section, APC, AFC and AUXADC						

3. Micro-Controller Unit Subsystem

Figure 6 illustrates the block diagram of the Micro-Controller Unit Subsystem in MT6228. The Subsystem utilizes a main 32-bit ARM7EJ-S RISC processor, which plays the role of the main bus master controlling the whole subsystem. The processor communicates with all the other on-chip modules via the two-level system buses: AHB Bus and APB Bus. All bus transactions originate from bus masters, while salves can only respond to requests from bus masters. Before data transfer can be established, bus master must ask for bus ownership. This is accomplished by request-grant handshaking protocol between masters and arbiters.

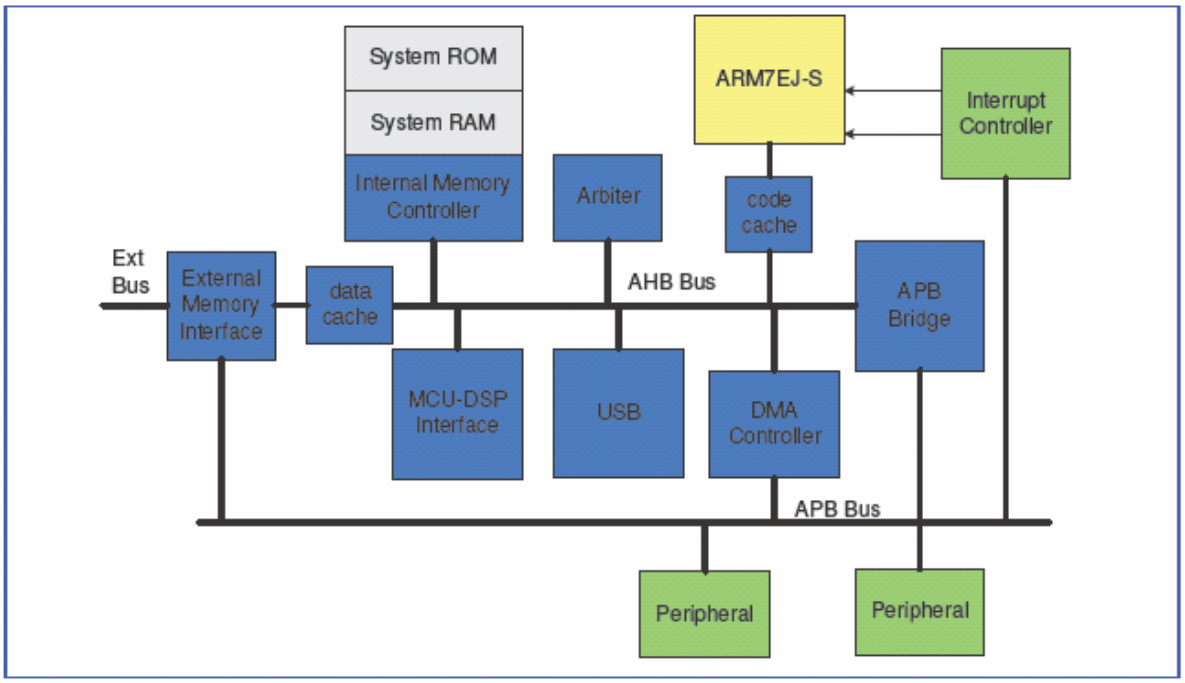


Figure 6. Block Diagram of MCU in MT6228

3.1 Processor Core

The Micro-Controller Unit subsystem in MT6228 uses the 32-bit Arm7EJ-S RISC processor that is based on the Von Neumann architecture with a single 32-bit data bus carrying both instructions and data. The memory interface of ARM7EJ-S is totally compliant to AMBA based bus system, which allows direct connection to the AHB Bus.

3.2 Memory Management

The processor core of MT6228 supports only memory addressing method for instruction fetch and data access. It manages a 32bit address space that has addressing capability up to 4GB. System RAM, System ROM , Registers, MCU Peripherals and external components are all mapped onto such 32-bit address space, as depicted in Figure 7.

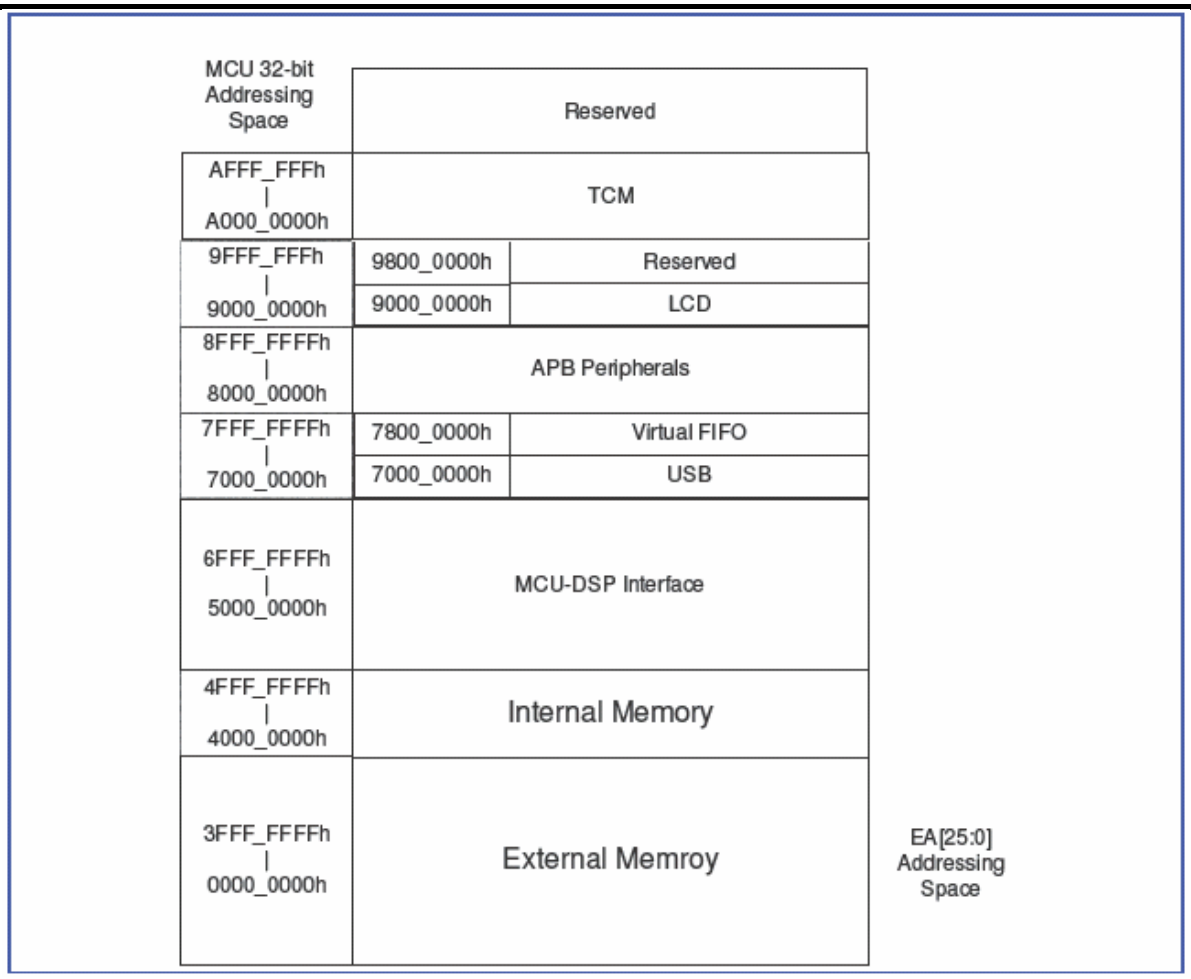


Figure 7. Memory Layout of MT6228

External Memory Access

To allow external access, the MT6228 outputs 26 bits (A25-A0) of address lines along with 4 selection signals that correspond to associated memory blocks. That is, MT6228 can support up to 4 MCU addressable external components. The data width of internal system bus is fixed at 32-bit wide, while the data width of the external components can be either 8- or 16- bit. Since devices are usually available with varied operating grades, adaptive configurations for different applications are needed.

Factory Programming

The configuration for factory programming is shown in Figure 8. Usually the Factory Programming Host connects with MT6228 via the UART interface. The download speed can be up to 921K bps while MCU is running at 26MHz.

After the system has reset, the Boot Code guides the processor to run the Factory Programming software placed in System ROM. Then, MT6228 starts and polls the UART1 port until valid information is detected. The first information received on the UART1 is used to configure the chip for factory programming. The Flash downloader program is then transferred into System RAM or external SRAM. Further information is detailed in the MT6228 Software Programming Specification.

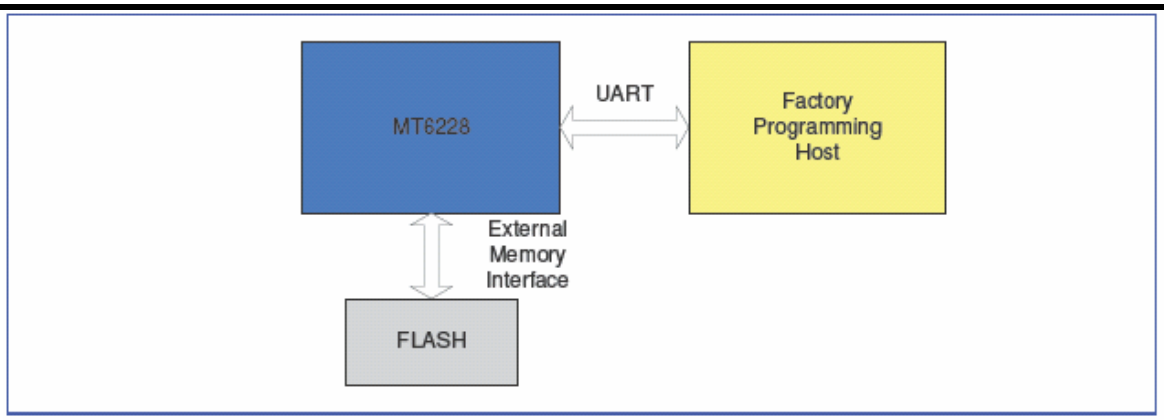


Figure 8. Factory Programming

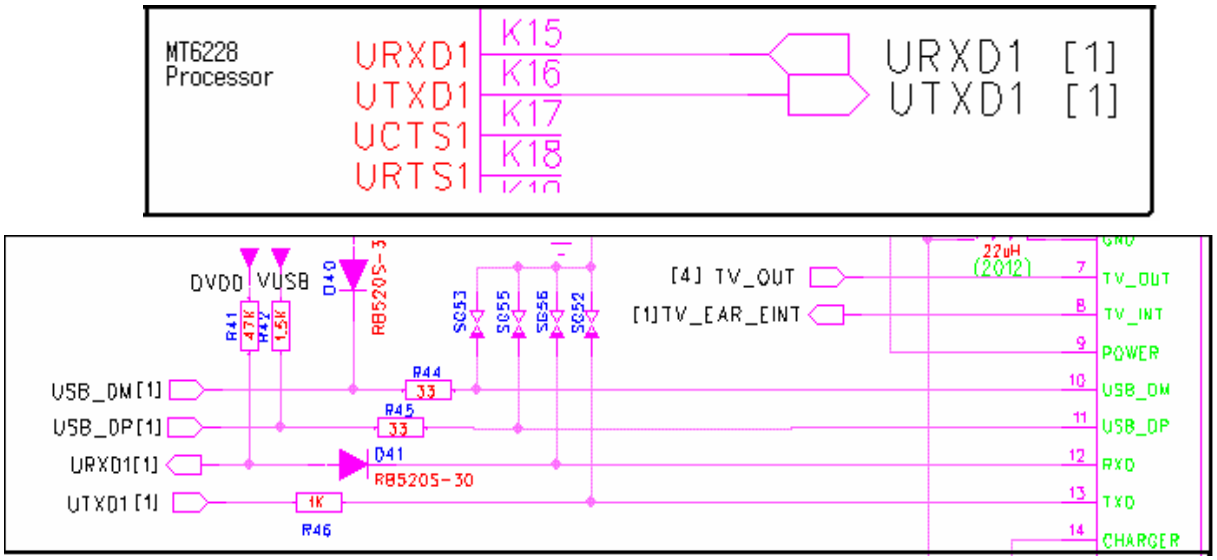


Figure 9. Circuit from MT6228 to I/O Connector

As shown in Figure 9, The UART is minimum UART and The Pin K15, K16 in MT6228 are used. The R41(47Kohm) is a pull up resistor for RXD.

3.3 Interrupt Controller

Figure 10 outlines the major functionality of the MCU Interrupt Controller. The interrupt controller processes all interrupt sources coming from external lines and internal MCU peripherals. Since ARM7EJ-S core supports two levels of interrupt latency, this controller generates two request signals: FIQ for fast, low latency interrupt request and IRQ for more general interrupts with lower priority.

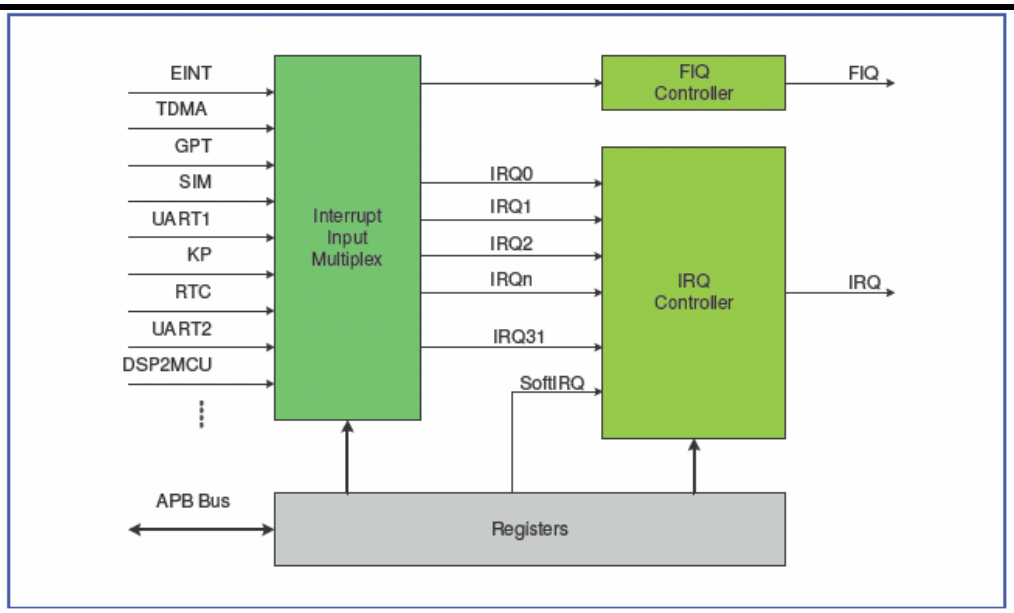


Figure 10. Block Diagram of Interrupt controller.

External Interrupt

This interrupt is for User interrupts of Accessory or peripheral components. This interrupt controller also integrates an External Interrupt controller that can support up to 4 interrupt requests coming from external sources, the EINT0~3 and 4 wake up interrupt requests. The four external interrupts can be used for different kind of applications, mainly for event detections .

MT6217/8B/9 EINT	BB Pin	Pin Name	GPIO MODE 0	GPIO MODE 1	GPIO MODE 2	GPIO MODE 3
EINT0	V1	EINT0	----	----	----	----
EINT1	U3	EINT1	----	----	----	----
EINT2	W1	EINT2	----	----	----	----
EINT3	V2	EINT3	----	----	----	----
EINT4	P16	USB_DP	----	----	----	----
EINT5	K18	URXD1	----	----	----	----
EINT6	J18	URXD2	GPIO35	URXD2	UCTS3	----
EINT7	H15	URXD3	GPIO33	URXD3	----	----
MIRQ	R5	MIRQ	GPIO41	MIRQ	13MHz	6.5MHz
MFIQ (6219 only)	R17	MFIQ	GPIO42	MFIQ	----	----

In MEGA3, External interrupts are used as followings.

-. EINT 0 : TV Out cable and Headset Detection.

-. EINT 1 : Folder On/Off

-. EINT 2 : Charger/USB Power Detection.

-. EINT 3 : Touch Panel .

-. EINT 4 : USB_DP.

-. EINT 5 : URXD1

-. EINT 6 : Blue Tooth Calling.

3.4 Internal Memory Interface

System Ram

MT6228 provides one 128 KByte size of on-chip memory modules acting as System RAM for data access with low latency. Such a module is composed of one high speed synchronous SRAMs with AHB Slave Interface connected to the system backbone AHB Bus, The synchronous SRAM operates on the same clock as the AHB Bus and is organized as 32 bits wide with 4 byte-write signals capable for byte operations. The SRAM macro has limited repair capability. The yield of SRAM is improved if the defects inside it can be repaired during testing.

System ROM

The System ROM is primarily used to store software program for Factory Programming. However, due to its advantageous low latency performance, some of the timing critical codes are also placed in System ROM. This module is composed of high-speed VIA ROM with an AHB Slave Interface connected to a system backbone AHB. The module operates on the same clock as the AHB and has a 32-bit wide organization.

3.5 External Memory Interface

MT6228 incorporates a powerful and flexible memory controller, External Memory Interface, to connect with a variety of memory components. This controller provides one generic access scheme for Flash Memory, SRAM, PSRAM and CellularRAM and another access scheme for MobileRAM. Up to 4 memory banks can be supported simultaneously, BANK0-BANK3, with a maximum size of 64MB each. Since most of the Flash Memory, SRAM, PSRAM and CellularRAM have similar AC requirements, a generic configuration scheme to interface them is desired. This way, the software program can treat different components by simply specifying certain predefined parameters. All these parameters are based on the cycle time of system clock. The interface definition based on such a scheme is listed in Table 17. Note that, this interface always works with data in Little Endian format for all types of access.

Signal Name	Type	Description
EA[25:0]	O	Address Bus
ED[15:0]	I/O	Data Bus
EWR#	O	Write Enable Strobe/MobileRAM Command Input
ERD#	O	Read Enable Strobe
ELB#	O	Lower Byte Strobe/MobileRAM Data Input & Output Mask
EUB#	O	Upper Byte Strobe/MobileRAM Data Input & Output Mask
ECS[3:0]#	O	BANK0~BANK3 Selection Signal
EPDN	O	PSRAM Power Down Control Signal
ECLK	O	Flash, SRAM, PSRAM and CellularRAM Clock Signal
EADV#	O	Flash, SRAM, PSRAM and CellularRAM Address Valid Signal
EWAIT	I	Flash, SRAM, PSRAM and CellularRAM Wait Signal Input
EDCLK	O	MobileRAM Clock Signal
ECKE	O	MobileRAM Clock Enable Signal
ERAS#	O	MobileRAM Row Address Signal
ECAS#	O	MobileRAM Column Address Signal

Table 17 **External Memory Interface Signal of MT6228**

In MEGA3, ECS0# is used for External SDRAM. The other ECSx# not used. Because of the Nand MCP used.

The Nand MCP is HYC0UGE0MF1P-5SH0E (1Gb Nand Flash x 256Mb SDRAM) from Hynix.

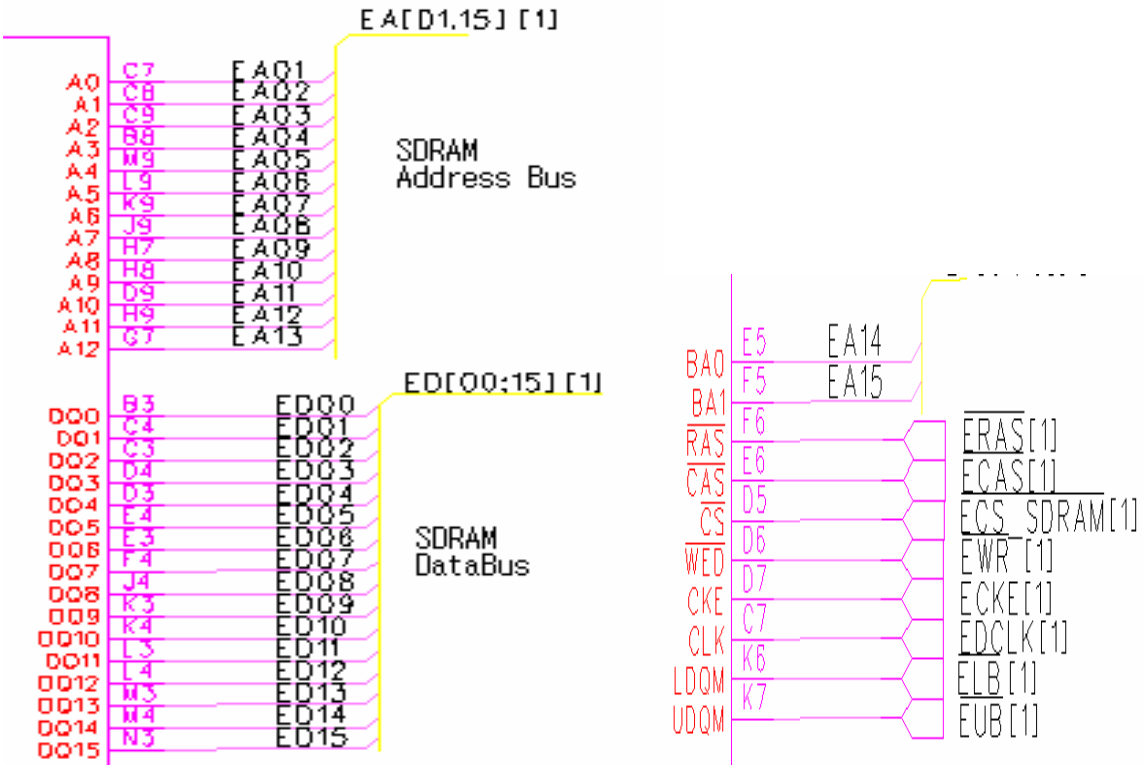


Figure 11 : Hynix Nand MCP Address, Data Bus and control Signals of SDRAM.

4. Microcontroller Peripherals

Microcontroller(MCU) Peripherals are devices that are under direct control of the Microcontroller. Most of the devices are attached to the Advanced Peripheral Bus(APB) of the MCU subsystem, and serve as APB slaves. Each MCU peripheral must be accessed as a memory-mapped I/O device: that is, the MCU or the DMA bus master reads from or writes to the specific peripheral by issuing memory-addressed transactions.

Pulse-Width Modulation Outputs.

Two generic Pulse-Width Modulators are implemented to generate pulse sequences with programmable frequency and duty cycle for LCD backlight or charging purpose. The duration of the PWM output signal is low as long as the internal counter value is greater than or equal to the threshold value.

In MEGA3, PWM1 is used for LCD Module Backlight Enable and PWM2 is used for Flash LED Enable for GPIO mode.

SIM Interface

The MT6228 contains a dedicated smart card interface to allow the MCU access to the SIM card. It can operate via 5 terminals, using SIMVCC, SIMSEL, SIMRST, SIMCLK and SIMDATA.

The SIMVCC is used to control the external voltage supply to the SIM card and SIMSEL determines the regulated smart card supply voltage. SIMRST is used as the SIM card reset signal. Besides, SIMDATA and SIMCLK are used for data exchange purpose. Basically, the SIM interface acts as a half duplex asynchronous communication port and its data format is composed of ten consecutive bits: a start bit in state Low, eight information bits and a tenth bit used for parity checking.

In MEGA3, Only 3V SIM interface is used. As Figure 12 shown, The External Level Shift is in PM(MT6318).

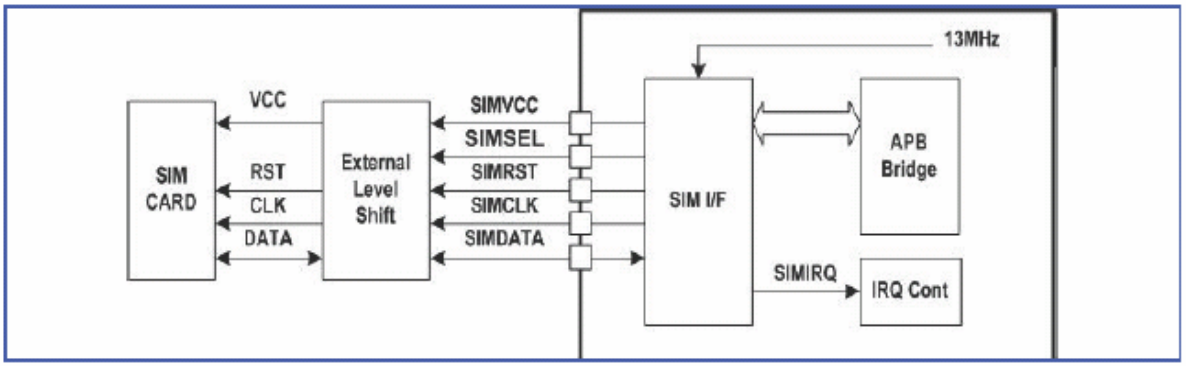


Figure 12. SIM interface

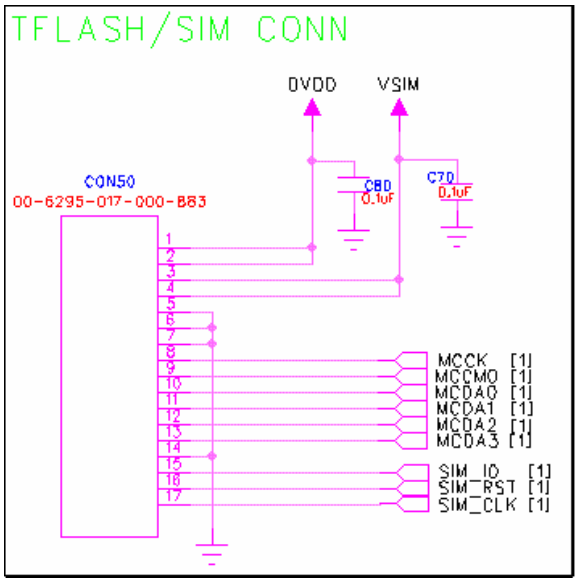


Figure 13. SIM/TFLAH Connector Circuit

In MEGA3, The SIM Connector is soldered on FPCB with T-Flash Connector as above Figure 13.

Keypad Scanner

The keypad can be divided into two parts : One is the keypad interface including 7 columns and 6 rows The other is the key detection block which provides key pressed, key released and de-bounce mechanism. Each time the key is pressed or released, i.e. something different in the 7x6 matrix, the key detection block will sense it, and it will start to recognize if it is a key pressed or key released event. Whenever the key status changes and is stable, a KEYPAD IRQ will be issued. The MCU can then read the key pressed directly in KP_HI_KEY, KP_MID_KEY and KP_LOW_KEY register.

In MEGA3, The 6 Rows are used (Row0 ~Row5) and The 5 Columns are used (Col 0~3 and Col 6)

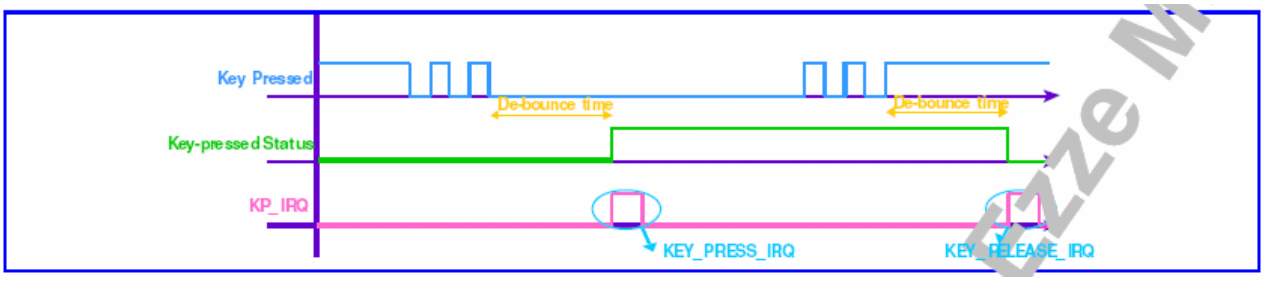


Figure 14. Key pressed with de-bounce mechanism

In MEGA3, The 6 Rows are used (Row0 ~Row5) and The 5 Columns are used (Col 0~3 and Col 6)

The 3x4 and Power On Keys are on Main Body. And Soft_Left/Right, Navy key are on Slide Body.

The Figure 15 shows the circuit.

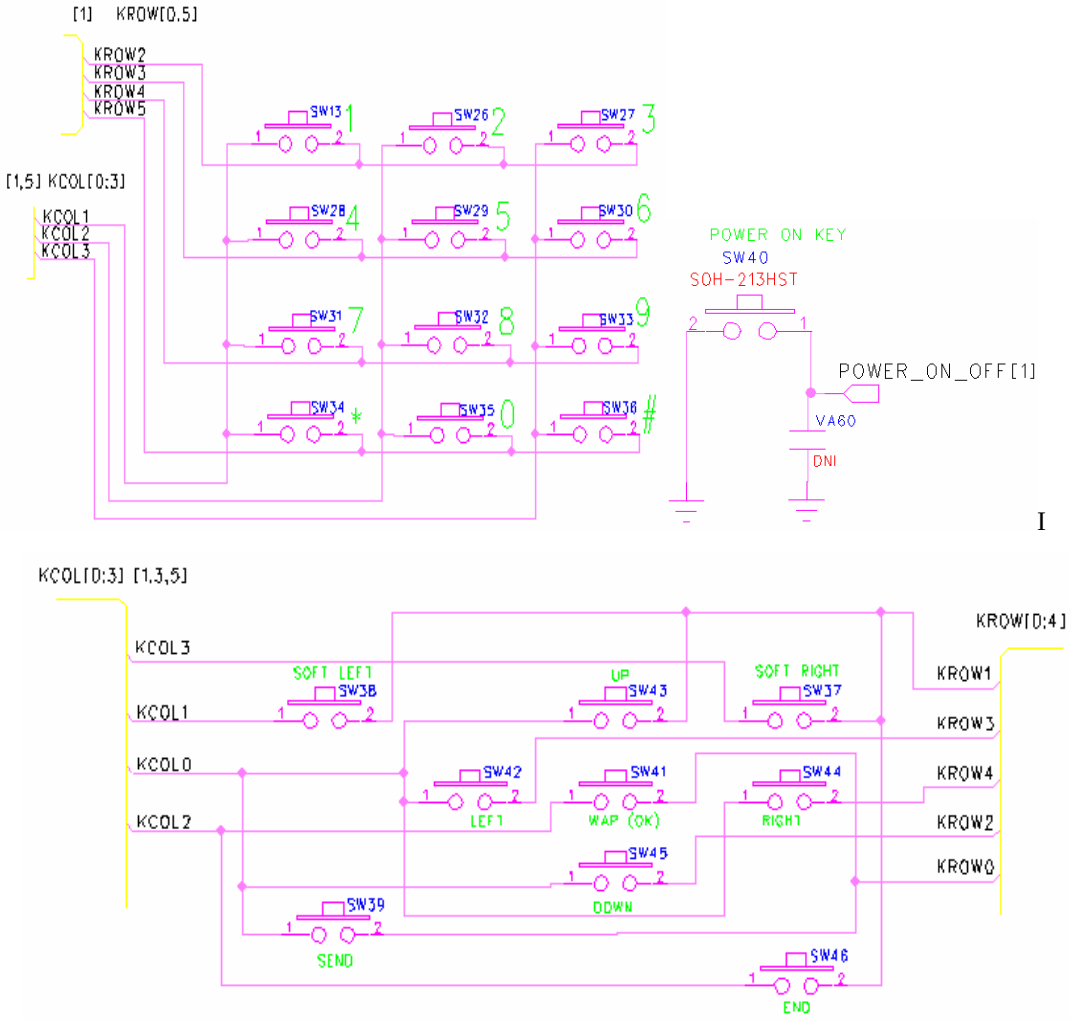


Figure 15. MEGA3 Key Scan Circuit.

General Purpose Inputs/Outputs

MT6228 offers 57 general purpose I/O pins and 5 general-purpose output pins. By setting the control registers, MCU software can control the direction, the output value and read the input values on these pins. These GPIOs and GPOs are multiplexed with other functionalities to reduce the pin count.

Upon hardware reset(/SYSRST), GPIOs are all configured as inputs and the following alternate usages of the GPIO pins are enabled.

Multiplexing of Signals on GPIO

The GPIO pins can be multiplexed with other signals.

-. DAICLK, DAIPCMIN, DAIPCMOUT, DAIRST: digital audio interface for FTA

-. BPI_BUS6, BPI_BUS7, BPI_BUS8, BPI_BUS9: radio hardwired control

-. BSI_CS1: additional chip select signal for radio 3-wire interface

-. LSCK, LSA0, LSDA, LSCE0#, LSCE1#: serial display interface

-. LPCE1#: parallel display interface chip select signal

-. NRNB, NCLE, NALE, NWEB, NREB, NCEB: NAND flash control signals

-. PWM1, PWM2: pulse width modulation signal ALERTER: pulse width modulation signal for buzzer

-. IRDA_RXD, IRDA_TXD, IRDA_PDN: IrDA control signals

-. URXD2, UTXD2, UCTS2, URTS2: data and flow control signals for UART2

-. URXD3, UTXD3, UCTS3, URTS3: data and flow control signals for UART3

-. CMRST, CMPDN, CMDAT9, CMDAT8, CMDAT7, CMDAT6, CMDAT5, CMDAT4, CMDAT3, CMDAT2, CMDAT1, CMDAT0: sensor interface

-. SRCLKENAI: external power on signal of the external VCXO LDO

-. NLD8, NLD9, NLD10, NLD11, NLD12, NLD13, NLD14, NLD15, NLD16, NLD17: NAND FLASH and Parallel LCD data signals

-. MFIQ, MIRQ: external interrupt

-. MCDA4, MCDA5, MCDA6, MCDA7: MMC4.0 data signals

Multiplexed of Signals on GPO

-. SRCLKENA, SRCLKENAN: power on signal of the external VCXO LDO

-. EPDN: external memory interface power down controls

UART

The baseband chipset houses three UARTs. The UARTs provide full duplex serial communication channels between baseband chipset and external devices. The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers.

In MEGA3, UART1(URXD1, UTXD1) is used for Factory Programming and UART3(URXD3, UTXD3) is used for Blue Tooth Programming.

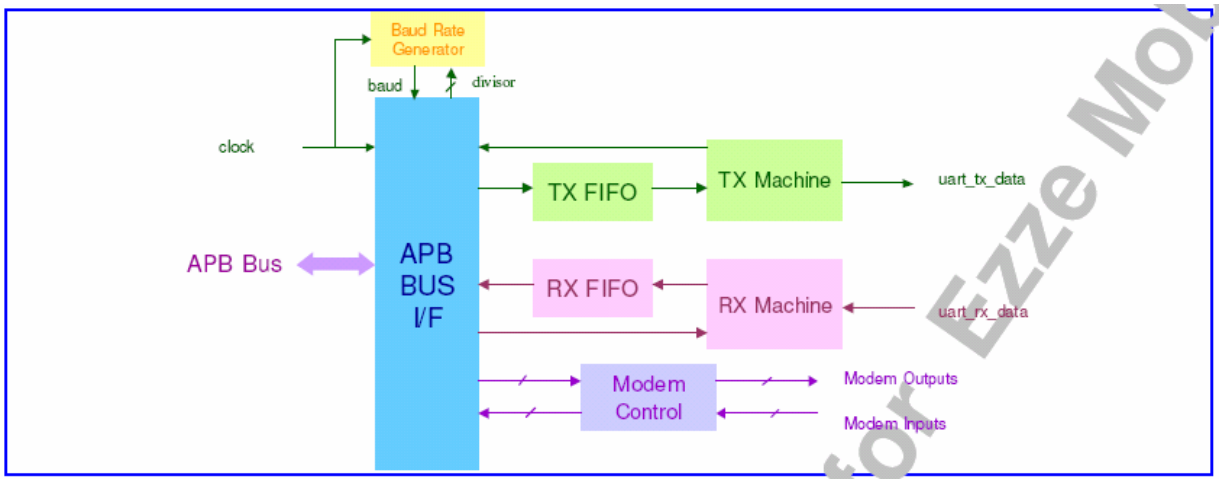


Figure 16. UART block diagram.

RX data Timeout Interrupt :

When virtual FIFO mode is disabled, RX data Timeout Interrupt is generated if all of the following apply :

1. FIFO contains at least on character.
2. The most recent character was received longer than four character periods ago(including all start, parity and stop bit)

3. The most recent CPU read of the FIFO was longer than four character periods ago.

When virtual FIFO mode is enabled, RX Data timeout Interrupt is generated if all of the following apply:

1. FIFO is empty.
2. The most recent character was received longer than four character periods ago(including all start, parity and stop bit)
3. The most recent CPU read of the FIFO was longer than four character periods ago

IrDA

MEGA3 uses the HSDL-3208 IrDA Module. The HSDL-3208 is an ultra-small low cost infrared transceiver module that provides the interface between logic and infrared(IR) signals for through air, serial, half duplex IR data link. The Module is compliant to IrDA physical layer specifications version 1.4 Low Power from 9.6kbit/s to 115.2kbit/s with extended link distance and it is IEC 825-Class 1 eye safe. .

Window material : Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture.

Shape of the Window : From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photo diode. If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side

Selection of Resistor R1Resistor : R1 should be selected to provide the appropriate peak pulse LED current over different ranges of VCC 3.3V and Minimum Peak Pulse Current 50mA.

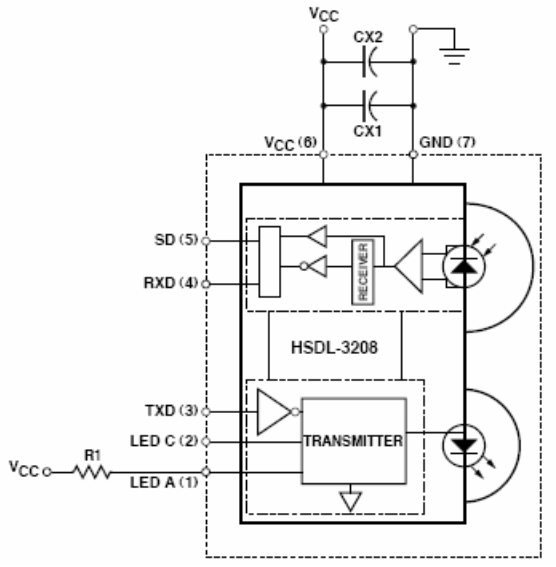


Figure 17. IrDA Block Diagram.

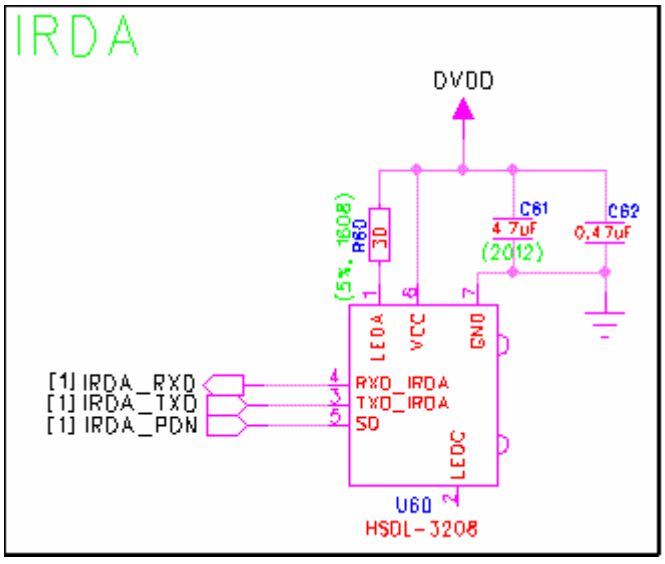


Figure 18. IrDA Circuit.

Read Time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768Khz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor is used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value

reaches a maximum value. The Maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MEGA3, Big Capacitor Battery(BAT300 TS414H) is used for Backup Battery. The Charging Voltage is about 1.5V by VRTC. The CM415DZF1 is a Cristal for 32.768Khz and The C100,C101 must be tuned.

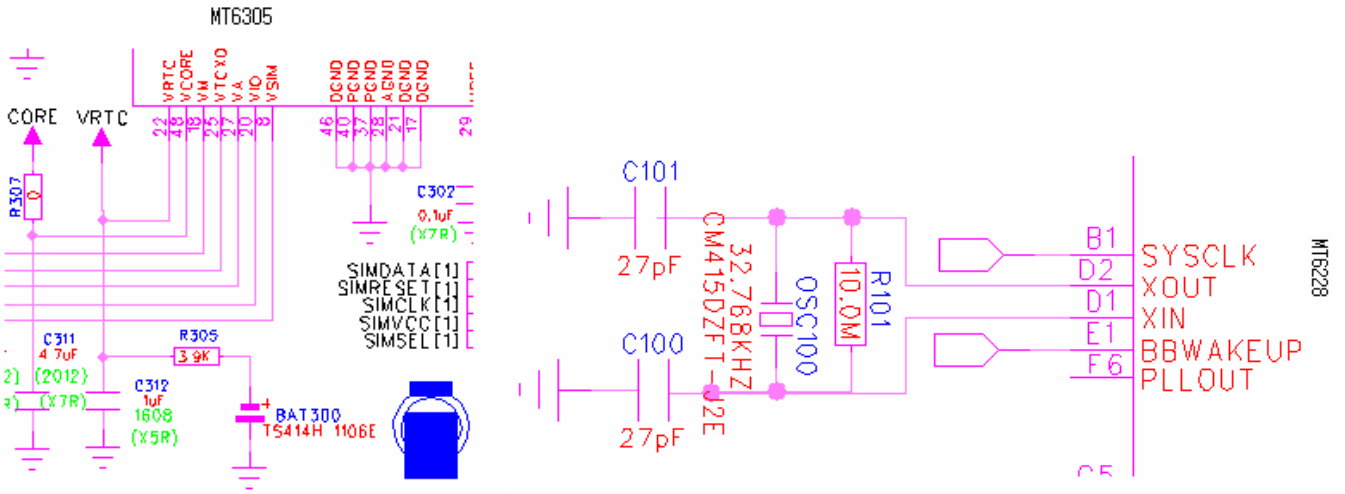


Figure 19. RTC Circuit

Auxiliary ADC Unit

The auxiliary ADC unit is used to monitor the status of battery and charger, identify the plugged peripheral and perform temperature measurement. There provides 7 input channels for diversified application in this unit.

In MEGA3, 6 ADC port are used as shown Figure 20.

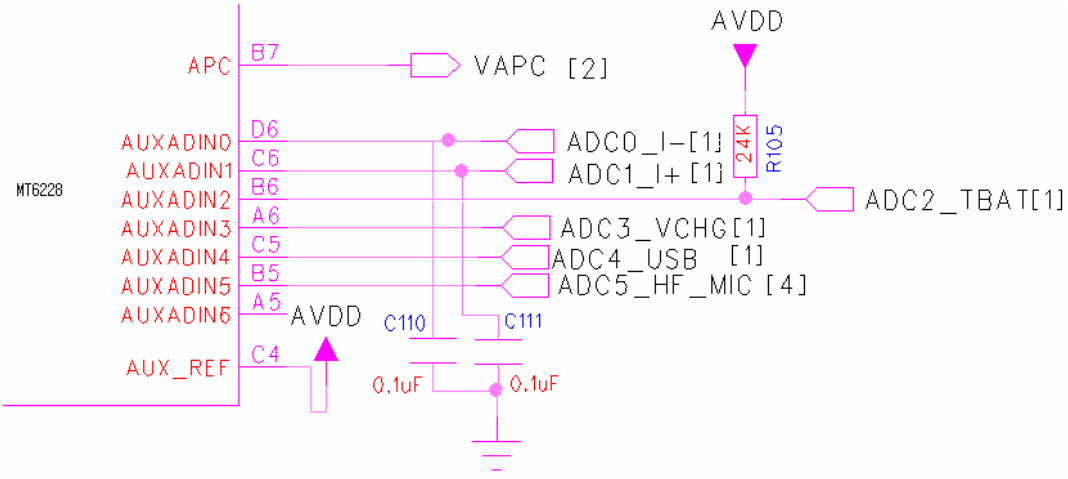


Figure 20. AUXADC Circuit

1) ADC0/1_I-/+ : Check the Battery and Charger voltage.
2) ADC2_TBAT : Connected to battery ID Resistor. Check the Battery Temperature by NTC ID Resistor(10Kohm), So, the voltage is about 0.6V in normal temperature.
3) ADC3_VCHG : Check and detect the the charger. If charger is connected the Voltage is changed from 0V to 1V. So, MT6228 can know the charger inserted.
4) ADC4_USB : Check and detect the USB cable. If USB cable is inserted, voltage of ADC4_USB pin is changed from 2.8V to 0V (2.8V → Pulse → 0V). So, MT6228 can know the USB cable inserted.

5) ADC5_HF_MIC : Check and Detect the Headset(Ear Microphone). If Ear microphone is inserted, the voltage of ADC5_HF_MIC is changed from 2.8V to about 1.5V(1.2~1.8V. depending on CMIC resistance).

5. Multi-Media Subsystem

MT6228 is a highly integrated Baseband/Multimedia single chip. It integrates several hardware-based multimedia accelerators to enable rich multimedia application. Hardware accelerators include Image signal processor, Image resizer, JPEG Codec, MPEG-4 Codec, GIF Decoder, PNG Decoder, 2D graphics engine, TV encoder, and advanced hardware LCD display controller. A lot of attractive multimedia functions can be realized through above hardware accelerators in MT6228. The functions include camera function, JPEG/GIF/PNG image playback, MPEG-4 video recording, MPEG-4 video playback, TV out, 2D graphics acceleration, and so on. Image data paths of multi-media sub-system are shown in Figure 21. Hardware data paths and Image DMA are designed to make data transfer more efficient. MT6228 also incorporates NAND Flash, USB 1.1 OTG Controller and SD/SDIO/MMC/MS/MS Pro Controllers for mass data transfers and storage.

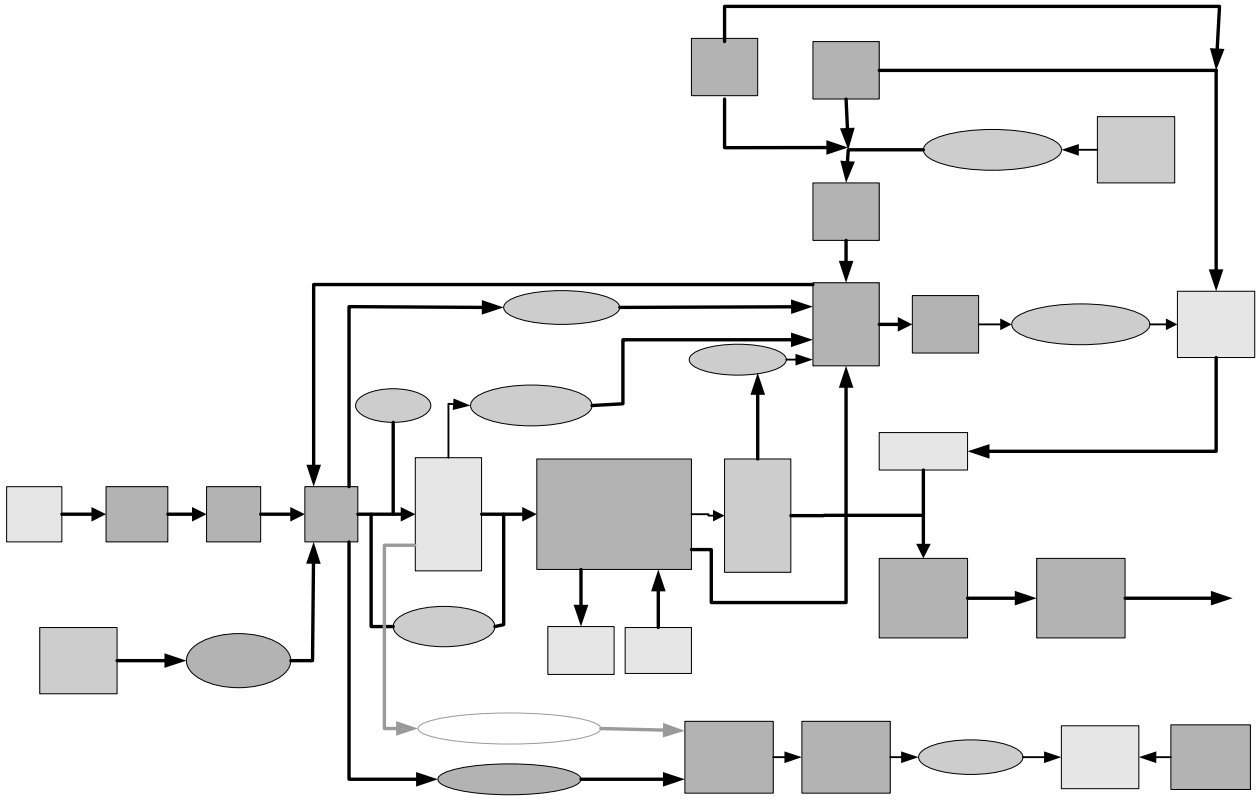


Figure 21. Image Data Path of Multi-media Sub-system

6.1 LCD Interface

MT6228 contains a versatile LCD controller, which is optimized for multimedia applications. This controller supports many types of LCD modules and contains a rich feature set to enhance the functionality.

These features are:

-. Up to 320 x 240 resolution

-. The internal frame buffer supports 8bpp indexed colour, RGB 565, RGB 888 and ARGB 8888 format.

-. Supports 8-bpp (RGB332), 12-bpp (RGB444), 16-bpp (RGB565), 18-bit (RGB666) and 24-bit (RGB888) LCD modules.

-. 6 Layers Overlay with individual colour depth, window size, vertical and horizontal offset, source key, alpha value and display rotation control(90°,180°, 270°, mirror and mirror then 90°, 180° and 270°)

-. One colour look-up table of 24bpp.

For parallel LCD modules, the LCD controller can reuse external memory interface or use dedicated 8/9/16/18-bit parallel interface to access them and 8080 type interface is supported. It can transfer the display data from the internal SRAM or external SRAM/Flash Memory to the off-chip LCD modules. For Parallel LCD Modules, The interface pins are 6pins and 18bit data lines.

-. /LWR : write enable signal.

-. /LRD : read enable signal

-. LPAO : Register select signal. To enter the command and data.

-. /LST : reset signal.

-. /LPCE0/1 : Chip enable signal.

-. NLD00 : 17 : data signal.

MEGA3 LCD uses the Hymax Driver IC HX8312 for 2.2" QVGA, 320x240 pixels 260Kcolors. Also, MEGA3 LCD Module includes the followings.

-. Key pad : soft left/right, OK, Navy key, Send and ESC.

-. Receiver/Vibrator

-. BLU driver IC : A8435.

-. Touch Panel.

MEGA3 can select the Touch Panel by option. The Driver IC is MT6301 from Media Tec.

After s/w downloading, When power on firstly, Phone indicates the Touch Panel calibration with stylus pen, Center, Top Left, Bottom Right coordinates. When Phone is in Sleep mode, If touch the panel, X+ Pin Voltage is changed and Phone is waked up from sleep mode. Also, EINT1_Pen interrupt signal is generated. If touch the Panel, MT6301 read and calculates the X+, Y+ and Z coordinates. Figure 22 is shown the Touch Panel driver IC circuit.

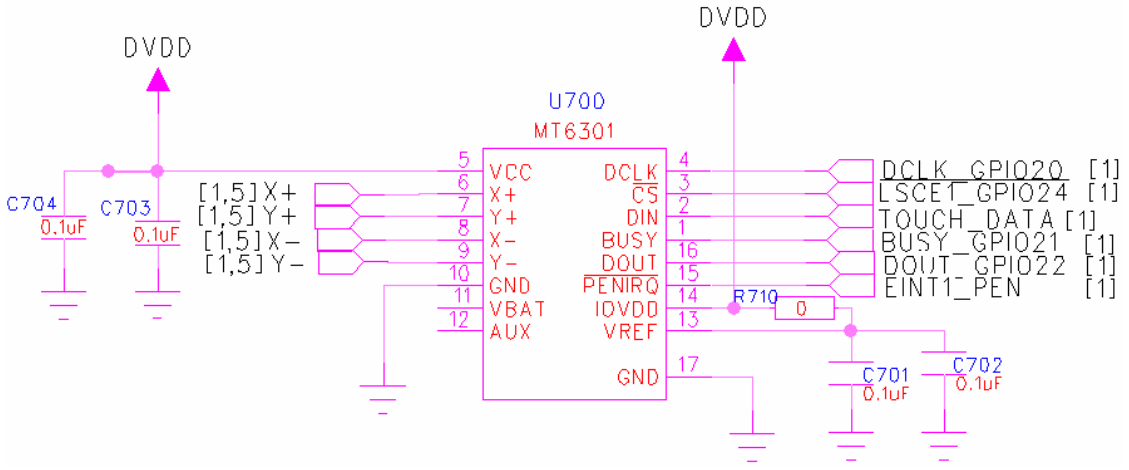


Figure 22. Touch Panel Driver IC circuit.

6.2 NAND Flash interface

MT6228 provides NAND flash interface. The NAND FLASH interface support features as follows:

-. ECC (Hamming code) acceleration capable of one-bit error correction or two bits error detection.

-. Programmable ECC block size. Support 1, 2 or 4 ECC block within a page.

-. Word/byte access through APB bus.

-. Direct Memory Access for massive data transfer.

-. Latch sensitive interrupt to indicate ready state for read, program, erase operation and error report.

-. Programmable wait states, command/address setup and hold time, read enable hold time, and write enable recovery time. -.

-. Support page size: 512(528) bytes and 2048(2112) bytes.

-. Support 2 chip select for NAND flash parts.

-. Support 8/16 bits I/O interface.

-. The NFI core can automatically generate ECC parity bits when programming or reading the device.

-. Used 7 control Signal : NRE#, NEW#,NCE#,NALE, WATCHDOG#,NCLE, NRNB.

In MEGA3, The Nand Flash Memory is used HYC0UGE0MF1P-5SH0E from Hynix. The HYC0UGE0MF1P-5SH0E is Nand Flash(1Gb) + SDRAM (256Mb). The Figure 23 is shown the Circuit diagram. The I/O is 8bit interface from MT6228.

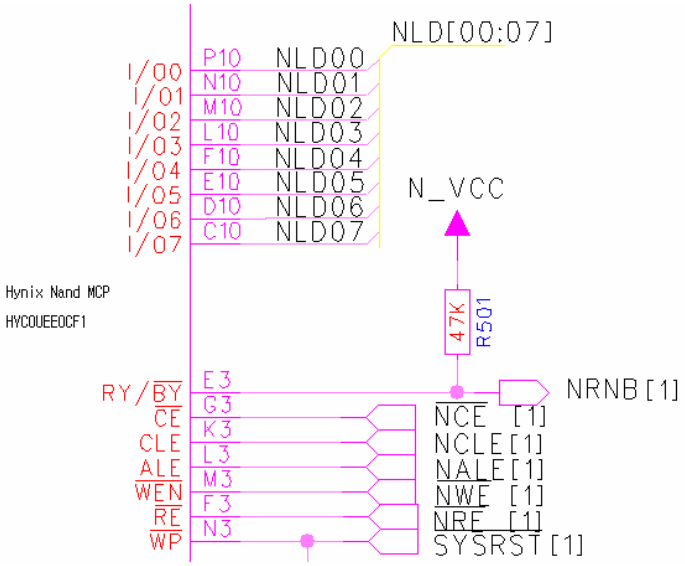


Figure 23. Hynix Nand MCP Circuit Diagram

6.3 USB Device controller

The MT6228 USB OTG controller complies with Universal Serial Bus (USB) Specification Rev 1.1 and USB On-The-Go (OTG) Supplement Rev. 1.0a. The USB OTG controller supports USB device mode, USB simple host mode, as well as OTG handshaking capabilities, at full-speed (12 Mbps) operation. The cellular phone uses this widely available USB interface to exchange data with USB hosts such as a PC or laptop; or to function as a host, allowing it to connect to other devices. When operating in host mode, only a single peer-to-peer (no intermediate hub) connection is supported.

The USB device uses cable-powered feature for the transceiver but only drains little current. An external resistor R42 (nominally 1.5kohm) is required to be placed across Vusb and DP Signal. Two additional external serial resistors(R44,R45)

might be needed to be placed on the output of DP and DM signals to make the output impedance equivalent to 28~44ohm. Also, USB cable can be used to Charger for 5V input. The ADC4_USB is to monitor whether USB cable is inserted or not.

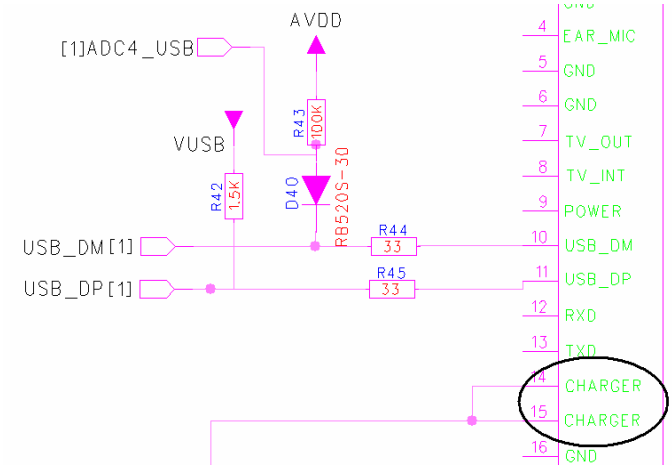


Figure 24. USB Interface Circuit

6.4 Memory Stick and SD Memory Card Controller

The controller fully supports the Memory Stick bus protocol as defined in Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) and the SD Memory Card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 1.0 as well as the MultiMediaCard (MMC) bus protocol as defined in MMC system specification version 2.2. Since SD Memory Card bus protocol is backward compatible to MMC bus protocol, the controller is capable of working well as the host on MMC bus under control of proper firmware. Furthermore, the controller also support SDIO card specification version 1.0 partially. However, the controller can only be configured as either the host of Memory Stick or the host of SD/MMC Memory Card at one time. **MEGA3** is not interfaced Mini SD card but T-Flash Memory Card. Interface Signals are same. Normally, the Detection is controlled by INS pin status. When Card is nothing, The INS is high logically. And When Card inserted, The INS is low.

Pin Assignment.

No.	Name	Type	MMC	SD	MS	MSPRO	Description
1	SD_CLK	O	CLK	CLK	SCLK	SCLK	Clock
2	SD_DAT3	I/O/PP		CD/DAT3		DAT3	Data Line [Bit 3]
3	SD_DAT0	I/O/PP	DAT0	DAT0	SDIO	DAT0	Data Line [Bit 0]
4	SD_DAT1	I/O/PP		DAT1		DAT1	Data Line [Bit 1]
5	SD_DAT2	I/O/PP		DAT2		DAT2	Data Line [Bit 2]
6	SD_CMD	I/O/PP	CMD	CMD	BS	BS	Command Or Bus State
7	SD_PWRON	O					VDD ON/OFF
8	SD_WP	I					Write Protection Switch in SD
9	SD_INS	I	VSS2	VSS2	INS	INS	Card Detection

Card Detection

A dedicated pin “INS” is used to perform card insertion and removal for SD/MMC. The pin “INS” will connect to the pin “VSS2” of a SD/MMC connector. Then the scheme of card detection is the same as that for MS. It is shown Figure 25. In Figure 25, The R115 is connected to GND.

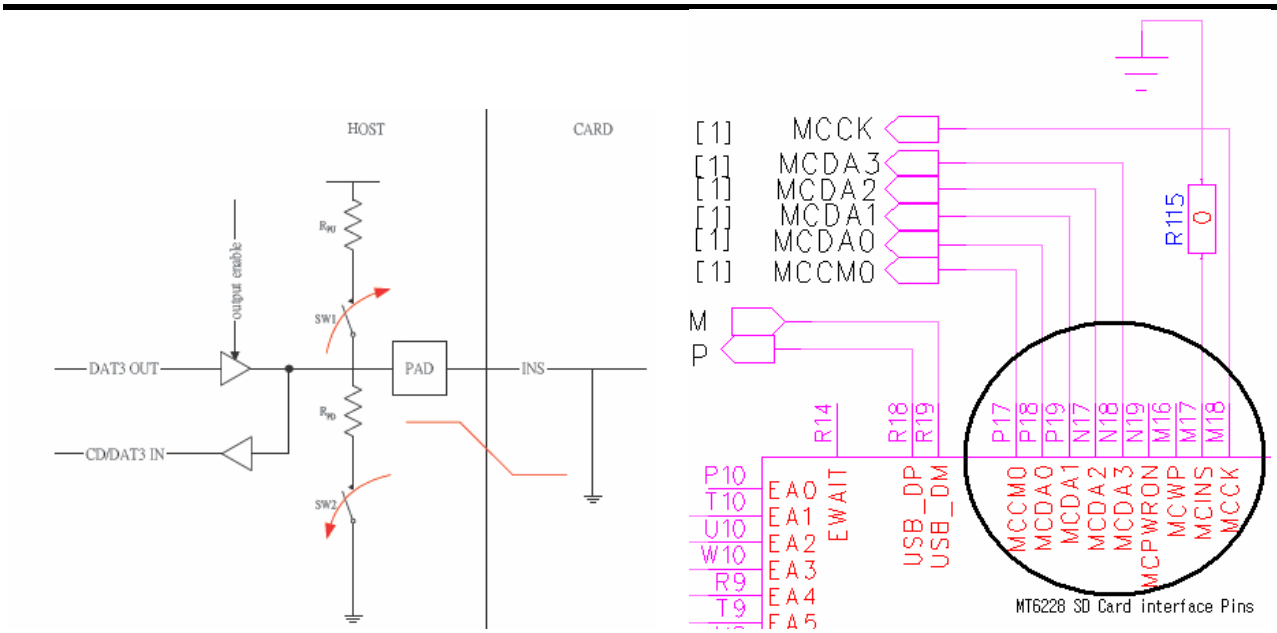
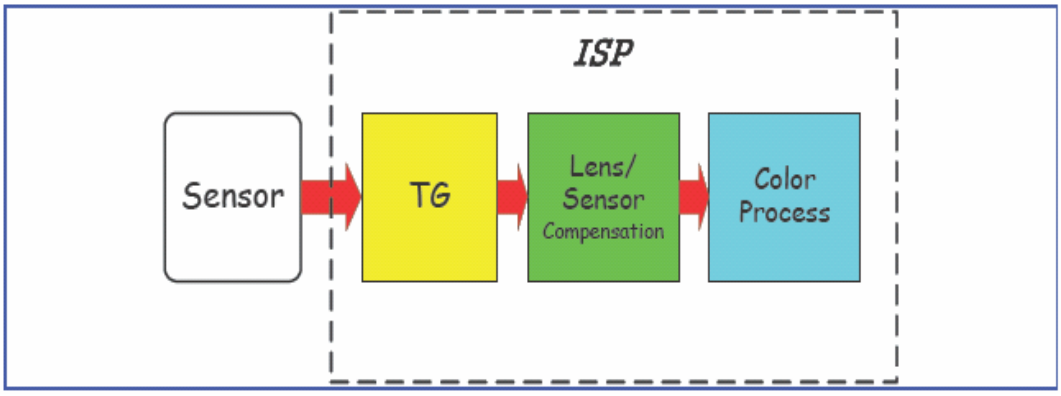


Figure 25. Card Detection.

6.5 Camera Interface



MT6228 incorporates a feature rich image signal processor to connect with a variety of image sensor components. This processor(ISP) consists of timing generated unit (TG) and lens/sensor compensation unit and image process unit. Timing generated unit (TG) cooperates with master type image sensor only. That means sensor should send vertical and horizontal signals to TG. TG offers sensor required data clock and receive sensor Bayer pattern raw data by internal auto synchronization or external pixel clock synchronization. The main purpose of TG is to create data clock for master type image sensor and accept vertical/horizontal synchronization signal and sensor data, and then generate grabbed area of raw data or YUV422/RGB565 data to the lens/sensor compensation unit. Lens/sensor compensation unit generates compensated raw data to the colour process unit in Bayer raw data input mode. In YUV422/RGB565 input mode, this stage is bypassed. Image process unit accepts Bayer pattern raw data or YUV422/RGB565 data that is generated by lens/sensor compensation unit. The output of ISP is YCbCr 888 data format which can be easily encoded by the compress engine (JPEG encoder and MPEG4 encoder). It can be the basic data domain of other data format translation such as R/G/B domain. The ISP is pipelined, and during processing stages ISP hardware can auto extract meaningful information for further AE/AF/AWB calculation. These information are temporary stored on ISP registers or memory and can be read back by MCU.

In MEGA3, Camera Sensors can be selected by BB processor. If MT6228 is used, The Camera Module can be used 3Mpixels sensor from Micron **(MT97012).**, The 2 Power supplies are used(2.8V, 1.8V) and 10bit data interface. The I2C signals need a pull up resistor 10Kohm. The CMMCLK is a 24Mhz and this is strong signal. So, The R32 and C37 used for EMI. Or Can be used the 600ohm bead at 100Mhz.

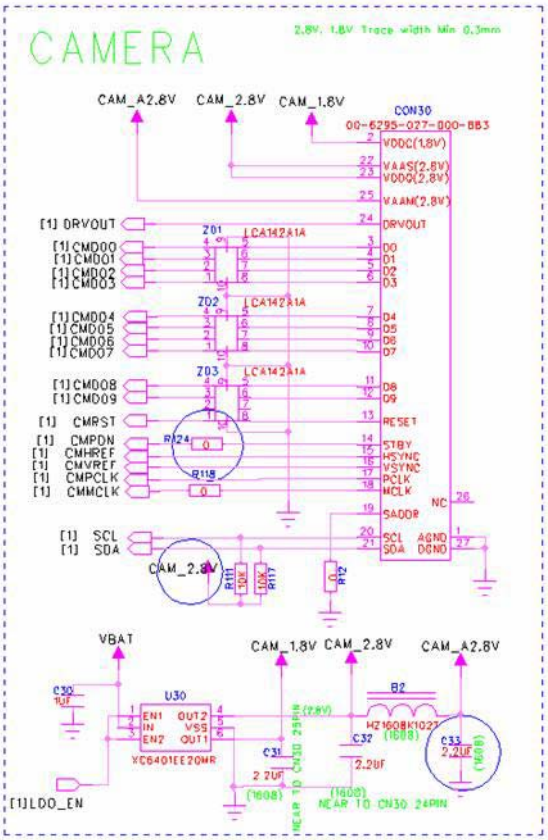


Figure 26. Camera Sensor Interface circuit.

6.6 TV Controller

MT6228 supports NTSC/PAL interlaced TV format. The display function includes two components: a TV controller and a TV encoder. The main functions of the TV controller are as follows:

1. **Fetch the TV frame buffer.** In video playback mode, the source is from the video codec buffer in YUV420 format. In this mode, the TV controller and MPEG4 decoder can also communicate to achieve the best performance. In image playback mode, the source is in RGB565 format. In this mode, still images can be displayed. The LCM controller can direct the image path to the TV controller. When the LCM controller sends frames to the frame buffer as it does for the LCD display, the TV controller retrieves the frames for display.

2. **Scale the frame size to fit the TV size**. MT6228 adopts bilinear interpolation in both horizontal and vertical dimension to scale up the frame. The user can adjust both the location and the size to achieve a suitable appearance.

In NTSC mode, the ideal display area is 720(W) x 480(H), but the actual display area depends on the TV set.

In PAL mode, the ideal display area is 720(W) x 576(H); the actual display area also depends on the TV set. TV frame updates consume a lot of bandwidth. For interlaced system, one frame contains 2 fields. In NTSC mode, the field update rate is 59.94 frames per second (fps); the field update rate in PAL mode is 50 fps. Performance is bound by the size of the source image. The larger the image size, the higher the bandwidth required to support the TV display. The controller

supports an arbitrary image size up to 640 pixels in height and 480 pixels in width. Figure 27 depicts the block diagram of the TV controller and TV Encoder.

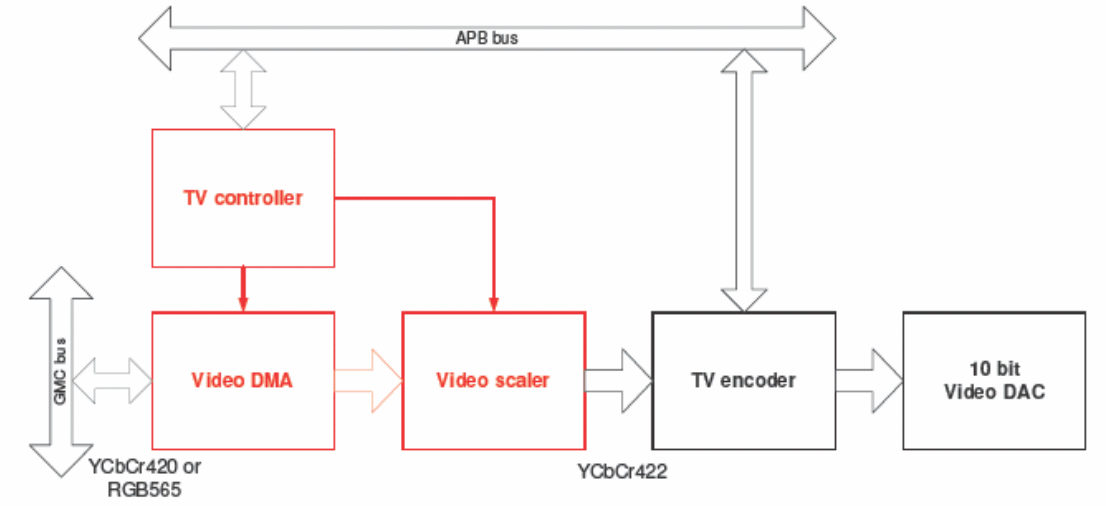


Figure 27. TV controller and Encoder block diagram.

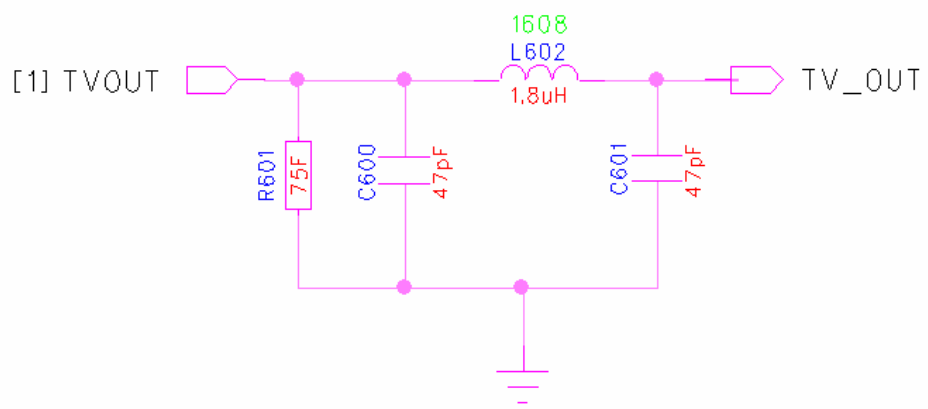


Figure 28. TV out Matching Circuit.

So, MEGA3 has a TV out function. The Figure 28 is a TV out matching circuit. The TV video cable is a 75ohm impedance and connected to I/O Connector CON40. The Audio Line is sharing with Melody Line.

6. Audio Front-End

6.1 Main MIC, Receiver, Headset and OPamp stage.

The audio front-end essentially consists of voice and audio data paths. Figure 29 shows the block diagram of the audio front-end. All voice band data paths comply with the GSM 03.50 specification. Mono hands-free audio or external FM radio playback paths are also provided. The audio stereo path facilitates CD-quality playback, external FM radio, and voice playback through a headset. In MEGA3, The Voice in normal mode is output to AU_Out0_N/P and voice in Headset Mode/Loud Mode is output to AU_MOUTL/R . The Melody in Normal mode/Headset Mode is output to AU_MOUTL/R.

The Mic input in normal mode/Loud mode is to AU_VIN0_N/P and Mic input in headset mode is to AU_VIN1_N/P.

The below tables are shown the PGA gains of Mic, Voice and Melody. And the S/W control gain can be changed in Debug Mode using *#110*01# → Audio → Normal mode/Headset Mode/Loud Mode.

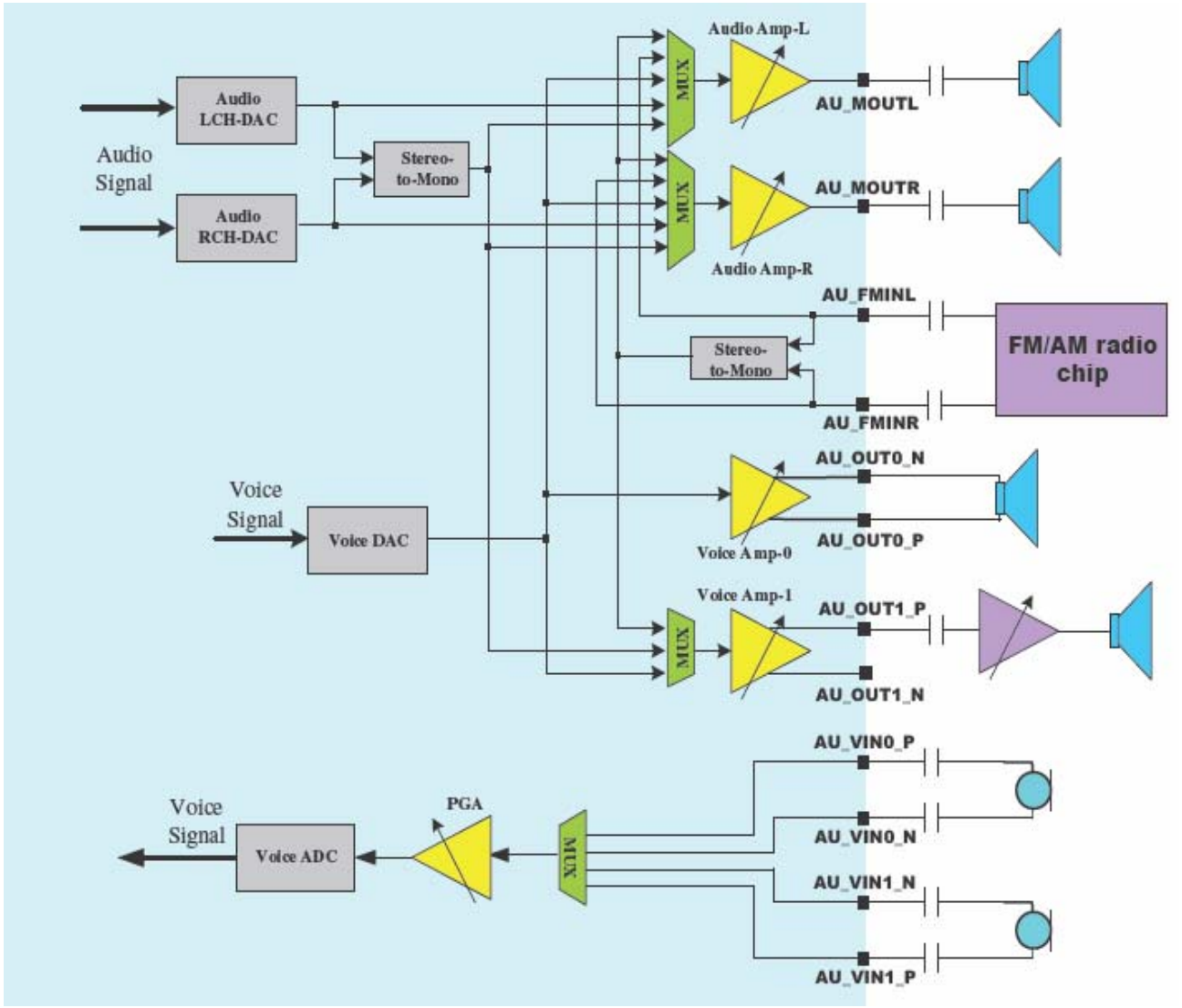


Figure 29. Audio Front-End Block Diagram

	Uplink PGA gain	Downlink PGA gain	
		Audio Amp L/R	Voice Amp 0/1
Step size	2dB	3dB	2dB
Tunable Range	-20~42dB	-22~23dB	-22~8dB
0dBm0	0.2Vrms	0.6Vrms	0.6Vrms

Engineer mode	Microphone	Melody	Speech
Tunable Range	0~255	0~255	0~255
Step size	8 (2dB)	16 (3dB)	16 (2dB)

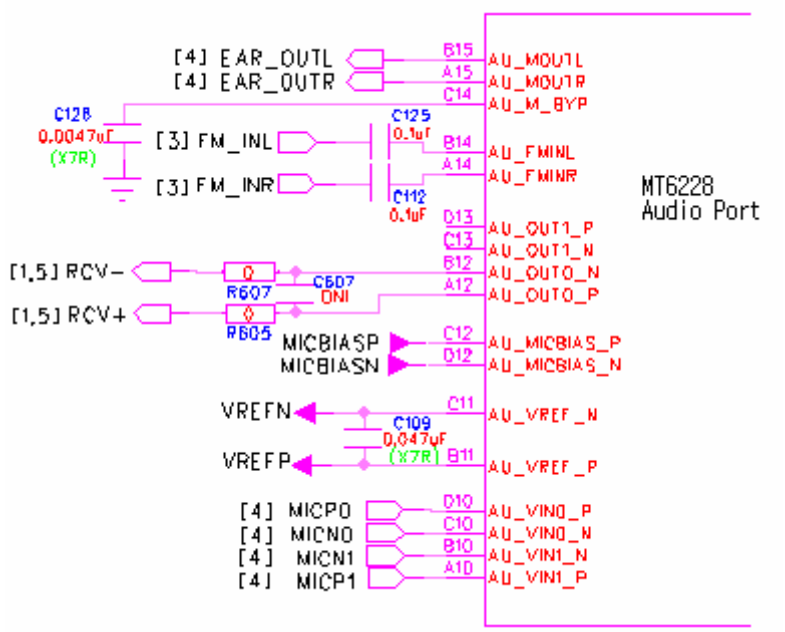


Figure 30. MT6228 Audio Port circuit diagram.

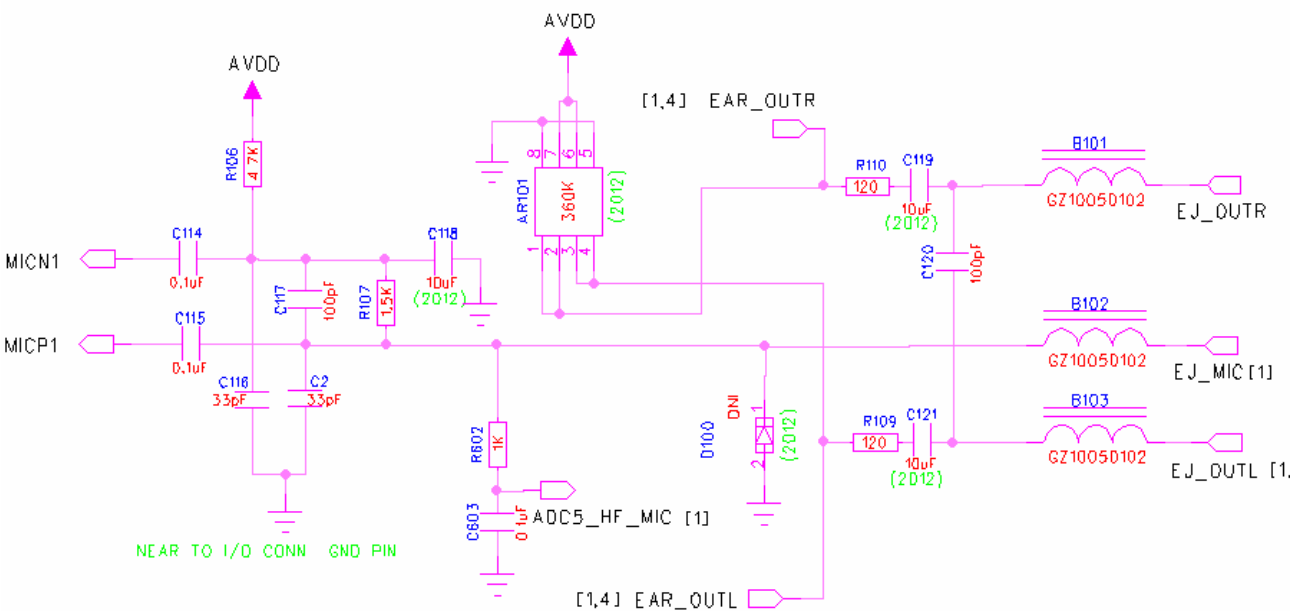


Figure 31. Headset Circuit diagram.

The Figure 31 is shown the Headset Circuit diagram. EJ_Mic is input and EJ_OUTR(L) is output.

The B101,102,103 is a 1Kohm bead at 100Mhz. These are important for FM Radio Blocking of 100Mhz and must be placed to near by Headset connector. Also, has a good performance for EMI. Because The FM Radio Ant is connected to EJ_OUTL. The ADC5_HF_MIC is for hook switch of Headset. If Hook is pressed, The ADC5_HF_MIC voltage is changed from 2.8V to 0V.

The Figure 32 is shown the OPAmp circuit. The D-Class OPAmp was used which has a good PSRR for 217 GSM burst noise. The Output gain is 9 times by R600 and R603 resistor.

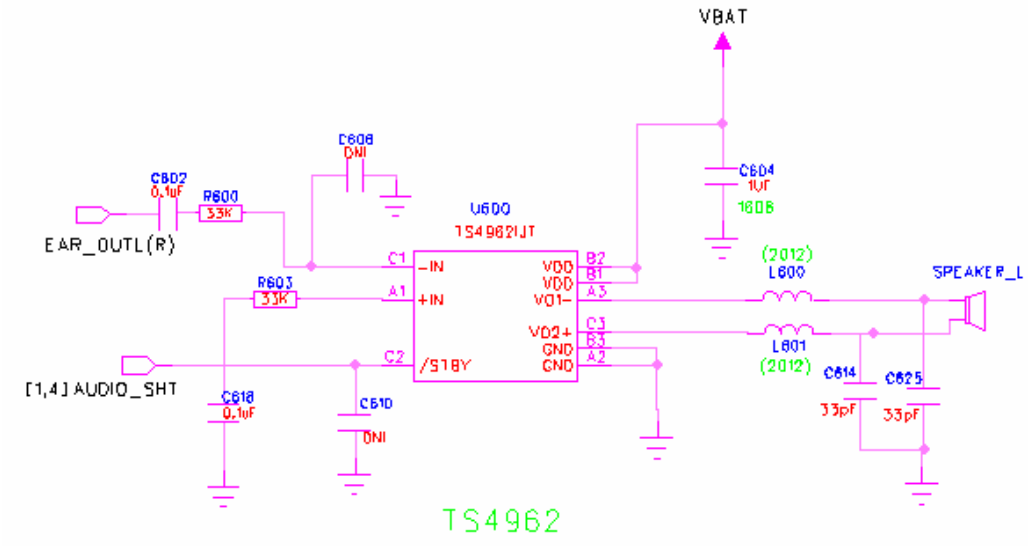


Figure 32. Audio Amp Circuit Diagram.

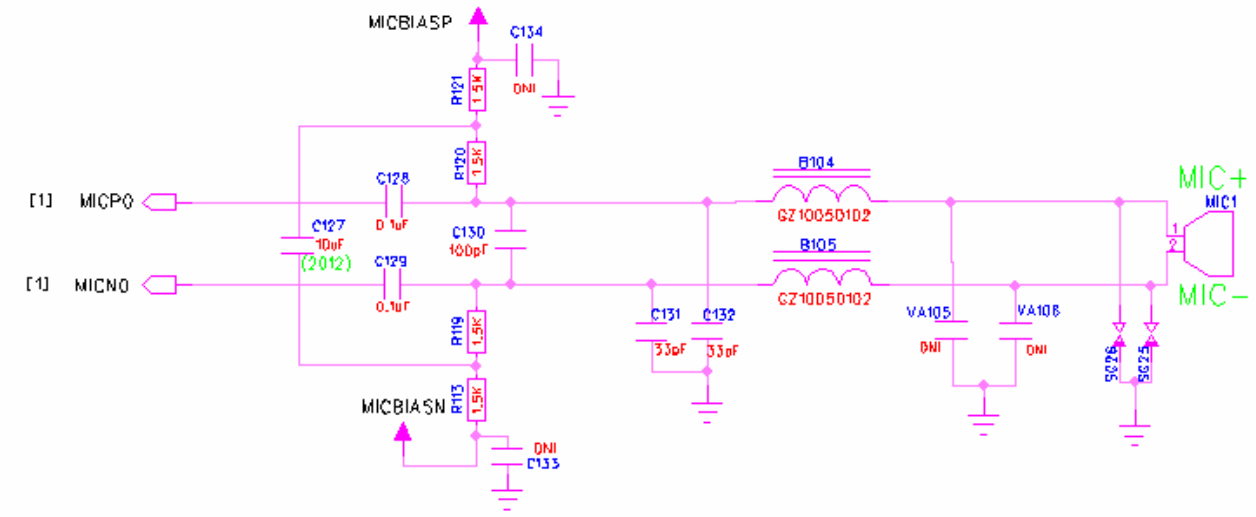


Figure 33. Mic Circuit diagram.

6.2 Blue Tooth Stage

Also, MT6228 has a Digital Audio Interface(DAI) block to communicate with the System Simulator for FTA or external Bluetooth module for particular applications. The digital filter block performs filter operations for voice band and audio band signal processing.

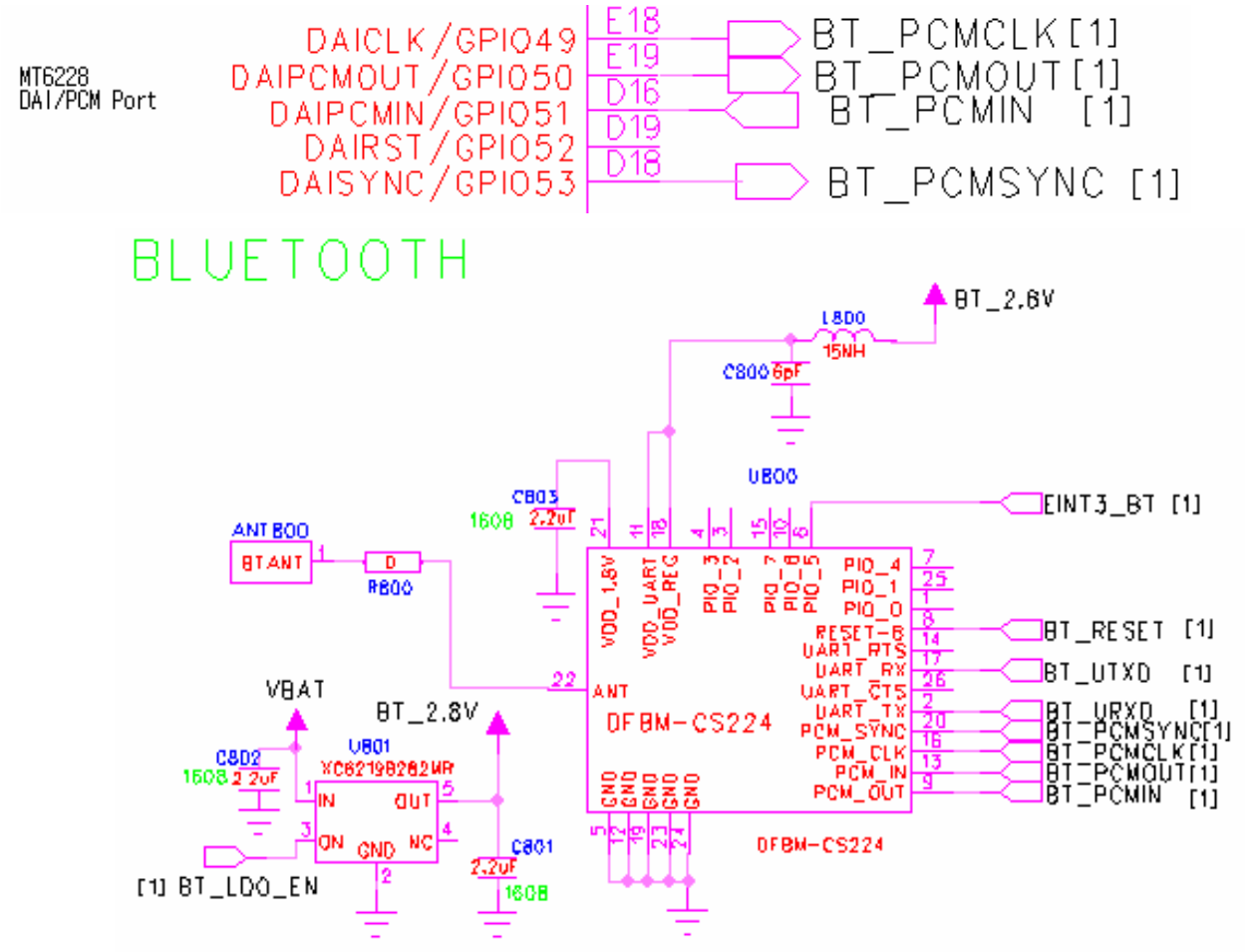


Figure 33. The digital circuits for Audio Front-End

The Below table is shown the MT6228 DAI/PCM Port mapping according to S/W concept.

PIN NAME	DAI	PCM	EDI
DAI_CLK (OUTPUT)	DAI_CLK	PCM_CLK	EDI_CLK
DAI_TX (OUTPUT)	DAI_TX	PCM_OUT	EDI_DAT
DAI_RX (INPUT)	DAI_RX	PCM_IN	
BT_SYNC (OUTPUT)	-	PCM_SYNC	EDI_WS

The BT Module is used CS224 from Delta and BTVZ0502SA from Samsung. The BT Version is 1.2 and Nominal Power is 0dBm and Sensitivity is about -80dBm. The distance during communication for Voice and Audio is around 13meter.

BT Chip is BlueCore 3.So, If BT headset has a CSR Chip set, The paring is no problem. The BT Test is certificated in BQB.

6.3 FM Radio Stage.

MEGA3 Also, has a FM Radio chip set MT6188 from Media Tek. The interface is very simple. The FM_X1 frequency can be used 32Khz, 13Mhz and 26Mhz. The FM_X1 is from MT6228 GPIO port can be used for Oscillator output. The L80 is to tune the FM Radio band Q. Since the Headset is used for FM Radio Receiver and ANT. So, The Headset Receiver GND line must be connected to GND via bead L40(22uH). If the Headset Receiver GND is connected to Power GND, The white noise is increased.

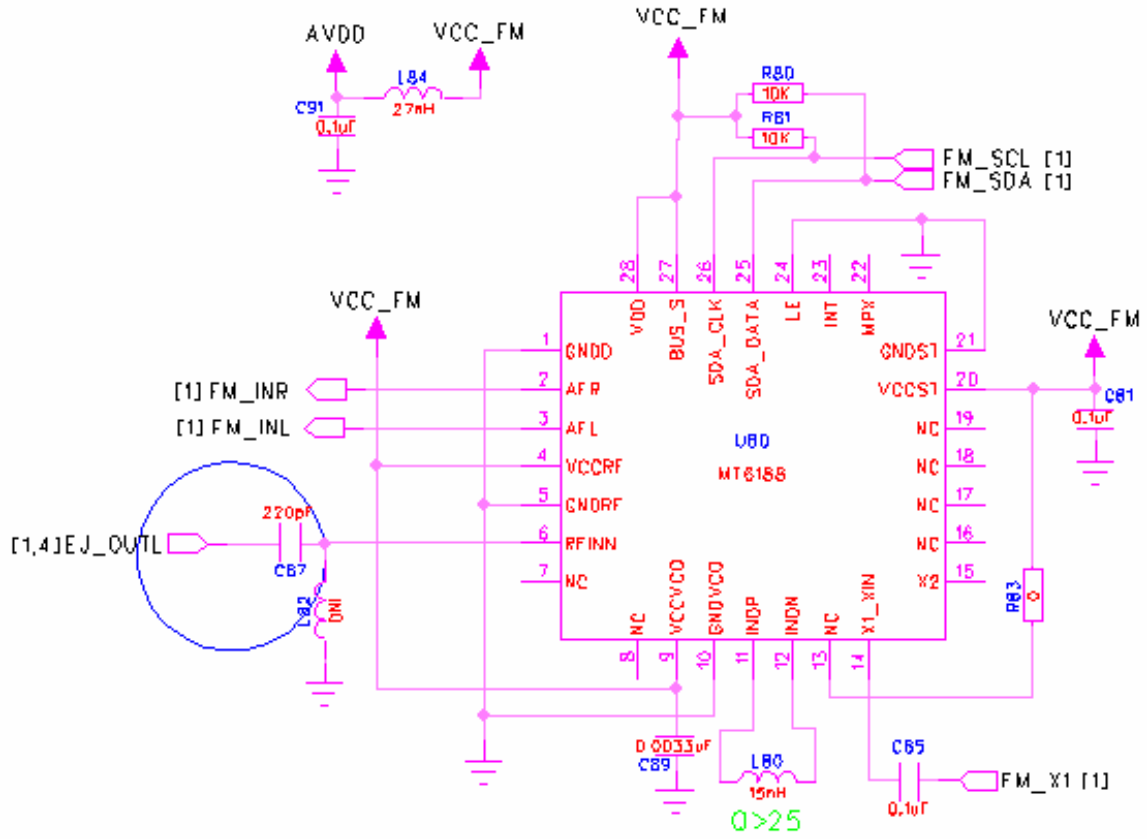


Figure 34. FM Radio Circuit diagram.

7. Radio Interface Control

This chapter details the MT6228 interface control with the radio part of a GSM terminal. Providing a comprehensive control scheme, the MT6228 radio interface consists of Baseband Serial Interface (BSI), Baseband Parallel Interface (BPI), Automatic Power Control (APC) and Automatic Frequency Control (AFC), together with APC-DAC and AFC-DAC.

7.1 Baseband Serial Interface

The Baseband Serial Interface controls external radio components MT6120. A 3-wire serial bus transfers data to RF circuitry for PLL frequency change, reception gain setting and other radio control purposes. In this unit, BSI data registers are double-buffered in the same way as the TDMA event registers. The user writes data into the write buffer and the data is transferred from the write buffer to the active buffer when a TDMA_EVTVAL signal(from the TDMA timer) is pulsed.

The unit has four output pins : BSI_CLK is the output clock, BSI_DATA is the serial data port and BSI_CS0,BSI_CS1 are the select pins for 2 external components. These outputs are connected to MT6120 Transceiver to program.

Baseband Parallel Interface

The Baseband Parallel Interface features a 10-pin output bus used for timing-critical control of the external circuits. These pins are typically used to control front-end components at the specified time along the GSM time-base, such as transmit-enable(PA_EN), band switching(BANDSW_DCS), FEM-switch(LB_TX, HB_TX), etc.

The following table is shown the used pin for RF part.

Pin Name	Pin Description	Description	Component
BPI_BUS 0	HB_TX	Switch Module DCS/PCS TX	Switch Module(LMSP54HA)
BPI_BUS 1	LB_TX	Switch Module GSM TX	Switch Module(LMSP54HA)
BPI_BUS 2	PCS	Switch Module PCS RX	Switch Module(LMSP54HA)
BPI_BUS 4	PA_EN	PAM Enable	PAM (RF3166)
BPI_BUS 5	BANDSW_DCS	Band switch for DCS	PAM (RF3166)
BPI_BUS 8	BT_LDO_EN	Blue Tooth Power Supply Enable	BTM(CR222)
BPI_BUS 9	RFVCOEN	RF VCO Enable	Transceiver(MT6120)

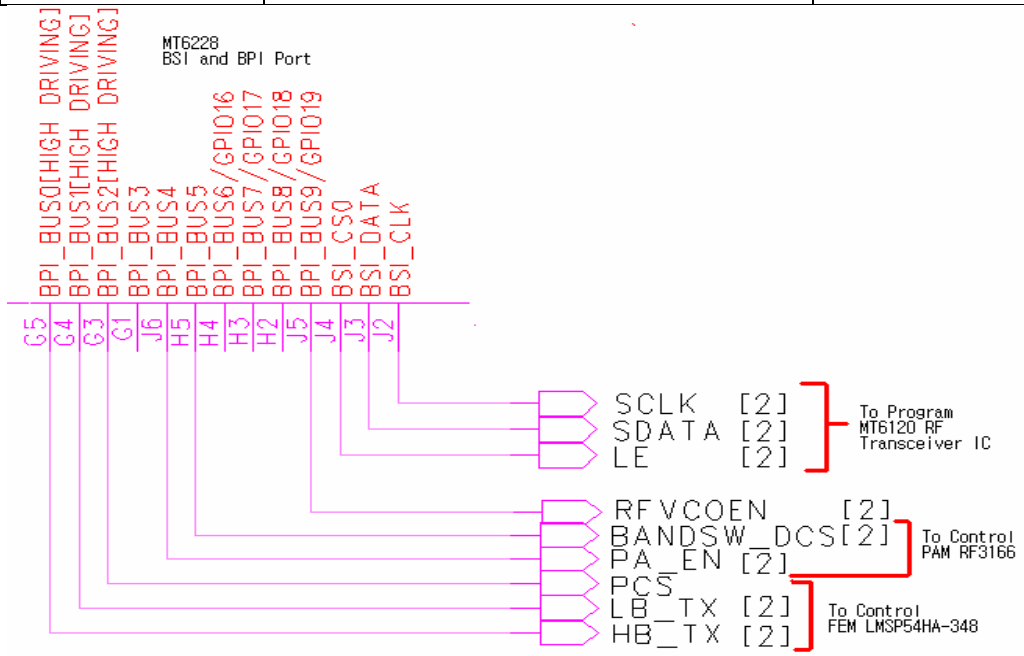


Figure 35. BSI and BPI Circuit diagram.

Automatic Power Control Unit

Automatic Power Control unit is used to control the Power Amplifier module. Through APC unit, we can set the proper transmit power level of the handset and to ensure that the burst power ramping requirements are met. In one TDMA frame, up to 7 TDMA events can be enabled to support multi-slot transmission. In practice, 5 banks of ramp profiles are used in one frame to make up 4 consecutive transmission slots.

The shape and magnitude of the ramp profiles are configurable to fit ramp-up, intermediate ramp, and ramp-down profiles. Each bank of the ramp profile consists of 16 8-bit unsigned values, which is adjustable for different conditions.

The entries from one bank of the ramp profile are partitioned into two parts, with 8 values in each part. In normal operation, the entries in the left half part are multiplied by a 10-bit left scaling factor, and the entries in the right half part are multiplied by a 10-bit right scaling factor. Those values are then truncated to form 16 10-bit intermediate values. Finally the intermediate ramp profile are linearly interpolated into 32 10-bit values and sequentially used to update to the D/A converter.

The APC Analog Signal is inputted to Power Amplifier Module through Low Pass filter (R400,R401,C406)

The APC Analog Signal has 32 Ramp profiles for Up Ramp and Down Ramp each 16 profiles as shown below.

TX power level=44,53,62,74,90,110,136,165,200,240,295,350,420,525,610,610

(Voltage Level according to TX Power GSM Level 19 ~ 5. DCS/PCS Level 15~0)

profile 0 ramp up=0,0,0,0,0,0,2,4,8,26,65,143,228,255,255,255

profile 0 ramp down=255,255,239,197,138,78,32,10,0,0,0,0,0,0,0,0

.

.

profile 15 ramp up=0,0,0,0,0,0,0,2,4,8,26,65,143,219,250,255

profile 15 ramp down=255,239,197,138,78,32,10,0,0,0,0,0,0,0,0,0

The Figure 36 shows the Timing Mask for Normal VAPC.

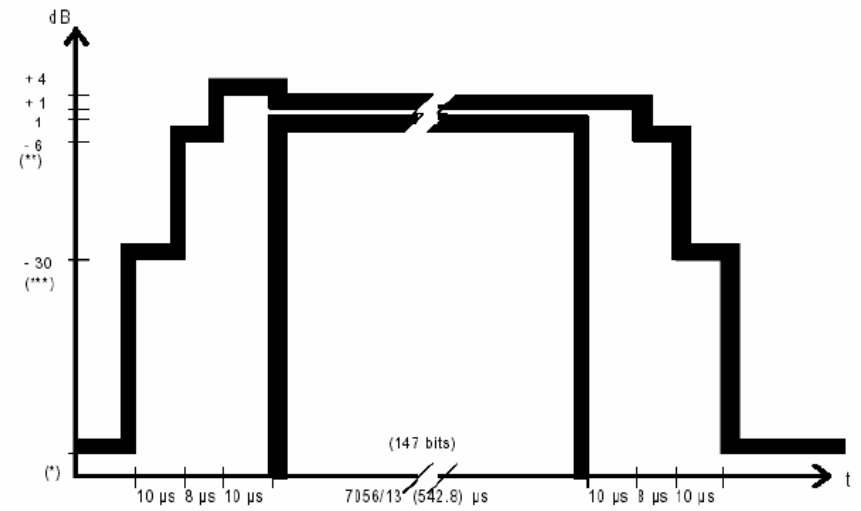


Figure 36. Timing Mask for normal VAPC.

Automatic Frequency Control Unit

Automatic Frequency Control unit provides the direct control of the oscillator for frequency offset and Doppler shift compensation. It utilizes a 13-bit D/A converter to achieve high-resolution control. The AFC is always inputted to VCTCXO to generate 26Mhz. The AFC Voltage must be calibrated to tune the VCTCXO to generate 26Mhz to be entered the MT6120 and MT6228 Main system clock. If the VCTCXO output a frequency with much ppm , The Frequency error and Phase error are out of range. After calibrated, The Analog voltage is about 1.5V and AFC_DAC is about 4200 decimally.

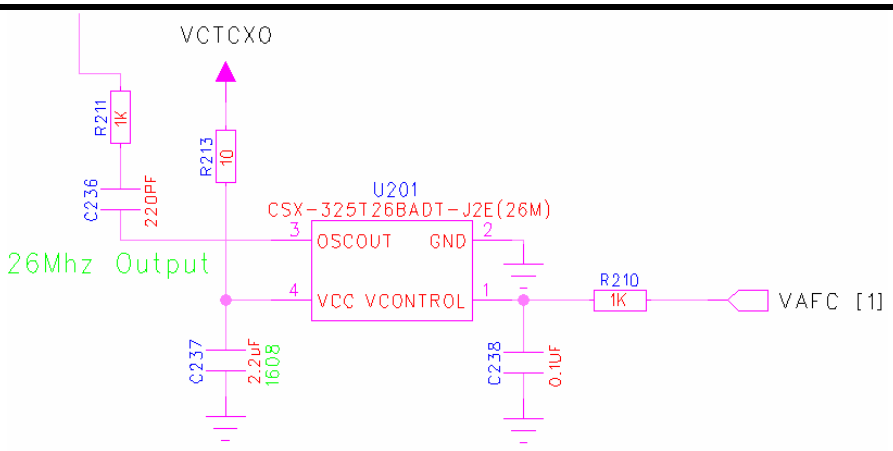


Figure 37. The AFC and VCTCXO Circiut diagram

8. Clocks and Reset

Clocks

There are two major time bases in the MT6228. For the faster one is the 13MHz clock origination from an off-chip temperature-compensated voltage controlled oscillator that can be 26MHz. This signal is the input from the SYSCLK pad then is converted to the square-wave signal. The other time base is the 32.768KHz clock generated by an on-chip oscillator connected to an external crystal.

- 32.768Khz Time Base

The 32.768Khz clock is always running. It's mainly used as the time base of the Real Time Clock(RTC) module, which maintains time and date with counters. In low power mode, the 13Mhz time base is turned off, so the 32.768Khz clock shall be employed to update the critical TDMA timer and Watchdog timer. This Time base is also used to clock the keypad Scanner logic. The C101,C102 must be tuned with Oscillator.

- 13Mhz Time Base

Two 1/2-dividers, one for MCU Clock and the other for DSP Clock, exist to allow usage of either 26 or 13Mhz TXVCXO as clock input. There phase-locked loops(MPLL, DPLL and UPLL) are used to generate three primary clocks.

MPLL : Provides the MCU System Clock.

DPLL : Provides the DSP System Clock. DPLL can be programmed to provide 1x to 6x output of the 13Mhz reference.

UPLL : Provides the USB System Clock.

Reset Generation Unit

Figure 38 shows reset scheme used in MT6228. There are three kinds of resets in the MT6228, i.e., hardware reset, watchdog reset, and software resets.

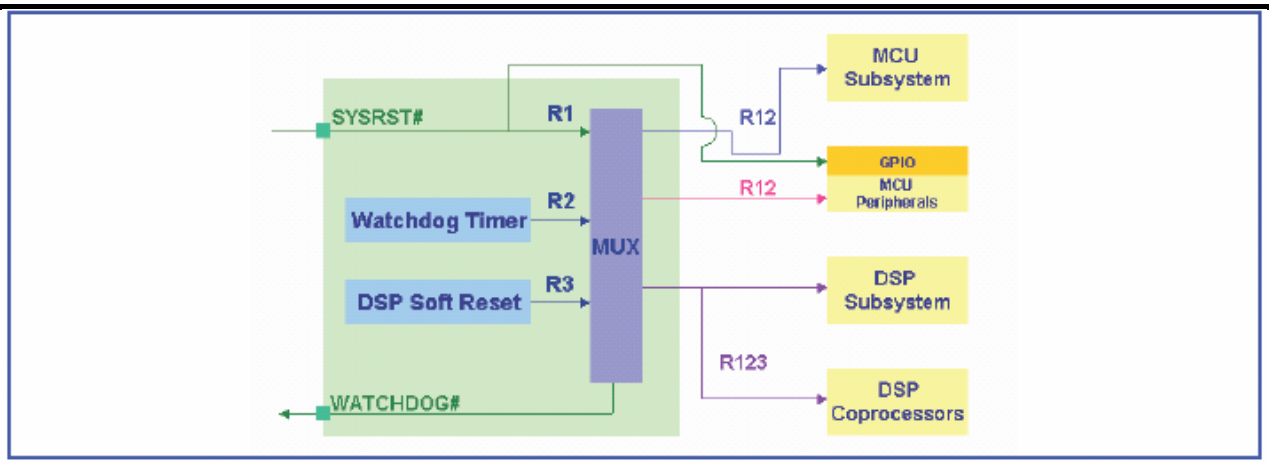


Figure 38. Reset Scheme used in MT6228

- Hardware Reset

This Reset is inputted through the SYSRST# pin from PMIC(MT6318 Pin 24). The SYSRST# shall be driven to low during power-on. The Hardware reset has a global effect on the chip. It initializes all digital and analog circuits except the RTC. Refer to the listed below.

- All Analog Circuits are turned off
- All PLLs are turned off and bypassed. The 13Mhz system clock is the default time base.
- Special Trap statue in GPIO.

- Watchdog Reset

A Watchdog reset is generated when the Watchdog timer expires as the MCU software failed to re-program the timer counter in time. Hardware blocks that are affected by the watchdog reset are :

- MCU Subsystem
- DSP Subsystem
- External Component (By software program)

- Software Reset

These are local reset signals that initialize specific hardware. For example, The MCU or DSP software may write to software reset trigger registers to reset hardware modules to their initial states, when hardware failures are detected. The following Modules has software resets

- DSP Core
- DSP Coprocessors.

II. MT6318 (GSM Power Management System)

The MT6318 is a power management system chip optimized for GSM/GPRS handsets, especially those based on the MediaTek

MT621x/MT622x system solution. MT6318 contains 11 LDOs, one to power each of the critical GSM/GPRS sub-blocks

Sophisticated controls are available for power-up during battery charging, for the keypad interface, and for the RTC alarm.

The MT6318 is optimized for maximum battery life.

The 2-step RTC LDO design allows the RTC circuit to stay alive without a battery for several hours.

The MT6318 battery charger can be used with a lithium-ion (Li+) battery.

The SIM interface provides the level shift between SIM card and microprocessor.

The MT6318 is available in a 96-pin TFBGA package.

The operating temperature range is -25°C to +85°C.

The interface Features are listed below.

- Handles all GSM/GPRS Baseband Power Management
- Input range: 2.8 V ~ 5.0 V
- Charger input of up to 15 V
- 11 LDOs optimized for specific GSM/GPRS subsystems
- 2-step RTC LDO
- 600 mW Class AB audio amplifier
- Booster for series backlight LED driver
- Charge pump for parallel backlight LED driver
- SPI interface
- Pre-charge indication
- Li-ion battery charge function
- SIM card interface
- RGB LED driver
- V_{core} for power-saver mode
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Power-on reset and start-up timer
- 96-pin TFBGA package

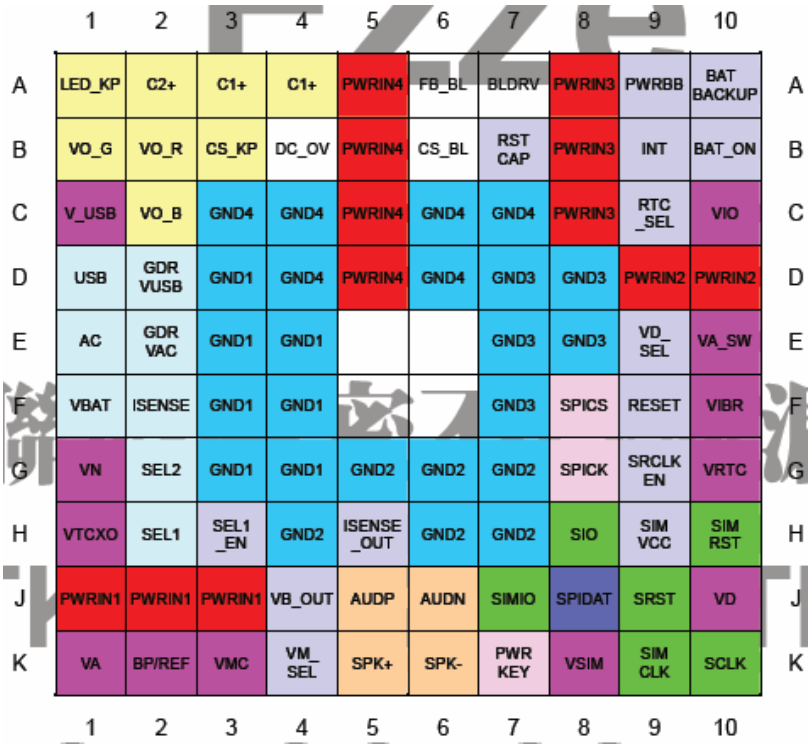


Figure 40. MT6318 Pin configuration.

	Pin	Symbol	I/O/A	Description
Control	K7	PWRKEY	I	Power on button input. Active low.
	A9	PWRBB	I	Power on/off from microprocessor. Active high.
	G9	SRCLKEN	I	VTCXO and VA enable. High = enable. Low = disable
	H9	SIMVCC	I	VSIM enable. High = enable. Low = disable.
	B10	BAT_ON	I	Indication that Li-ion battery is inserted. High = no battery. Low = battery inserted.
	B4	DC_OV	I	DC/DC protection input. OV threshold voltage is 1V.
	K4	VM_SEL	I	External memory supply selection. 1 = 2.8V, 0 = 1.8V.
	H3	SEL1_EN	I	Enable the "pre-charge indication" function. 1 = enable, 0 = disable. (Note1)
	C9	RTC_SEL	I	VRTC output voltage selection. 1 = 1.5V, 0 = 1.2V (Note1)
	E9	VD_SEL	I	VD output voltage selection. 1 = 1.8V/1.5V, 0 = 1.2V/0.9V
Charger Control	E1	AC	IA	AC-DC adaptor input
	D1	USB	IA	USB power input
	C1	V_USB	OA	3.3V USB power output
	B9	INT	O	Interrupt PIN. Active low.
	D2	GDRVUSB	OA	Control output to the gate of the external p-channel FET for the USB charger.
	E2	GDRVAC	OA	Control output to the gate of the external p-channel FET for the AC charger.
	F2	ISENSE	OA	Charger current sensing input
	H2	SEL1	OA	Control output to the gate of the external PMOS for the AC charger input as power source.
	G2	SEL2	OA	Control output to the gate of the external PMOS for the VBAT input as power source.
SIM Interface	J7	SIMIO	I/O	Non level-shifted SIM data (3V)
	H10	SIMRST	I	Non level-shifted SIM reset input (3V)
	K9	SIMCLK	I	Non level-shifted SIM clock input (3V)
	H8	SIO	I/O	Level-shifted SIM data (1.8/3V)
	J9	SRST	O	Level-shifted SIM reset output (1.8/3V)
	K10	SCLK	O	Level-shifted SIM clock output (1.8/3V)
Reset	B7	RSTCAP	IA	Reset delay time capacitance
	F9	RESET	O	System reset. Low active.
Power-Related	F1	VBAT	IA	Battery input voltage
	J1, J2, J3, D9, D10, A8, B8, C8, A5, B5, C5, D5	PWRIN	IA	Power input
	J4	VB_OUT	OA	Battery output voltage. Switchable.
	H5	ISENSE_OUT	OA	ISENSE output voltage. Switchable.
	K2	BP/VREF	OA	Bandgap reference and bypass capacitance
	D3, E3, E4, F3, F4, G3, G4, G5, G6, G7, H4, H6, H7, D7, D8, E7, E8, F7, C3, C4, C6, C7, D4, D6	GND		Ground
	J10	VD	OA	Digital core supply
	C10	VIO	OA	Digital IO supply

	K1	VA	OA	Analog supply
	E10	VA_SW	OA	Auxiliary analog supply. Switchable.
	H1	VTCXO	OA	TCXO supply
	G1	VM	OA	Memory supply
	K8	VSIM	OA	SIM supply
	G10	VRTC	OA	RTC supply
	K3	VMC	OA	Memory card supply
Miscellaneous	F10	VIBR	OA	Vibrator driver
	A3	C1+	A	Charge pump capacitor. Positive terminal.
	A4	C1-	A	Charge pump capacitor. Negative terminal.
	A2	C2+	A	DC/DC output back-up capacitor. Positive terminal.
	A10	BAT_BACKUP	OA	Backup battery pin for 2-step RTC
Speaker Amplifier	J5	AUDP	IA	Audio positive input
	J6	AUDN	IA	Audio negative input
	K5	SPK+	OA	Speaker positive output
	K6	SPK-	OA	Speaker negative output
LED Driver	B2	VO_R	IA	R LED current driver
	B1	VO_G	IA	G LED current driver
	C2	VO_B	IA	B LED current driver
	A1	LED_KP	OA	KP LED driver
	B3	CS_KP	IA	KP LED current sensor
	A7	BLDRV	OA	Control output to the gate of the external FET for the backlight DC-DC converter.
	B6	CS_BL	IA	Voltage sensor input for external BL FET current
	A6	FB_BL	IA	Voltage sensor input from white LED ballast resistor
SPI Interface	F8	SPICS	I	Serial port select input
	G8	SPICK	I	Serial port clock input
	J8	SPIDAT	IO	Serial port I/O

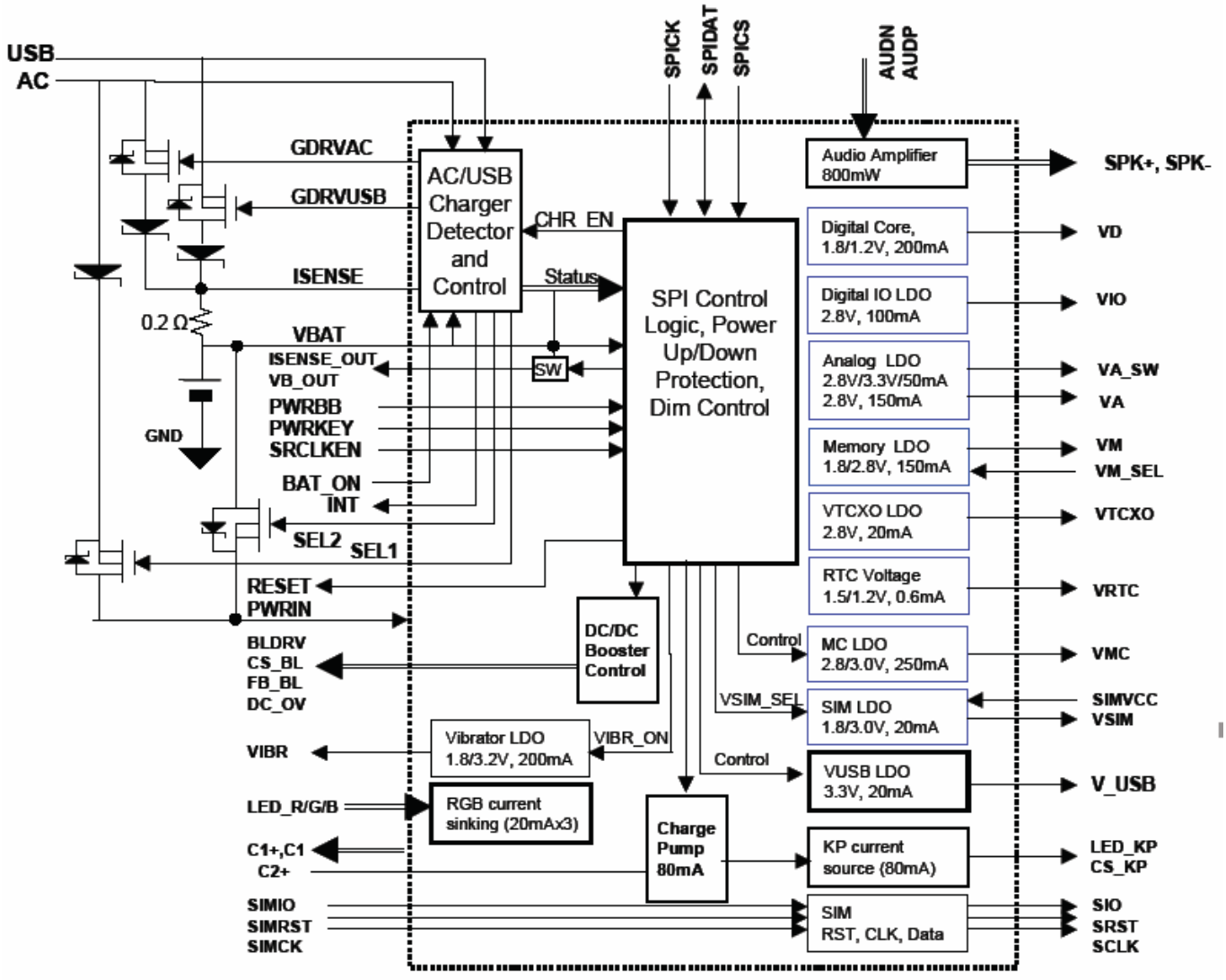


Figure 41. Functional Block Diagram of MT6318

1. Charger Circuit

The charger circuit in PMIC is mainly comprised of 3 sub-functions.

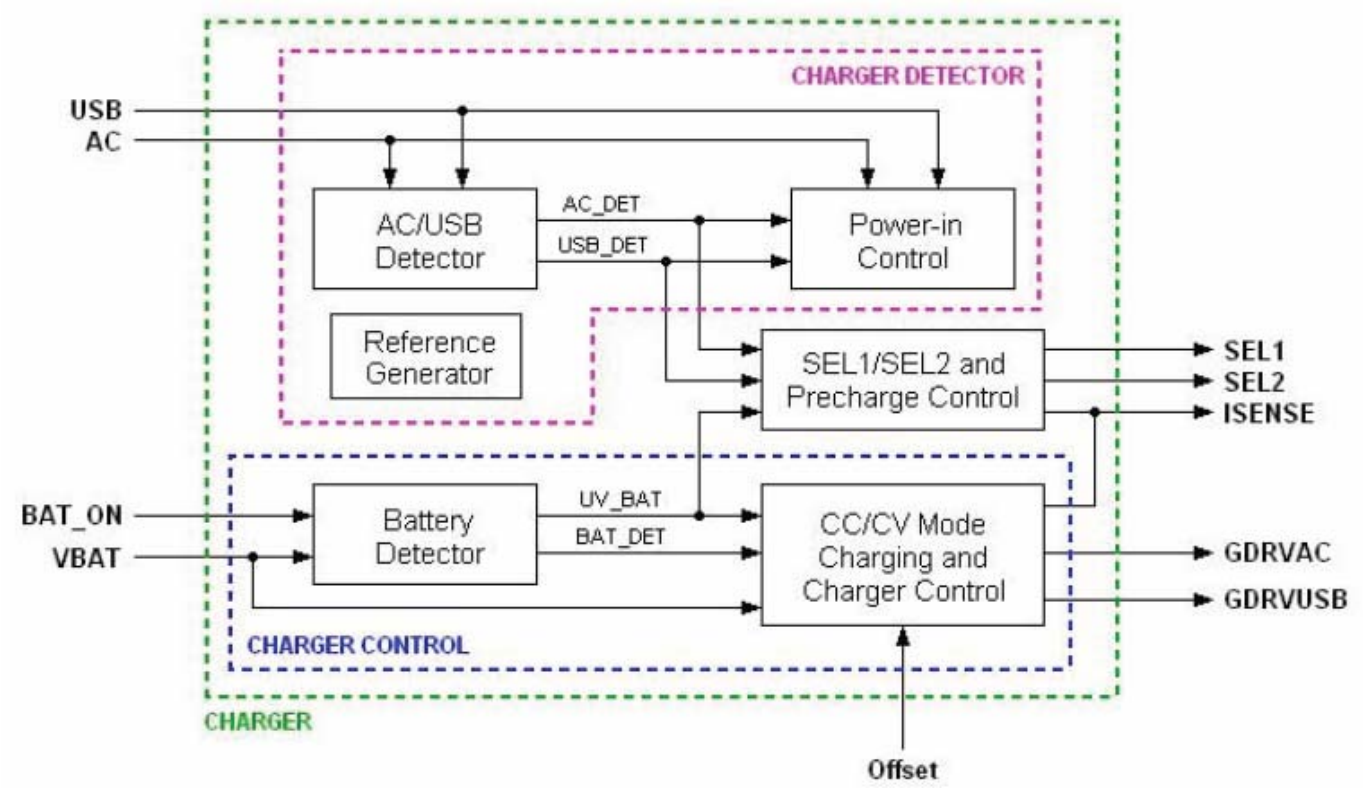


Figure 42. PMIC Charger Block Diagrams

Charger Detector

The charger detector senses the charging voltage from either a standard AC-DC adaptor or a USB connection. When the charging input voltage is greater than the pre-determined threshold, the charging process is triggered. The detector resists higher input voltages than other parts of the PMIC.

Charger Control

When the charger is on, this block controls the charging phase and turns on the appropriate LDOs according to the battery status. The battery voltage is constantly monitored: if the voltage is greater than 4.3 V, charging is stopped immediately to prevent permanent damage to the battery.

Control for Pre-Charge Indication

The PMIC provides 2 control signals SEL1 and SEL2 for the application that shows pre-charge status on the LCD. In normal cases, VBAT is selected (SEL2 turned on) as the power input to the PMIC.

State	CHR_EN	CHR_DET	VBAT<3.3/3.0 V	CV(VBA>4.2 V)	BAT_ON (battery inserted)	Operation
No charging	X	L	X	X	L	Wait for CHR_DET transition
Charger detection	L	H	L	X	L	Wait for CHR_EN
Pre-charging	X	H	H	L	L	Monitor UV and CHR_DET (see Note)
CC charging	H	H	L	L	L	Monitor CV and CHR_DET
CV charging	H	H	L	H	L	Monitor CHR_DET
Pause charging	L	H	X	X	L	No charge
Emergency stop	X	H	X	X	H	Turn off charger powered off state

Figure 43. Charger and Voltage Detection

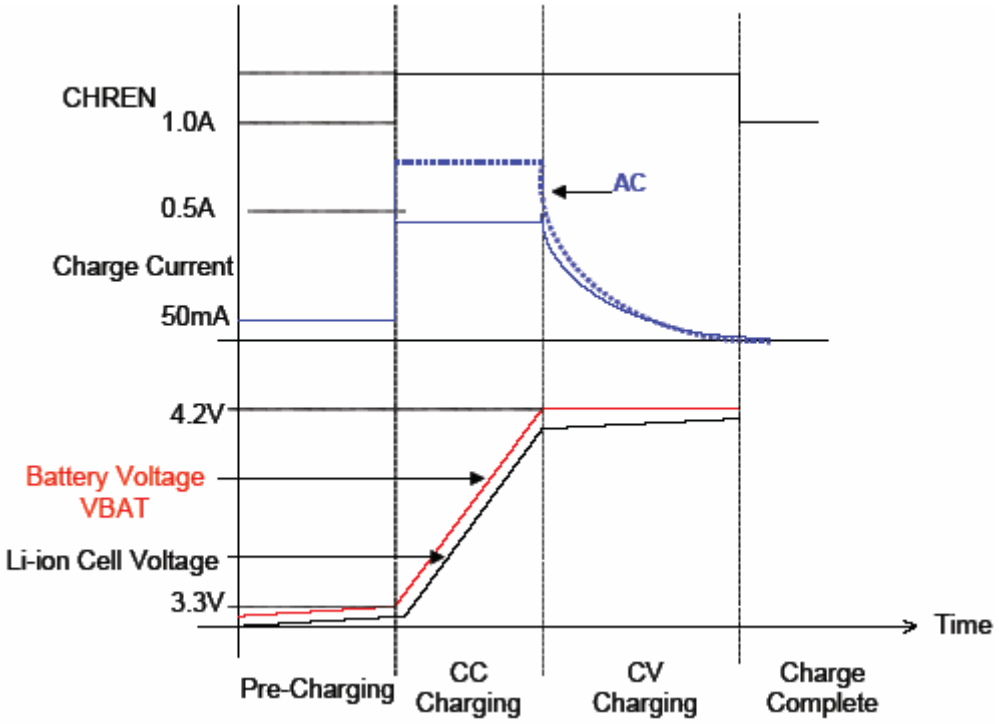


Figure 44. Li-Ion Battery Charging Profile

2. Low Dropout Regulator (LDOs) and Reference

The MT6318 integrates eleven LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

1) Digital Core LDO (VD)

The digital core LDO is a regulator that sources 200 mA (max) with a 1.8 V or 1.2 V output voltage selection based on the supply voltage requirement of the BB chipset. The LDO also provides 1.5 V/0.9 V power-down modes that can be controlled either by the SRCLKEN pin or by the PWR_SAVE_SPI software register. The digital core LDO supplies the BB circuitry in the handset, and is optimized for a very low quiescent current.

2) Digital IO LDO (VIO)

The digital IO LDO is a regulator that sources 100 mA (max) with a 2.8 V output voltage. The LDO supplies the BB circuitry in the handset, and is optimized for a very low quiescent current. This LDO powers up at the same time as the digital core LDO.

3) Analog LDO (VA)

The analog LDO is a regulator that sources 150 mA (max) with a 2.8 V output voltage. The LDO supplies the analog sections of the BB chipsets and is optimized for low frequency ripple rejection in order to reject the ripple coming from the RF power amplifier burst frequency at 217 Hz.

4) TCXO LDO (VTCXO)

The TCXO LDO is a regulator that sources 20 mA (max) with a 2.8 V output voltage. The LDO supplies the temperature compensated crystal oscillator, which needs its own ultra low noise supply and very good ripple rejection ratio.

5) RTC LDO (VRTC)

PMIC features a 2-step RTC that keeps RTC alive for a long time after the battery has been removed. The 1st LDO charges a backup battery on the BAT_BACKUP pin to ~2.6 V. Also, when the battery is removed, the first stage prevents the backup battery from leaking back to VBAT. The 2nd LDO regulates the 2.6 V supply to a 1.5 V/1.2 V optional RTC voltage. The RTC voltage can be set by the RTC_SEL pin while the BB is alive.

6) Memory LDO (VM)

The memory LDO is a regulator that sources 150 mA (max) with a 1.8 V or 2.8 V output voltage selection based on the supply specs of the memory chips. The LDO supplies the memory circuitry in the handset, and is optimized for a very low quiescent current. This LDO powers up at the same time as the digital core LDO.

7) SIM LDO (VSIM)

The SIM LDO is a regulator that sources 20 mA (max) with a 1.8 V or 3.0 V output voltage selection based on the supply specs of subscriber identity module (SIM) card. The LDO supplies the SIMs in the handset, and is controlled independently of the other LDOs.

8) Memory Card LDO (VMC)

The memory card LDO is a regulator that sources 250 mA (max) with a 2.8 V or 3.0 V output voltage selection. The LDO supplies the memory card (MS, SD, MMC) in the handset, and is controlled independently of the other LDOs.

9) Auxiliary Analog Circuit LDO (VA_SW)

The auxiliary analog circuit LDO is a regulator that sources 50 mA (max) with 2.8 V or 3.3 V output voltage selection based on the VA_SW_SEL register setting (Register F [7]). It can be switched on/off by register control.

10) USB IO LDO (VUSB)

The USB IO LDO is a regulator that sources 20 mA (max) with a 3.3 V output voltage. The LDO output on/off follows the control bit USB_PWR (Register 1 [3]). When the USB_PWR control bit is set to off, the VUSB output voltage drops below 0.3 V within 1 ms. (VUSB output is shunt with a 1 μF capacitor.)

11) Vibrator LDO (VIBR)

The vibrator LDO is a regulator that sources 200 mA (max) with a 1.8 V or 3.2 V output voltage selection based on the VIBSEL register setting (Register E [1]). This LDO can be powered on/off by register.

12) Reference Voltage Output (VREF)

The reference voltage output is a low noise, high PSRR and high precision reference with a guaranteed accuracy of 1.5% over temperature. The output is used as a system reference in MT6318 internally. However for accurate specs of every LDO output voltage, avoid loading the reference voltage; only bypass it to GND with a minimum 100 Nf capacitance.

Conditions							Operations							
THR	UV (PWRIII)	CHDET	PWRKEY	PWRBB	SRCLKEN	PWRIII <2.5V	VTCXO	VRTC	VA	VD/VIO /VM	VUSB	VMC	VSIM	VA_SW
L	H	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	X	X	X	X	L	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	L	X	L	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	X	X	H	L	ON	ON	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	ON	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
					L	L	OFF	ON	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	ON	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
L	L	X	L	X	H	L	ON	ON	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	ON	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
					L	L	OFF	ON	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	ON	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
L	L	X	X	H	H	L	ON	ON	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	ON	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
					L	L	OFF	ON	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	ON	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
H	X	X	X	X	X	L	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF

Figure 45. Status of Mobile Handset and LDOs.

3. LED Drivers

PMIC provides 4 independent drivers. Three of them use an identical structure to drive 3 different LEDs (R, G, B). The fourth is dedicated to driving the keypad LEDs. The reason for separating the LED drivers into 2 groups is phone feature oriented.

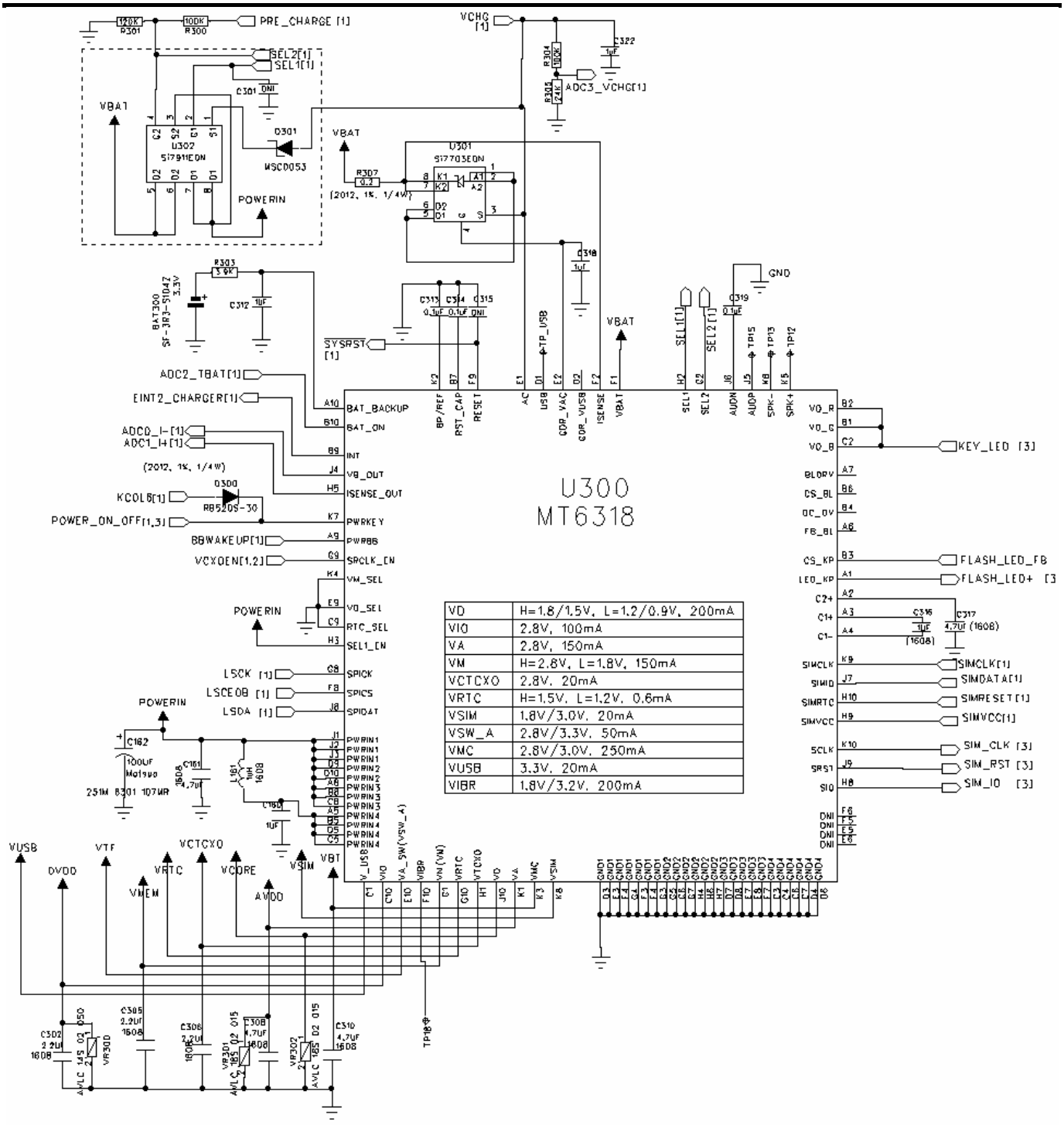


Figure 46. MT6318 Circuit diagram

To Power on the handset, The Power_On_Off Signal must be Low. The external sense resistor R307 0.2ohm can determine the charging current. The function equation is : Iconstant = 0.16/R307 = about 800mA. Ipre-charging = 10/R307 = about 50mA. The LDO Bypass capacitors are recommended to use Min X5R grade. Specially The DVDD, AVDD,VMEM and VCORE must be used 4.7uF, 2012 type.

IV. HYC0UGE0MF1P-5SH0EP

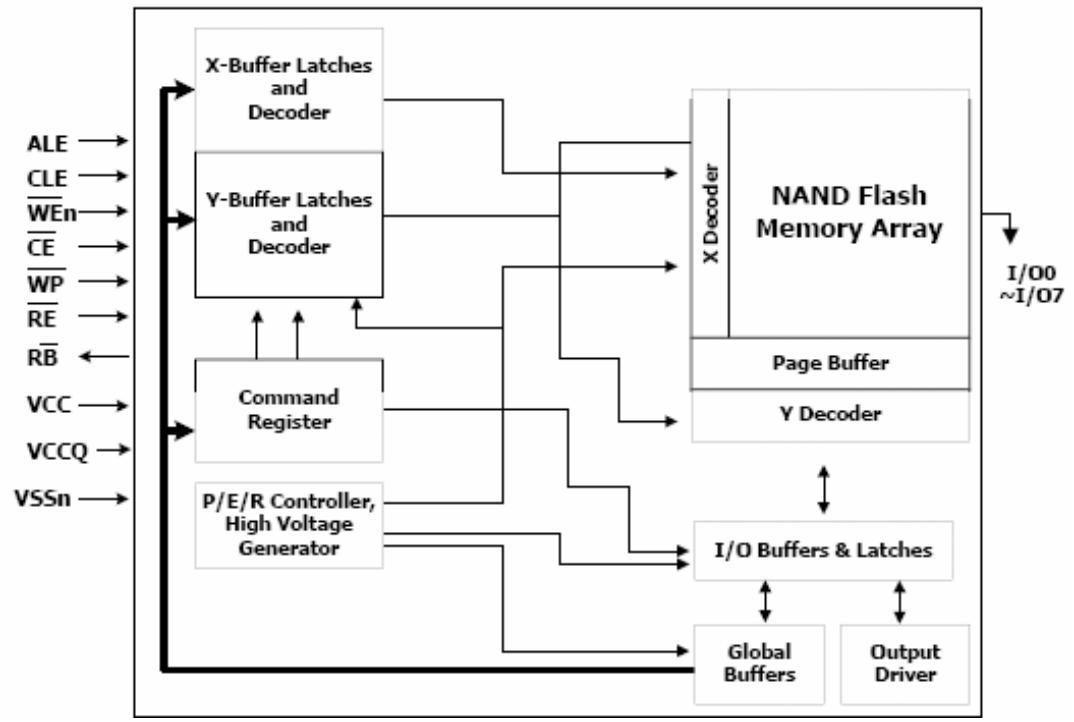
1G (128Mx8bit) Nand FLASH Memory and 256M (16Mx16bit) Mobile SDRAM Multi-Chip Package

The HYC0UGE0MF1P-5SH0E(P) Series is suited for mobile communication system application which use in data memory to reducenot only mount area but also power consumption. The HYNIX HYC0UGE0MF1P-5SH0E(P) is is a Multi Chip Package Memory which combined a 553,648,128-bit Nand Flash Memory and a 268,435,456-bit Low Power Synchronous DRAM(Mobile SDRAM). Combination of HYC0UGE0MF1P-5SH0E(P), 1Gbit NAND Flash memory is organized as 64M x8 bits and the size of a Page is either 528 Bytes (512 + 16 spare) depending on whether the device has a x8 bus width. 256Mbit Low Power SDRAM(Mobile SDRAM) is a 268,435,456bit CMOS Synchronous Dynamic Random Access Memory. It is organized as 4banks of 4,194,304x16.

The devices are available in the following packages: 149-Ball P-FBGA Type - 10x14.0mm, 0.8mm pitch : Lead Free

SYMBOL	TYPE	DESCRIPTION
1G NAND Flash Device Pin		
I/O0 ~ I/O7	I/O	Input/Output
$\overline{CE}$	INPUT	Chip Enable
$\overline{WEn}$	INPUT	Write Enable
$\overline{RE}$	INPUT	Read Enable
ALE	INPUT	Address Latch Enable
CLE	INPUT	Command Latch Enable
$\overline{WP}$	INPUT	Write Protect
RY/$\overline{BY}$	I/O	Ready/Busy
VCCn	Power	Power Supply

256M (4M x4Bank x16bit) Mobile SDRAM Device Pin		
CLK	INPUT	Clock : Clock input for Mobile SDRAM
CKE	INPUT	Clock enable for Mobile SDRAM
A0 to A12	INPUT	Address inputs for Mobile SDRAM
BA0, BA1	INPUT	Bank Select for Mobile SDRAM
$\overline{RAS}$	INPUT	Row address strobe for Mobile SDRAM
$\overline{CAS}$	INPUT	Column address strobe for Mobile SDRAM
$\overline{WE}$	INPUT	Write enable for Mobile SDRAM
$\overline{CS}$	INPUT	Chip select for Mobile SDRAM
UDQM	INPUT	Upper Input/Output for Mobile SDRAM
LDQM	INPUT	Lower Input/Output for Mobile SDRAM
DQ0 ~ DQ15	I/O	Data Input/Output for Mobile SDRAM
VDD	Power	Main power supply for Mobile SDRAM
VDDQ	Power	DQ power supply for Mobile SDRAM
VSSd	Ground	Ground
DNU	-	Do Not Use
NC	-	No connection : These pads should be left unconnected



NAND FLASH MEMORY 528MBIT = 528 BYTES X 32 PAGES X 4,096 BLOCKS

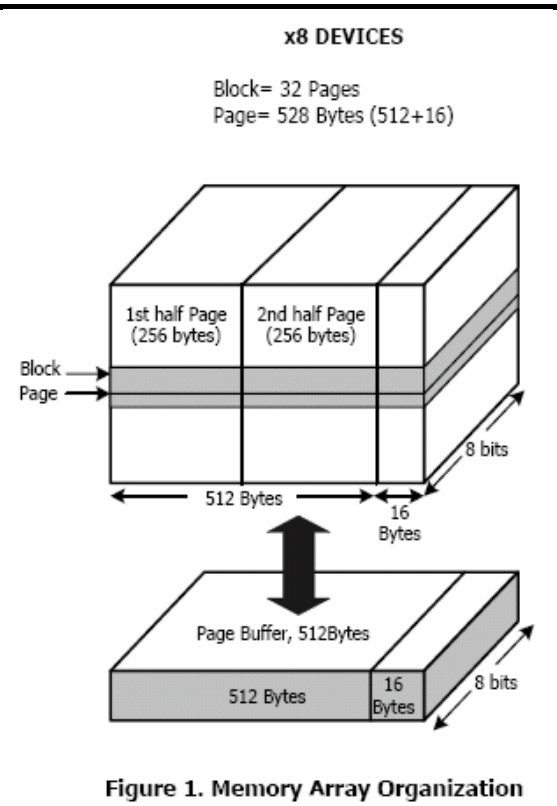


Figure 45. Nand Flash Block diagram and Memory Cell

Organized as 4banks of 4,194,304x16

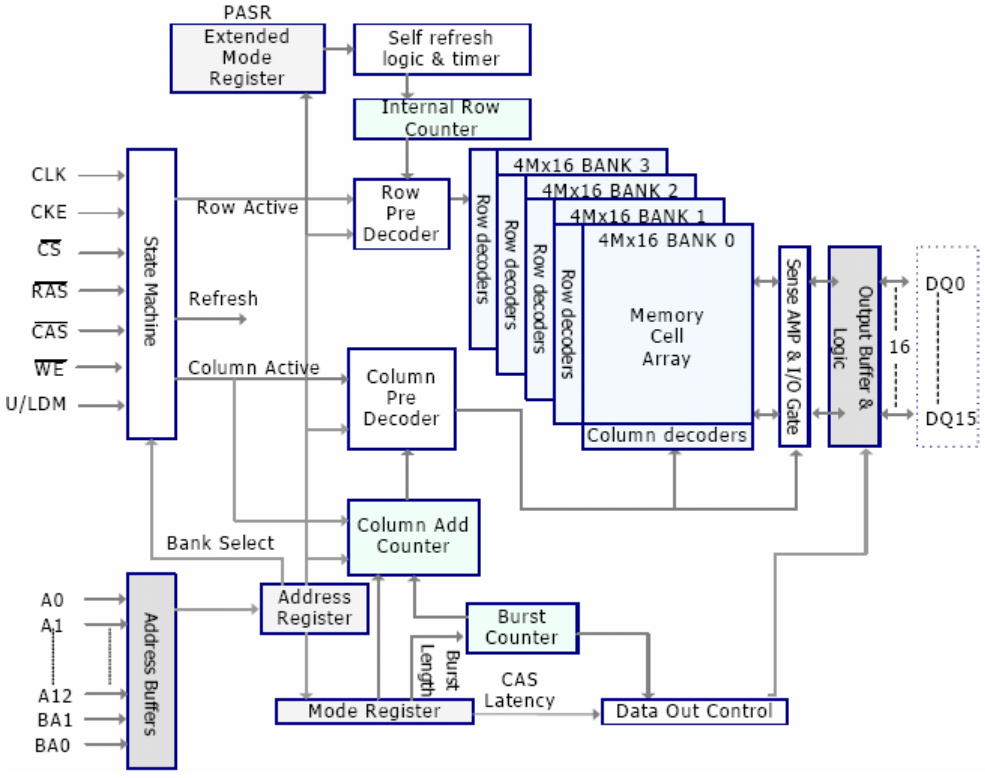


Figure 46. SDRAM Block diagram

DC Operating Voltage

Parameter		Symbol	Min	Typ	Max	Unit	Note
VDD Power Supply Voltage		VDD	1.7	1.8	1.95	V	
VDDQ Power Supply Voltage		VDDQ	1.7	1.8	1.95	V	
VCCn Power Supply Voltage		VCCn	2.5	2.7	3.0	V	
Input High Voltage	NAND FLASH	VIH	2.0	-	VCCn+0.3	V	
	Mobile SDRAM		0.8*VDDQ	-	VDDQ+0.3	V	1
Input Low Voltage	NAND FLASH	VIL	-0.3	-	0.4	V	2
	Mobile SDRAM		-0.3	-	0.3	V	3

DC Characteristics (Nand Flash Memory). VCC : 2.5V ~ 3.0V.

Sym-bol	Parameter		Test Condition	Min	Typ.	Max	Unit
ICC1	NAND Operating Current	Sequential Read	t_{RLRL} minimum $\overline{CE}=V_{IL}$, I_{OUT} = 0 mA	-	10	20	mA
ICC2		Program	-	-	10	20	mA
ICC3		Erase	-	-	10	20	mA
ICC4	NAND Standby Current (TTL)		$\overline{CE}=V_{IH}$, $\overline{WP}$=0V/V_{CC}	-	-	1	mA
ICC5	NAND Standby Current (CMOS)		$\overline{CE}=V_{CC}$-0.2, $\overline{WP}$=0/V_{CC}	-	10	50	uA

DC Characteristics (Mobile SDRAM). VDD/VDDQ : 1.7 ~ 1.95V

Parameter	Symbol	Test Condition	Speed		Unit	Note
			H	S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	65	55	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns	0.3		mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	0.3		mA	
Standby Current in Deep Power Down Mode	IDD7	See p. 83 ~ 84 & 90 ~ 91	10		uA	

RF section

RF Section is combined with Transceiver MT6120, VCTCXO CSX-325T26, Power Amplier Module RF3166 and Front-End Module LMSP54HA-348(9). The MEGA3 was designed for Tri-Band according to FEM, PCB Modify and S/W Matching.

The one type is GSM900, DCS1800 an PCS1900 with LMSP54HA-348. Another type is GSM900, DCS1800 and PCS1900 with LMSP54HA-348.

I. MT6120 (RF Transceiver IC)

MT6120 includes LNAs, two RF quadrature mixers, an integrated channel filter, programmable gain amplifiers(PGA), an IQ demodulator for the receiver, a precision IQ modulator with offset PLL for the transmitter, two internal TX VCOs, a VCXO, on-chip regulators, and a fully programmable sigma-delta fractional-N synthesizer with an on-chip RF VCO.

Features Receiver

- Very low IF architecture
- Quad band differential input LNAs
- Quadrature RF mixers
- Fully integrated channel filter
- More than 100 dB gain
- More than 110 dB control range
- Image-reject down conversion to baseband

Transmitter

- Precision IQ modulator
- Translation loop architecture
- Fully integrated wideband TX VCO
- Fully integrated TX loop filter

Frequency Synthesizer

- Single integrated, fully programmable fractional- N synthesizer
- Fully integrated wideband RF VCO
- Fast settling time suitable for multi-slot GPRS application

Voltage Control Crystal Oscillator (VCXO)

- 26 MHz crystal oscillator capable of supporting 13 MHz / 26 MHz output clock
- Programmable capacitor array for coarse tuning
- Internal varactor for fine tuning

Regulators

- Built-in low-noise, low-dropout (LDO) regulators

Low power consumption

QFN (Quad Flat Non-lead) Package 56-pin SMD

3-wire serial interface

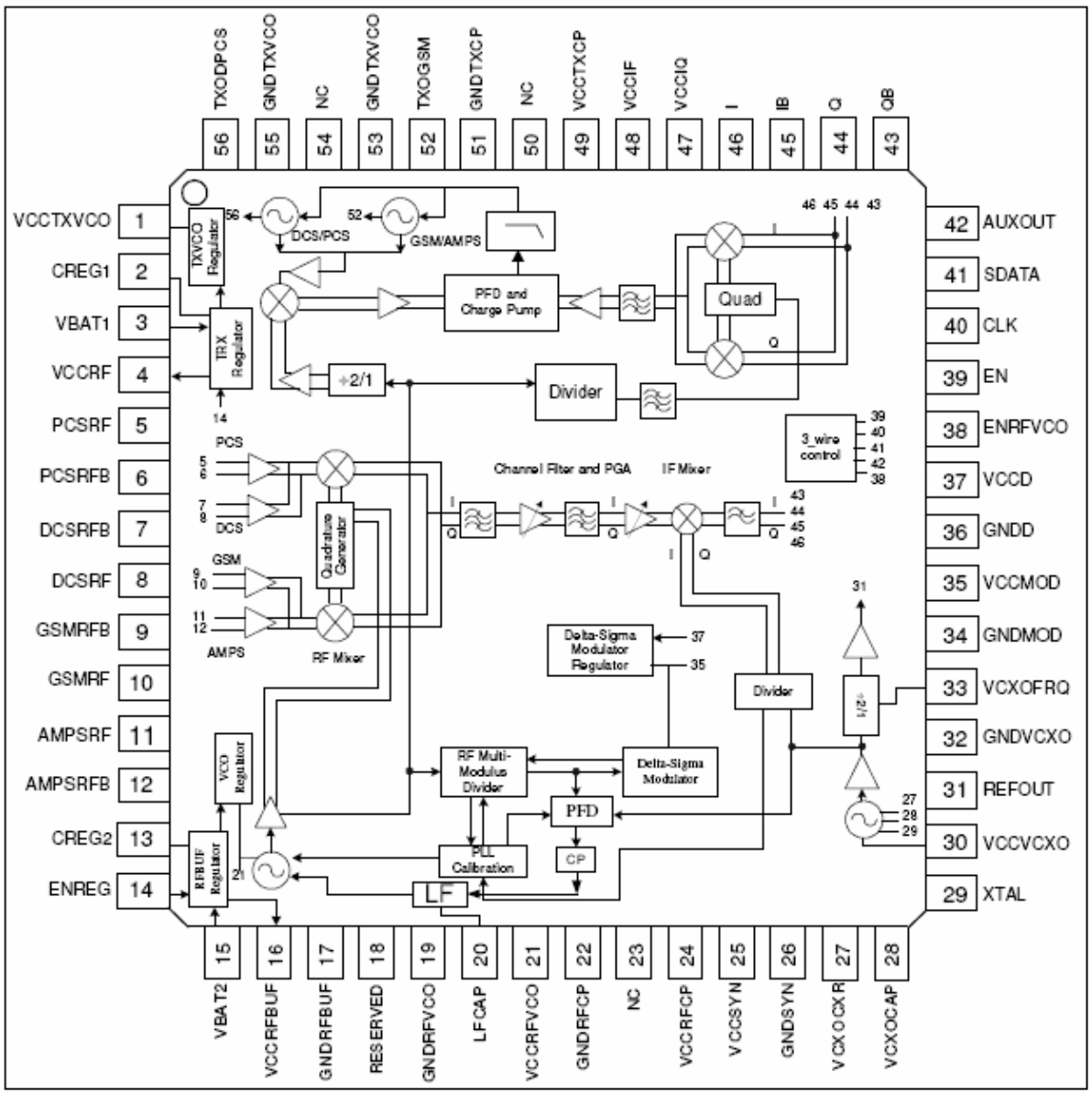


Figure 47. MT6120 Functional block diagram

- Recommended Operating Range

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage(VBAT)	VBAT	3.1	3.6	4.6	V
Power Supply Voltage(VCCD)	VCCD	2.5	2.8	3.1	V
Operating Ambient Temperature	Topr	-20	25	75	C

A description of MT612X hardware control pins and their functionality are shown in the table below. MT612X has an internal VCXO and its control.

Name	Setting	Description
ENREG	0	Power off Regulator1 and 2
	1	Power on Regulator 1 and 2
ENRFVCO	0	Power off RFVCO
	1	Power on RFVCO
VCXOCXR	0	Select internal VCXO
	1	Select external TCVCXO Note: Connect to VCCVCXO
VCXOFRQ	0	Reference output buffer 13 MHz
	1	Reference output buffer 26 MHz Note: Connect to VCCVCXO

Pin Description

Pin No.	Pin Name	Description
1	VCCTXVCO	TX VCO supply voltage and Regulator 1 (TX VCO) voltage output
2	CREG1	Regulator 1 external noise bypass capacitor
3	VBAT1	Battery supply for Regulator 1
4	VCCRF	TRX RF and TX BUF block supply voltage and Regulator 1 (TRX) voltage output
5	PCSRF	Receiver PCS 1900 RF differential positive input
6	PCSRFB	Receiver PCS 1900 RF differential negative input
7	DCSRFB	Receiver DCS 1800 RF differential negative input
8	DCSRF	Receiver DCS 1800 RF differential positive input
9	GSMRFB	Receiver E-GSM 900 RF differential negative input
10	GSMRF	Receiver E-GSM 900 RF differential positive input
11	AMPSRF	Receiver GSM 850 RF differential negative input
12	AMPSRFB	Receiver GSM 850 RF differential positive input
13	CREG2	Regulator 2 external noise bypass capacitor
14	ENREG	Regulator 1 & 2 enable input for TRX/ RFVCO buffer/ Synthesizer/ VCXO
15	VBAT2	Battery supply for Regulator 2
16	VCCRFBUF	RF VCO buffer supply voltage and Regulator 2 (SX) voltage output
17	GNDRFBUF	RF VCO buffer ground
18	Reserved	Keep this pin floating
19	GNDRFVCO	RF VCO ground
20	LFCAP	Loop filter main capacitor input
21	VCCRFVCO	RF VCO supply voltage and Regulator 2 (RF VCO) voltage output
22	GNDRFCP	Synthesizer charge pump and PFD ground
23	NC	No connection
24	VCCRFCP	Synthesizer charge pump and PFD supply voltage
25	VCCSYN	Synthesizer supply voltage
26	GNDSYN	Synthesizer ground
27	VCXOCXR	VCXO internal / external output buffer control
28	VCXOCAP	VCXO coarse tuning capacitor and fine tuning varactor

29	XTAL	26 MHz crystal reference input
30	VCCVCXO	VCXO supply voltage
31	REFOUT	13 MHz / 26 MHz reference buffer output
32	GNDVCXO	VCXO ground
33	VCXOFRQ	Reference output buffer 13 MHz / 26 MHz selection
34	GNDMOD	Synthesizer Sigma-Delta modulator ground
35	VCCMOD	Synthesizer Sigma-Delta modulator supply voltage and Regulator 3 output
36	GNDD	3-wire digital circuit ground
37	VCCD	Supply voltage for 3-wire digital circuit and supply voltage for Regulator 3
38	ENRFVCO	Regulator 2 enable input for RFVCO
39	EN	3-wire serial bus enable input
40	CLK	3-wire serial bus clock input
41	SDATA	3-wire serial bus data input
42	AUXOUT	Auxiliary test output
43	QB	Q path negative baseband input / output
44	Q	Q path positive baseband input / output
45	IB	I path negative baseband input / output
46	I	I path positive baseband input / output
47	VCCIQ	IF circuit supply voltage
48	VCCIF	Transmitter PFD and Receiver IF circuit supply voltage
49	VCCTXCP	Transmitter charge pump supply voltage
50	NC	No connection
51	GNDTXCP	Transmitter charge pump ground
52	TXOGSM	TX VCO buffer transmit output for GSM
53	GNDTXVCO	TX VCO ground
54	NC	No connection
55	GNDTXVCO	TX VCO ground
56	TXODPCS	TX VCO buffer transmit output for DCS/PCS

1. Receiver

The receiver section of MT6120 includes Quad-band low noise amplifiers(LNAs), RF quadrature mixers, an on-chip channel filter, Programmable Gain Amplifiers(PGAs), quadrature second mixers, and a final low-pass filter. The very low-IF MT6120 uses image-rejection mixers and filters to eliminate interference. With accurate RF quadrature signal generation and mixer matching techniques, the image rejection of the MT6120 can reach 35dB for all bands. Compared to a direct conversion receiver(DCR), MT6120's very low-IF architecture improves the blocking rejection, AM suppression, as well as the adjacent channel interference performance.

- Receiver Input Frequency

Mode	Min	Max	Unit
GSM850	869	894	Mhz
GSM900	925	960	Mhz

DCS	1805	1880	Mhz
PCS	1930	1990	Mhz

The below table is shown LNA input impedance. So, From FEM Sawfilter to MT6120 LNA input, The Impedance matching is need for high sensitivity. The L903, L904, L905, C910, C911, C912, C913, C914 and C915 are the matching State.

LNA differential input impedance	GSM850	Zin, RF = 882 MHz		71-j73 (146// 1.2 pF)		Ω
	GSM900	Zin, RF = 945 MHz		71-j73 (146// 1.2 pF)		Ω
	DCS	Zin, RF = 1842 MHz		33-j85 (252// 885 fF)		Ω
	PCS	Zin, RF = 1960 MHz		37-j81 (214// 830 fF)		Ω

The IF signal is then filtered and amplified through an image-rejection filter and a PGA. The multi-stage PGA is implemented between filtering stages to control the gain of the receiver. With 2 dB gain steps, a 78 dB dynamic range of the PGA ensures a proper signal level for demodulation. The quadrature 2nd mixers are provided on-chip to down convert IF signal to baseband in an analog differential IQ format.

2. Transmitter

The MT6120 transmitter section consists of two on-chip TX VCOs, buffer amplifiers, a down-converting mixer, a quadrature modulator, an analog phase detector and a digital phase frequency detector, each with a charge pump output and on chip loop filter. The dividers and loop filters are used to achieve the desired IF frequency from the down-conversion mixer and quadrature modulator. For a given transmission channel, the transmitter will select one of the two different TX reference dividing numbers. These built-in components, along with an internal voltage controlled oscillator and a loop filter, implement a translation loop modulator. The TX VCO output is fed to the power amplifier. A control loop, implemented externally, is used to control the PA's output power level.

- Transceiver Output Frequency

Mode	Min	Max	Unit
GSM850	824	849	Mhz
GSM900	880	915	Mhz
DCS	1710	1785	Mhz
PCS	1850	1910	Mhz

3. TX VCO

Two power VCOs are integrated with OPLL to form a complete transmitter circuit. The TX VCO output power is typically 9dBm with +/-2.5dB variation in GSM850 bands and +8dBm output power with +/-2dB variation in PCS1900 bands over extreme Temperature conditions.

The PAM(RF3166) Input range is typically 3dBm. So 5dB Attenuator is added Between MT6120 and RF3166.

- For GSM850/GSM900 : R406, R407, R408,
- For DCS/PCS : R403, R404, R405.

Tx VCO Frequency Range is same with Transmitter Frequency Range.

4. Frequency Synthesizer

The MT6120 includes a frequency synthesizer with a fully integrated RF VCO to generate RX and TX local oscillator frequencies. The PLL locks the RF VCO to a precision reference frequency at 26MHz. To reduce the acquisition time or to enable fast settling time for multi-slot data services such as GPRS, a digital loop along with a fast-acquisition system are implemented in the synthesizer. After the calibration, a fast-acquisition system is utilized for a period of time to facilitate fast locking.

The frequency ranges of the synthesizer for RX mode are

RX mode	GSM850	1737Mhz ~ 1788Mhz
	GSM900	1850Mhz ~ 1920Mhz
	DCS1800	1805Mhz ~ 1880Mhz
	PCS1900	1930Mhz ~1990Mhz

The Calculate LO Frequency Fvco from RX Channel Frequency Fch is following.

Fvco = 2*Fch-200K	for GSM850 and GSM900
Fvco = Fch-100K	for DCS1800 and PCS1900.

The frequency ranges of the synthesizer for TX mode are

TX mode	GSM850	1813Mhz ~ 1868Mhz
	GSM900	1936Mhz ~ 2059Mhz
	DCS1800	1881Mhz ~ 2008Mhz
	PCS1900	2035Mhz ~2149Mhz

The Calculate LO Frequency Fvco from TX Channel Frequency Fch is following.

(Set the divider ratio D1 of TX reference divider = 11)

Fvco = 2*D1*Fch/(D1-1)	for GSM850 and GSM900
Fvco = D1*Fch/(D1-1)	for DCS1800 and PCS1900.

The MT6120 uses a digital calibration technique to reduce the PLL settling time once the RF synthesizer is programmed through a 3-wire serial interface, the calibration loop is activated. The main function of the calibration loop is to preset the RF VCO to the vicinity of the desired frequency quickly and correctly, thus aiding the PLL to

settle faster. On the other hand, since a large portion of initial frequency error is dealt with by the integrated calibration loop, the overall locking time can be drastically reduced, irrespective of the desired frequency.

5. Voltage Control Crystal Oscillator(VCXO)

VCXO consists of an amplifier, a buffer, and a programmable capacitor array. The VCXO provides the MT6120 with a selectable reference frequency of either 13MHz or 26MHz. When VCXOFRQ pin is high, Output Frequency is 26Mhz. When VCXOFRQ pin is low, Output Frequency is 13Mhz.

VCXOFRQ is high in MEGA3. The Amplifier is designed to be in series resonance with a standard 26Mhz crystal. The Crystal is connected from the Input pin XAL of Amplifier to ground through a series load capacitance. The buffer provides a typical 600mVpp voltage swing. As an alternative, the reference frequency can be provided by an external 26Mhz VCTCXO module. When Pin VCXOCXR is tied to the VCCVCXO supply, the XTAL pin will accept an external signal. Furthermore, the VCXO control pin can be tied to VCCVCXO to prevent the current leakage during the sleep mode operation.

Buffer output level	13 MHz baseband clock (Load = 148 - j1206 Ω@ Frequency = 13 MHz) 26 MHz baseband clock (Load = 37 - j610 Ω@ Frequency = 26 MHz)	400	600		mVpp
Duty cycle	13 MHz / 26 MHz baseband clock	45		55	%

6. Regulator

The MT6120 internal regulators provide low noise, stable, temperature and process independent supply voltages to critical blocks in the transceiver. An internal P-channel MOSFET pass transistor is used to achieve a low dropout voltage of less than 150mV in all regulators.

II. RF3166 (GSM850,GSM900 and DCS,PCS Power Amplifier Module)

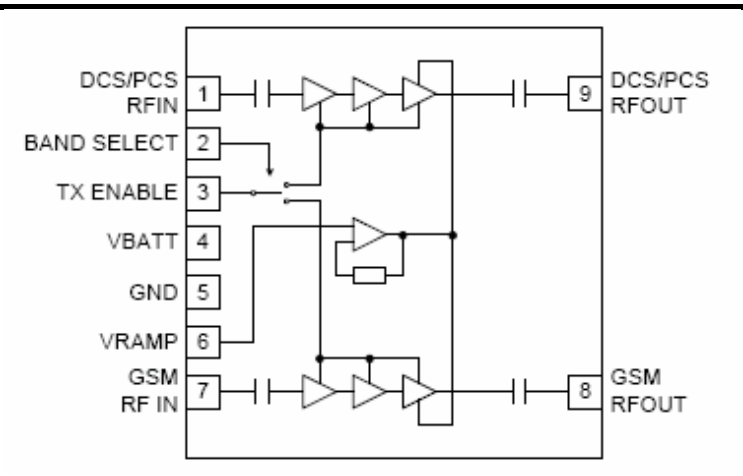


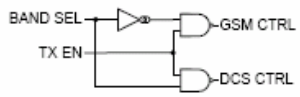
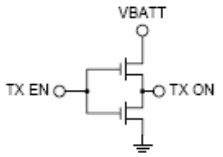
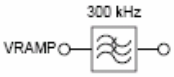
Figure 48. RF3166 Block Diagram

The RF3166 is a high-power, high-efficiency power amplifier module with integrated power control that provides over 50dB of control range. The device is a self-contained6mmx6mm module with 50Ω input and output terminals. The device is designed for use as the final RF amplifier inGSM850, EGSM900, DCS and PCS handheld digital cellular equipment and other applications in the 824MHz to849MHz, 880MHz to 915MHz, 1710MHz to 1785MHzand 1850MHz to 1910MHz bands. The RF3166 incorporates RFMD's latest VBATT tracking circuit, which monitors battery voltage and prevents the power control loop from reaching saturation. The VBATT tracking circuit eliminates the need to monitor battery voltage, thereby minimizing switching transients. The RF3166 requires no external routing or external components, simplifying layout and reducing board space.

The VRamp Range is from 0.26V to 2.1V. And the R400, R401, C408 is a Voltage divider for fine tuning and Low pass filter of 300Khz.

The Input/Output Impedance is 50ohm. So, The PCB Design must be designed with 50ohm strobe line.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies. The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Pin	Function	Description	Interface Schematic
1	DCS/PCS IN	RF input to the DCS band. This is a 50Ω input.	
2	BAND SELECT	Allows external control to select the GSM or DCS band with a logic high or low. A logic low enables the GSM band whereas a logic high enables the DCS band.	
3	TX ENABLE	This signal enables the PA module for operation with a logic high.	
4	VBATT	Power supply for the module. This should be connected to the battery.	
5	GND		
6	VRAMP	Ramping signal from DAC. A 300kHz lowpass filter is integrated into the CMOS. No external filtering is required.	
7	GSM IN	RF input to the GSM band. This is a 50Ω input.	
8	GSM OUT	RF output for the GSM band. This is a 50Ω output. The output load line matching is contained internal to the package.	
9	DCS/PCS OUT	RF output for the DCS band. This is a 50Ω output. The output load line matching is contained internal to the package.	
Pkg Base	GND		

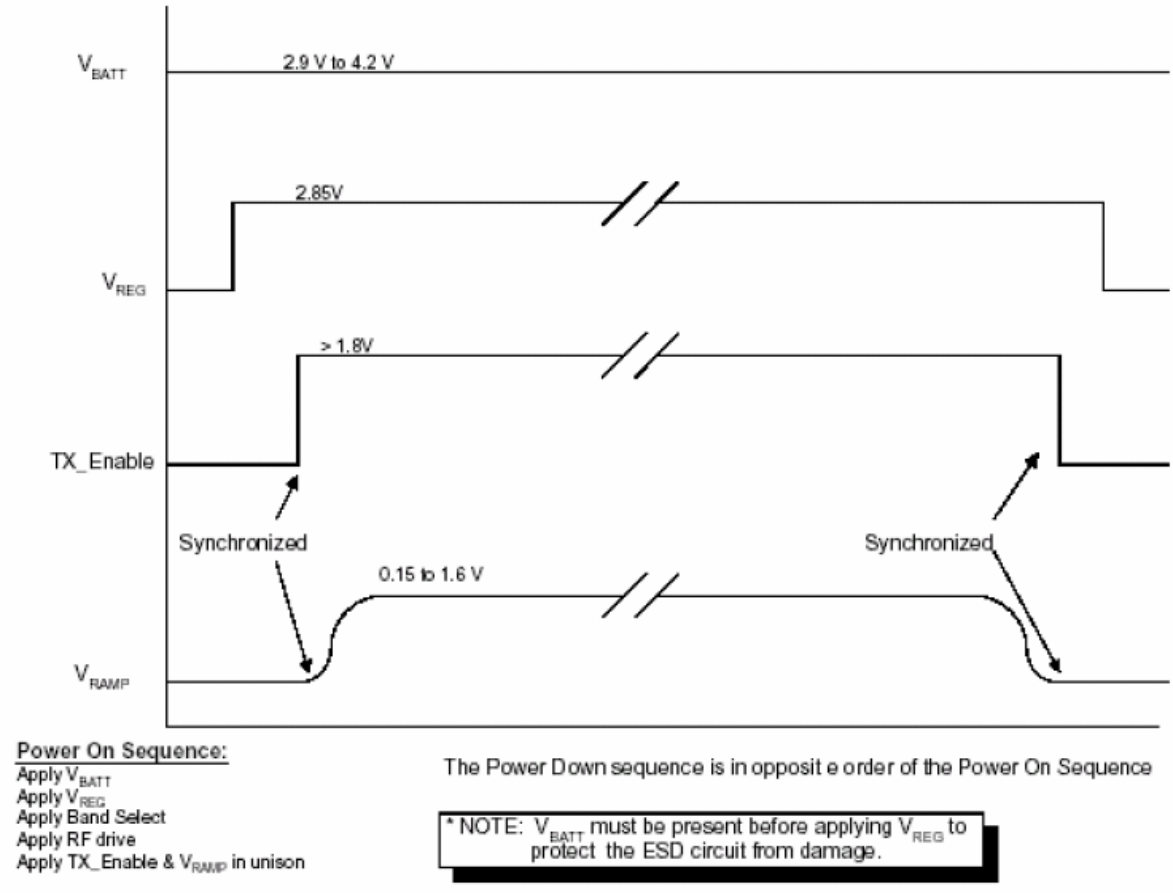
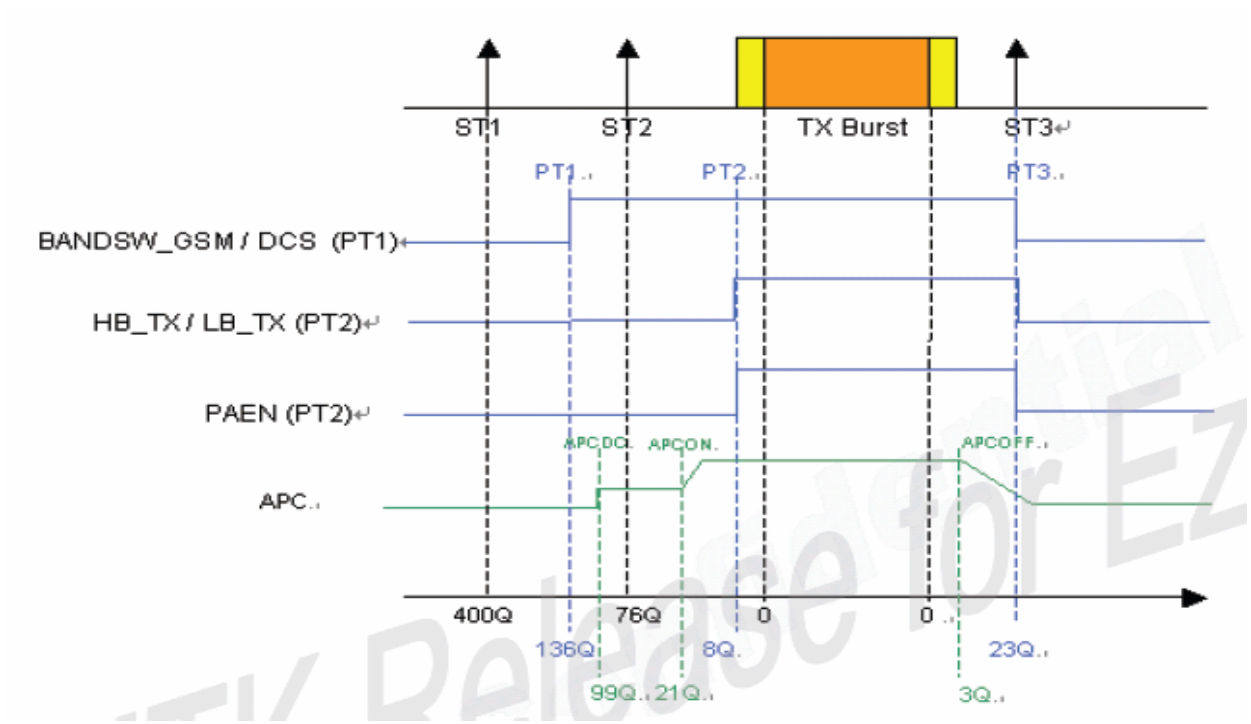


Figure 49. Power control sequence

The Next Picture is for RF TX Timing of BSI and BPI.



< Single Slot TX Event with Timing Requirement>

<BSI Interface>

In order to simply the serial control mechanism, and achieve best usage of BSI resources. Each burst transmitted, There are three generic timing defined (ST1/ST2/ST3) to send 3-wire control commands to transceiver. Usually 1'st BSI event(ST1) is used to warm up the synthesizer and set its N-counter to lock the operational frequency. The 2'nd BSI(ST2) is used to set the transmitted mode and indicate the operational band. The 3'rd BSI(ST3)is used to command transceiver entering idle mode. All bands(GSM/DCS/PCS) share the same timing.

<BPI interface>

In order to simply the parallel control mechanism, and achieve best usage of BPI resources. Each burst transmitted, there are also three generic timing defined(PT1/PT2/PT3) to send HW control Signals to RF module. In other words, there are only three timing events to trigger HW control signals changing their states. Usually 1'st BPI event(PT1) is used to select suitable band for TXVCO. The 2'nd BPI(PT2) is used to turn on PA and control antenna switch depends on its band. The 3'rd BSI(ST3) is used to force RF module to terminate transmission and enter idle mode. All bands share the same timing but could has different HW control signals.

III. LMSP54HA-348 (Antenna Switch Module For Tri- Band with SAW Filter)

LMSP54HA-348 is an Antenna Switch Module for GSM900, DCS1800 and PCS1900 of Murata with Three SAW Modules. Control Pins (VC1, VC2, and VC3) are connected to LB_TX, HB_TX, and PCS_RX (signals from baseband processor). The Control Pins Operating range is 2.4V ~ 2.8V.

LB_TX : GSM900 TX Enable.

HB_TX : DCS1800, PCS1900 TX Enable.

PCS_RX : PCS RX Enable.

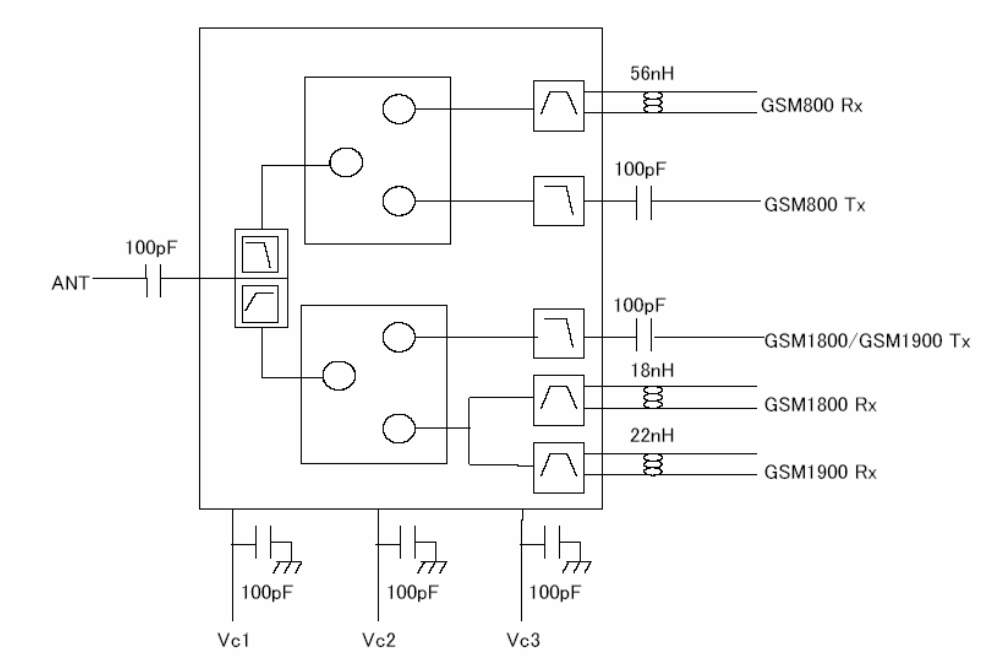


Figure 50. The Evaluation board of LMSP54HA-349

TERMINAL CONFIGURATION

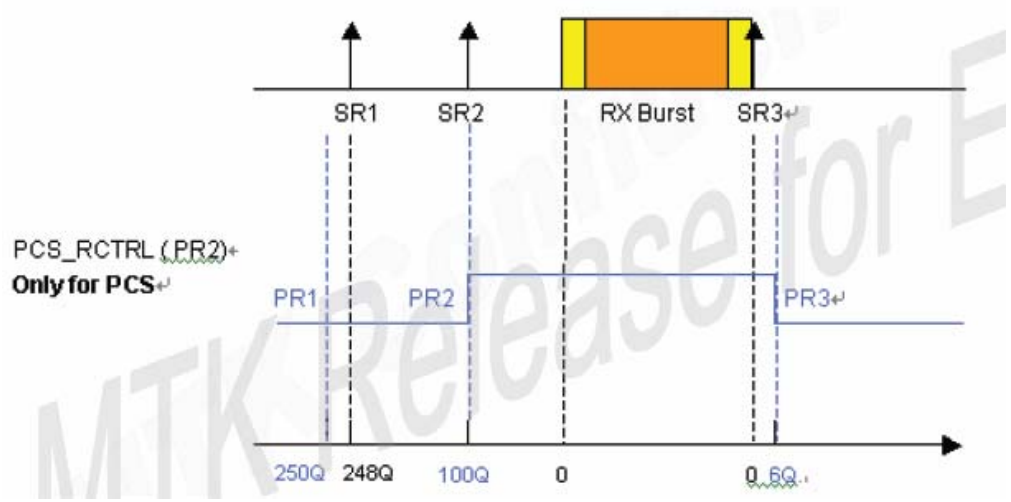
Terminal No.	Terminal Name	Terminal No.	Terminal Name
(1)	GSM900 Rx	(8)	GSM1800/1900 Tx
(2)	GSM900 Rx	(9)	Vc2(GSM1800/1900 Tx)
(3)	GSM1800 Rx	(10)	GSM900 Tx
(4)	GSM1800 Rx	(11)	Vc1(GSM900 Tx)
(5)	GSM1900 Rx	(12)	Vc3(GSM1900 Rx)
(6)	GSM1900 Rx	(13)	ANT
(7)	GND	(14)	GND

Switch Mode	Vc1(GSM900 -Tx)	Vc2(GSM1800/1900 -Tx)	Vc3(GSM1900 - Rx)
GSM900 - Rx	Lo(0.0-0.1V)	Lo(0.0-0.1V)	Lo(0.0-0.1V)
GSM1800 - Rx	Lo(0.0-0.1V)	Lo(0.0-0.1V)	Lo(0.0-0.1V)
GSM1900 - Rx	Lo(0.0-0.1V)	Lo(0.0-0.1V)	Hi(2.4-2.8V)
GSM900 - Tx	Hi(2.4-2.8V)	Lo(0.0-0.1V)	Lo(0.0-0.1V)
GSM1800/1900 - Tx	Lo(0.0-0.1V)	Hi(2.4-2.8V)	Hi(2.4-2.8V)

The GSM900 and DCS1800/PCS1900 input port matching impedances are 50 ohm from PAM(RF3166).

The GSM900, DCS1800 and PCS1900 (Balance) output port matching impedance are 150ohm to Transceiver (MT6120).

The Next Picture is for RF Receiving Timing of BSI and BPI.



<Single Slot RX Event with Timing Requirement>

<BSI Interface>

In order to simply the serial control mechanism, and achieve best usage of BSI resources. Each burst received, there are three generic timing defined (SR1/SR2/SR3) to send 3-wire control commands to transceiver. Usually 1'st BSI event(SR1) is used to warm up the synthesizer and set its N-Counter to lock the operation frequency. The 2'nd BSI(SR2) is used to set the receiving amplifier gain, received mode and operation band of transceiver. The 3'rd BSI(SR3) is used to command transceiver entering idle mode. All bands(GSM/DCS/PCS) share the same timing.

<BPI Interface>

In order to simply the parallel control mechanism, and achieve best usage of BPI resources. Each burst received, there are also three generic timing defined(PR1/PR2/PR3) to send HW Control signals to RF Module. In other words, There are only three timing events to trigger HW control signals changing its state. Usually 1'st BPS event(PR1) is used to activate the RF Component. The 2'nd BPI(PR2) is used to control antenna switch depend on its band. The 2'rd BPI(PR3) is used to force RF Module entering idle mode. All bands(GSM/DCS/PCS) share the same timing but could have different HW control signals.