INTEGRATED FINITE STATE MACHINE AND RF TIMING MODULES FOR VMEBUS AND VXIBUS INSTRUMENTATION

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ABSTRACT

A set of control and timing modules that provide a combination of a finite state machine (FSM) interface to the accelerator clock systems and RF resolution timing have been developed. These modules provide external process control and synchronization with accelerator events. Designed for both VMEbus and VXIbus platforms, these devices provide an integrated timing resource that has been utilized by various distributed control systems at Fermilab.

1. INTRODUCTION

Much of the timing and synchronization of the accelerators at the Fermi National Accelerator Laboratory complex is done through the use of global clock-timing systems; primarily the Tevatron Clock (TCLK) and Beam Synchronous Clocks (BSCLK). These clock signals carried on serial data links consist of a carrier (TCLK = 10MHz, BSCLKs = approximately 7.5 MHz, based on the RF frequency), onto which are encoded 8 bit events. Bi-phase Mark (modified Manchester) encoding is used. Events are decoded off the data stream and delays timed using the carrier. Beam synchronous clocks exist for almost all of the major accelerators at Fermilab.

In addition, primary machine parameters, such as the Main Ring and Tevatron accelerator dipole magnet currents, are transmitted on another serial link called the Machine Data (MDAT) link. MDAT data frames are also encoded using Bi-phase Mark, however, no continuous carrier is provided. Data frames on the MDAT link are 24 bits in length, including an 8 bit data frame type identifier and 16 bit data value.

These clocks are distributed throughout the accelerator complex via a system of repeaters and fan-out modules, and are used by a wide variety of control and timing modules and systems.

2. UNIVERSAL DECODING RESOURCE

The initial motivation for this project was the pending retirement of the Unibus Clock Decoder [1]. This module, which resided in a PDP-11 computer, was responsible for receiving and storing Tevatron Clock event data. Data received was then distributed over Ethernet for transfer to the accelerator control consoles. For compatibility with previous system development efforts, a VMEbus replacement for this module was desired.

For the VME/VXIbus system designer there was also the desire to use a single module to receive and decode the various clocks described above. This would, of course, reduce the amount of crate space used, as well as eliminating the need for managing module inter-activity.

In response to both of these requirements, a universal decoding module was designed. This first module was most aptly named, the VMEbus Universal Clock Decoder (VUCD) [2].

3. SYSTEM ARCHITECTURE

The VUCD can decode and process the TCLK, a BSCLK, and MDAT simultaneously. The overall module architecture is shown in figure 1 below.

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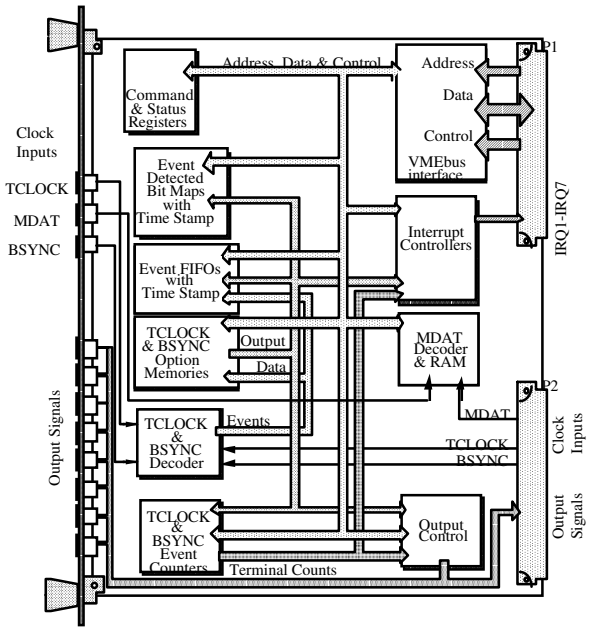

Figure 1. VUCD Block Diagram

The major components of the module can be divided into two functional subgroups; *Event Reporting*, with features similar to those found on the Unibus Clock Decoder and *Process Control,* which is primarily used for control system and instrumentation applications.

Event reporting features include:

- Event FIFO memory and free-running time stamp counter with programmable time-base (1 KHz - 1 MHz).
- Two commercial interrupt controllers (MX68C153) used for immediate event interrupts.
- One custom, FIFO-based, interrupt controller, which is preceded by event scalers. This controller is used for generating interrupts after a programmed number of event occurrences.
- MDAT memory, which hold the current machine parameter values.
- Two independent event bit-map memories, one for TCLK and one for a BSCLK. These are 16 bit x 16 bit matrices which record all incoming event occurrences. Automatic clear on read and time stamp support are also provided.

Process control features include:

- Two independent RAM-based finite state machines (FSM), one for the TCLK and one for a BSCLK.
- Output control logic for processing FSM outputs.

3.1 I/O Configuration

The clock inputs are taken either from the front panel or the rear P2 connector of the card. Outputs generated from the TCLK or the BSCLK (shown as BSYNC), can also be presented to the front panel or to the P2 connector. Outputs are predominantly used for external instrument timing or triggering.

All outputs on the P2 match VXIbus TTLTRGn* assignments and only require output driver replacement for specification compatibility.

3.2 RAM-Based Finite State Machines

The core components of the module are the two RAM based finite state machines. Figure 2 shows the basic feedback mechanism which is used for state machine operation.

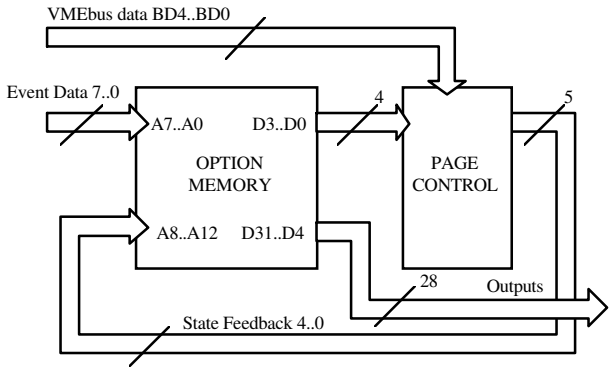

Figure 2. RAM-based Finite State Machine

Each FSM consists of two elements: the Option Memory (FSM RAM) which holds a list of immediate actions to be completed when a particular clock event is decoded and the Page Control Logic which contains the state register. When a particular event is decoded and all programmed actions are completed, the new state, defined by the lower four bits of the active memory location, is placed in the state register. A change in the state register value forces the Page Control Logic to point to a different section of memory and therefore an entirely different response configuration for the incoming clock events. The FSMs for the TCLK and BSCLK operate independently from one another.

As shown in Figure 2, the VME/VXIbus can force the FSM to a particular state in between clock events. This capability can be used to configure a FSM with a hold state and having the exit from the hold state under program control. Additional control of the FSM is also provided by allowing the VME/VXIbus to suspend event input into the FSM. VME/VXIbus actions are arbitrated to avoid collisions with clock events.

Note that there is an extra line coming from the VME/VXIbus interface into the page control. This allows for programmed transition into anther state machine stored in a different bank of memory. This effectively doubles the number of possible states from 16 to 32.

These FSMs can operate very rapidly as TCLK event spacing can be as little as 1.2 µs.

For a more detailed example of a RAM Based FSM see reference [3].

3.3 Event Triggered Actions

Event triggered actions can either occur automatically or are programmed into the FSM RAM.

Automatically occurring actions include the following:

- Marking the event in the event bit map.
- Updating system status.

Programmed actions include the following:

- Writing the event and current time stamp into the FIFO memory.
- Resetting the time stamp counter.
- Counting the event and automatically generating an interrupt on terminal count (often used for process scheduling).
- Generating an immediate interrupt.
- Generating an output pulse.

- Setting or re-setting an output level.
- Changing FSM state as outlined above.

3.4 MDAT data storage

All current machine parameter values received from MDAT are stored in a dual port memory for immediate access.

3.5 Combined FSM Output

As described above, the two state machines, operate independently from one another. The FSM output control bits, however, feed a common output logic block. This provides a mechanism for providing RF synchronous outputs following a pre-determined TCLK event sequence.

The BSCLK resolution is 132 ns (RF frequency / 7). To provide RF resolution timing two more modules were developed as described below.

4. RF RESOLUTION TIMING SUPPORT

4.1 VXI-UCD

The first module to be built with RF resolution timing was a "C sized" VXIbus card called the VXI Universal Clock Decoder (VXI-UCD) [4]. The core of VXI-UCD is identical to the VUCD, however, there have been some significant features added to the board. Among them are:

- 8 channels of independent event delay timers (time-base options: TCLK, BSCLK, VXIbus CLK10, External to 15 MHz).
- Added interrupt based on programmed MDAT frame type arrival and
- RF based Pulse Pattern Generator (PPG).

4.1 RF Pulse Pattern Generator

The PPG consists of two elements, a 64K x 8 pattern memory and a programmable address counter which is used to index into the memory. Each bit position in the memory can be thought of as a column in a table which is either a "0" or a "1". Each of these columns can be directly mapped to one of the outputs. Pattern generation is initiated by programming a start address in the address counter and an end address in the address counter. Once a trigger is received by the address counter the pattern that is programmed in the memory is then presented to the output(s).

The address counter can be programmed to play a selected number of pattern cycles, or can free-run until triggered or programmed to stop.

The frequency that this PPG operates in is the range 35 - 53 MHz which corresponds to the frequencies of operation for the Fermilab accelerators.

4.2 VMEbus RF Timer

In order to provide the same functionality as the VXI-UCD in a 6U VMEbus form factor, a third card was made, the VMEbus RF Timer (VRFT) [5]. The VRFT combined with a VUCD provides the same essential capabilities as the VXI-UCD.

4.3 Example usage

An excellent example of the use of the VXI-UCD is described below (excerpt from reference [6]).

The upgrade of the Fermilab Linac from 200 MeV to 400 MeV has reduced the losses in the Booster due to space charge effects, but the increased beam current causes greater coupled bunch mode instabilities. The challenges associated with designing a coupled bunch mode damper for the Booster are a large dynamic range, a

fast sweeping RF system, and a large spread in tunes through the cycle. A digital system is ideal for handling these problems; therefore, digital bunched beam dampers were designed. The damper configuration is shown in Figure 3. It consists of a common mode rejection front-end, digitizing units, fast memory, a D/A unit, and power amplifiers. All of the components, except for the power amplifiers, are VXI compatible and can be controlled with a personal computer or any other VXI control system.

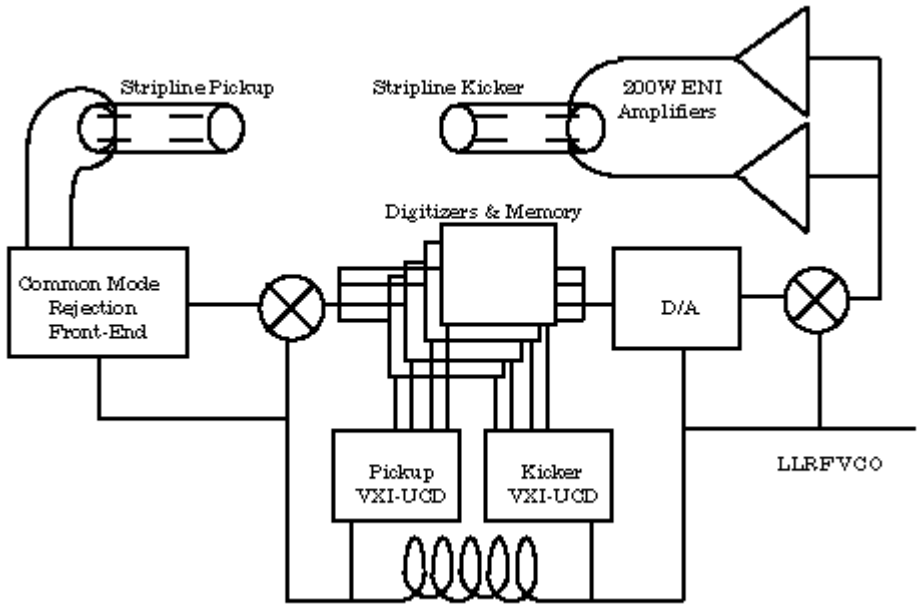

Figure 3: Block diagram of Fermilab Booster transverse digital damper system.

The RF accelerating voltage in the Booster must ramp from a frequency of 37 MHz to 53 MHz in a cycle time of 33 ms, and the non-linear frequency ramp has a peak slope of 1 GHz/s near the beginning of the cycle. The revolution period varies from 2.8μs to 1.59μs. To maintain feedback on the proper bucket, the processing system must handle 1.21μs of delay change quickly.

The VXI-UCD cards maintain the proper delay by remaining locked to the beam. The waveform generator memory is programmed with an interleaving pattern and clocked with an external reference which is the beam reference oscillator. This pattern triggers the digitzers to sample the beam and also triggers the digitizers to send signal to the kicker. The pattern can also be fine tuned to allow for single bucket precision in adjusting the delay.

VXI-UCD cards also act as interpreters of the laboratories global trigger system. These triggers are used to control the start and stop times of the system as well as external gates which turn of the signal during delicate times of the acceleration cycle.

5. POSSIBLE IMPROVEMENTS

Possible improvements for these modules include:

5.1 State Tracing

State tracing capabilities can be especially useful for process control and interfacing. This feature requires storing not only event and time stamp information, but state and possibly state transition information as well.

5.2 Enhanced Multi-processor Support

To improve support for multi-processor systems, an effective method for providing several message queues could be employed. This could include state tracing information as described above.

5.3 Improved PPG output phase adjustment

Improved linearity of the PPG output phase adjustment circuitry would be beneficial, as the current circuitry shows significant phase variation over the full frequency range of operation.

6. CONCLUSION

These modules have proven to be an effective tool for the Fermilab VME/VXIbus system designer. They provide a seamless interface to the accelerator timing systems and provide RF resolution synchronization capabilities as well.

7. ACKNOWLEDGMENTS

We wish to acknowledge David DuPuis who did the layout and prototype assembly of all of these modules and Jay Ticku who designed several of the timer chips used on the boards. We also wish to acknowledge all of the users, whose support and encouragement helped make these modules a reality. Special thanks to Jim Steimel for providing the module usage example (4.3) for this manuscript.

8. REFERENCES

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