Part IV

System Specifications

Chapter 24

Silicon Drift Detector

Last Updated: 15 June 1995

The SVT is made of 216 silicon detectors . The silicon drift detector operates in a manner analogous to gas drift detectors. Fig. 1 shows a schematic layout that illustrates the geometry and operation of semi-conductor based drift chambers.

A 4 inch, high resistivity (around 3 KΩ/cm) n-type Si wafer is used as a substrate. Field shaping electrodes are constituted of p-type material implanted symmetrically on both surfaces in a regular strip pattern. The pitch between cathodes in the STAR SDD prototypes is 120 μm. A high voltage gradient (up to 600 V/cm) applied to these shaping electrodes fully depletes the Si thus creating a deep potential well that attracts free electrons produced by the passage of charged particles through the detector. The surface electrodes are symmetrically connected to a voltage divider network that produces an independent electrostatic field parallel to the surface of the wafer. The field transports the electrons towards the edge of the detector where signals are read out on a segmented anode (pitch = 250 μm). Under suitable conditions, the electron drift velocity is constant, so that a measure of the drift time is equivalent to a measurement of the position in the drift direction. During drift, with typical speed of 1 $cm/\mu s$, the initial cloud of electrons expands due to diffusion and Coulomb repulsion. The charge thus read out is shared among few anodes (2-6) over a somewhat extended time period (few 100 ns). Charge sharing techniques can then be used to determine the original position of the cloud to an accuracy better than the anode pitch. Prototypes of this technology were used in the CERN NA45 (CERES) experiment and have been found to have excellent position sensing precision and resolution ($<$ 10 microns). This remarkable position resolution can be achieved at a small fraction of the cost associated with a pixel detector of equivalent resolution.

The SVT drift detectors are based on the above model. Prototypes are currently designed and fabricated at BNL. A bi-directional drift detector with minimized guard area ('mini guards') will be used in the final SVT design to allow operation with a maximized active area at a reduced voltage.

Table II gives the specifications and critical parameters for the Silicon Drift Detectors to be used for the SVT.

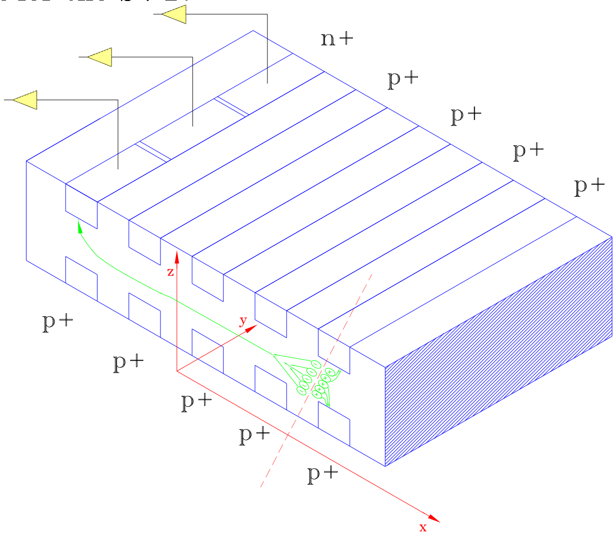

Figure 24.1: Functional diagram of generic n-type Silicon drift detector

parameter	**SDD**
number of SDD for SVT	216
number of channels for SVT	103,680
SDD size	6 x 6 cm
number of channels per SDD	480
anode pitch	250 μm
number of cathode strips	500
cathode pitch	120 μm
number of external voltage lines	50
maximum voltage on external line	2500 V
external voltage line pitch	1.2 mm
min. signal in pixel	500 e
max. signal in pixel	200,000
min. signal on anode (integrated)	6000 e
max. signal on anode (integrated)	360,000
minimum ionizing potential	24,000 e
$<$ signal length in time domain $>$	200 ns
$<$ signal spread in anode domain $>$	1.25 mm
cluster size	40 pixel
$<$ occupancy $>$ in central Au+Au	3.5%
unsuppressed event size	13 MByte
zero suppression	yes
suppressed event size	505 kByte
test pulse injection	yes
charge injectors per wafer	6
separation between injector lines	1 cm
rate of charge injection	2 per minute
position resolution (time domain = y)	25 μm
position resolution (anode domain = x)	25 μm
power requirement	$<$ 2 kW

Table I: SDD specification and critical parameters

Chapter 25

Electronics

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This section gives specifications for the main electronics components associated with the SVT. Table III summarizes the specifications for the on-detector front end electronics.

The charge produced by the passage of ionizing particles through the bulk of the detectors is collected on segmented anodes, with a pitch of 250 μm, on the far edges of the detector. The 240 anodes on both ends of the detector are wire-bonded to an electronics carrier which houses bipolar preamplifier/shaper chips (PASA) and a CMOS based switch capacitor array (SCA) used as an analog memory pipeline.

In 300 μm of Silicon a minimum ionizing particle traversing at normal incidence will generate 24,000 electrons. However, diffusion and Coulomb repulsion limits the signal in a single electronics pixel to not more than 5,000 electrons. The incoming signals from the SDD are preamplified and shaped in the PASA. The intrinsic noise of the readout chain does not exceed 400 rms electrons, leading to a signal to noise ratio of 60:1. Detector response simulations show that this ratio is required to achieve excellent position resolution. The complete readout chain is designed to have a dynamic range that allows measurement of the energy deposition of minimum ionizing particles (1 MIP) as well as low momentum ($\sim$ 100 MeV/c) protons ($\sim$ 30 MIPs).

The shaped signals are stored in a switched capacitor array as a function of arrival time. The SCA is clocked at a frequency of 27 MHz and has a depth of 128 time-buckets. It is operated as a circular buffer to avoid the loss of drift space implied by the 1 μs Level-0 trigger delay.

Each PASA and SCA chip hosts 16 channels. The chips will share an on detector Hybrid mounted on a 2 cm wide Beryllia substrate to reduce radiation length on the detector. The inclusion of the SCA on the detector provides multiplexing capabilities leading to a drastic reduction (factor 240) of the number of cables to be attached to the detector and hence not only simplifies the design but allows a reduction of the effective detector mass.

The SCA output is subsequently transmitted to the readout boards (RDO) located at the TPC end caps. Each readout board houses ADCs and a fiber link driver used to send the 10 bit ADC output to the DAQ. Part of the RDO is a power conditioning sector which distributes all required low voltage power levels.

High voltage will be supplied to voltage dividers via separate HV lines. The dividers are located at the water manifolds on each side of the SVT. Each divider board serves 1/2 ladder, which results in 72 lines.

parameter	**specification**
max. size per carrier	56 cm x 2 cm
cross talk	$< 1\%$
clock speed	27 ± 3 MHz
noise requirement	400 rms e
inefficiency	$< 0.1\%$
radiation hardness	up to $10^{11}\gamma$'s / cm^2 RHIC year
maximum power consumption	< 10 mW/channel
dynamic range (max. ion. to min. ion.)	40:1
S/N ratio (peak signal on single anode to system noise)	60:1
linearity for minimum ionizing particle	1%
linearity for maximum ionization	4%
redundancy	10%
readout rate	100 Hz

Table I: A summary of system requirements for SVT front end electronics

25.1 PASA

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Table IV summarizes PASA specifications.

parameter	PASA
channels per die	16
shaping time	34 ns peaking
maximum signal swing in mV	1500
output signal swing in mV	2200
operating output voltage range in mV	800-3500
dynamic range (max.signal/min.signal)	10:1
dynamic range (max.signal/noise)	600:1
maximum power consumption	5 mW/channel

Table II: PASA specifications

25.1.1 Cross Talk

Requirement:
The electronic cross talk should not exceed 1%.

Justification:
Rough estimates show that at a level of 2-3% the cross talk starts to effect the position resolution.

25.1.2 Linearity

Requirement:
The constraint on the linearity has to be defined for a low level signal. For a low level signal the linearity should be better than 1%. For higher level signals the linearity can increase up to 4%.

Justification:
Nonlinear response in the high level signals can be corrected. A non linearity in the minimum ionizing response range will effect the position resolution.

25.1.3 Shaping Time

Requirement:
The maximum peaking time will be 40 ns.

Justification:
The maximum peaking time is based on the minimum proximity of 2 independent signals that have to be resolved sufficiently (pulse pair resolution).

25.1.4 Input/Output Capacitance

Requirement:
The input (parasitic) capacitance due to the PASA will be .2pf to .3pf, which is similar to that expected external to the PASA (Hybrid and SDD anode node). The bipolar process can minimize noise effectively for such capacitance levels.

Justification:
The device has to meet the input and output capacitance of the connecting external components (SDD in, SCA out) without degrading S/N performance.

25.1.5 Inefficiency

Requirement:
Inefficiency should be held below 0.1%.

Justification:
The inefficiency of the electronics has to be negligible compared to the STAR detector inefficiency.

25.1.6 Power Consumption

Requirement:
The power consumption of the PASA should not exceed 5 mW/channel.

Justification:
The maximum power consumption is based on the layout and water throughput of the designed water cooling system. The readout chain should not induce a temperature gradient on the active area that exceeds 0.1^{o}C.

25.1.7 Adjustable Gain

Requirement:

The maximum gain will be .007 mV swing/electron for 1 MIP step charge, adjustable downward.

Justification:
This is high enough to meet system S/N, but adjustable downward to prevent excess output levels and distortion in the event of higher SDD charge production than expected.

25.1.8 Signal Output Range

Requirement:
The maximum signal swing expected is 1500 mV, due to an input Gaussian(σ=25 ns) dq/dt having total charge=360,000 e. The expected signal swing expected with a 1 MIP step charge is 165 mV. The maximum (not to exceed) output range is -.8 to 3.5 V.

Justification:
The device has to have a linear response in the range of minimum and maximum ionization.

25.1.9 Dynamic Range

Requirement:
The dynamic range of the SVT electronics is defined by the ratio of the integrated maximum ionizing to the integrated minimum ionizing signal. The maximum ionizing signal the SVT is interested in is a 100 MeV/c proton, which deposits around 30 times the minimum ionizing signal. The integrated minimum ionizing signal is about 24,000 electrons in 300 μm of Silicon. This signal will spread out almost immediately after deposition (in the first 100 ns) due to Coulomb repulsion, though. The repulsion strength depends on the the size of the electron cloud and increases successively for higher ionizations. Coulomb repulsion at 30 times minimum ionizing spreads the cloud integrated for a single anode by a factor 2 which leads to a maximum signal on a single anode of at most 360,000 electrons. So the signal swing in the preamp has to accommodate a dynamic range of 15:1, if defined by maximum signal in electrons on one anode. If we assume that the 360,000 electrons form a Gaussian shaped signal, the maximum signal in one anode corresponds to 1500 mV. A δ-function minimum ionizing signal would deposit 160 mV. Thus, the dynamic range defined as maximum signal to minimum signal is 1500/160 = 10:1. If we compare the maximum signal to the noise level at the output we have to divide 1500 mV by (350 electrons$\times$160 mV/24,000 electrons) which yields a dynamic range of 600:1. Both numbers are listed in the PASA requirements.

Justification:
The device has to accommodate the signal levels for maximum and minimum ionizing particles.

25.1.10 Type of Electronics

Bipolar Design, SHPi Process by Tektronix
In order to achieve the same speed and noise characteristics one would have to run transistors at a much higher current in a CMOS design. The power consumption would rise from currently 2mW/channel to around 10-15 mW/channel. Also, at low capacitance level CMOS characteristics are worse than the bipolar characteristics.

25.1.11 Size and Channel Count

The size of the PASA should not exceed 2 mm by 3.5 mm. The PASA should not be packaged, rather the bare die should be mounted on a Hybrid substrate. Each die should carry 16 channels with a pitch corresponding to the detector anode pitch (250 μm). The size of the PASA is one of the components that determine the superlayer overlap area. This overlap has to be optimized to the smallest possible area. PASA and SCA will be mounted on Hybrid, so both dies do not have to be packaged. The size of the Hybrid is adjusted to the size of the detector. The size of the die has to allow bond pads between adjacent PASA.

25.2 SCA

Last Updated: 15 June 1995

Table V summarizes SCA specifications.

25.2.1 Sampling

Requirement: *Sampling Rate and Procedure*
The SCA shall sample PASA output data when the R/W control signal is active in the W (write) state. The SCA shall continuously sample input data on all channels simultaneously at a rate of 27$\pm$3 million samples per second. The newest data shall overwrite the oldest data. Switching the R/W control signal to R (read) will stop SCA sampling and freeze the last 128 samples pending readout. Timing for this is controlled by the Trigger subsystem.

Justification:
The sample rate is determined by physics resolution requirements. The need for continuous sampling arises because there is insufficient time after an event occurrence for the trigger system to generate a write trigger signal. Timing for the switching of the R/W signal to read is controlled by the Trigger subsystem because the Trigger subsystem has sampled and determined the likelihood that an event is interesting using fast detectors before the charge from that event has completely drifted through the SDD.

Requirement: *Write Pointer Reset*
The write pointer shall be reset to one cell called the fiducial cell at the start of a write cycle.

Justification:
This permits tracking and correcting stored charge pedestals.

25.2.2 Readout

Requirement: *Sample Depth*
The SCAs shall have a depth of 128 time samples.

Justification:
The depth is dictated by the electron cloud spread.

parameter	**SCA**
die size (target)	4.2 x 3.6 mm
voltage supplies (V_{dd1}, V_{dd2})	+5V±5% anal./anal.return, +5V±5% dig./dig.return
extreme input voltage tolerance	-0.4 to V_{dd}+0.4 V without device degradation
input capacitance	Maximum 10 pf , 5 pf desired at signal input
channels per die	16
maximum SCA depth	128
sample rate	27 ±3 MHz (integer mult. of RHIC bunch crossing).
readout rate	3 Msamples/s (100 Hz Hybrid readout rate).
crosstalk, any channel pair	-50 dB, minimum
output noise in a 20 MHz band	< 1 mV rms, all sources
maximum power consumption	< 3 mW/channel
large signal input signal swing	min. 2.2 V linear range
operating input voltage range	0.8 to 3.5 VDC
small signal diff. linearity error	< 1% 0-0.5 V linear swing range
large signal diff.linearity error	< 4% 0-2.0 V linear swing range
power supply rejection ratio	≤ 45 dB
latchup immunity, any I/O pin	±40 mA (JEDEC method)
current overdrive, I/O < 0 or > 5V	±20 mA with power applied (JEDEC method)
input control signal logic levels	CMOS compatible
input control signals	Analog and digital reset, read/write, two token inputs (internally ORed), PECL levels preferred
clock load	max. 2 pf at clock input; max. 0.5 μA over clock V range
clock voltage range	diff. PECL compatible, 0 level <3.4 V, 1 level >4.1 V With $0 \leq V_{in} \leq V_{dd}$, $I_{in} \leq <$ 0.5 μA
clock control	R/W share single clock input. State of R/W input monitored. Number of clock pulses metered externally.
output control signal	Only signal is Token Out. 16 clocks during read after token input. Token Out level is CMOS.
output drive capability	Analog, tri-state. Must drive a 2.2V swing into a 30 pf load when active. Settles to < 0.1% within 125 ns min. 10 MΩ out. imp. and <1 pf out. cap. (inactive)
DAQ timing and control	Continuous data sampling at clock rate during write. Circular overwrite. Reset to clock cell after digital reset R/W line switched to write
data readout control	Sample count reset when R/W switched to read. Upon token input, 1 ch. read in a clock interval Sample count indexed and token output asserted
ESD protection	2KV min., all pins, human body model (JEDEC)

Table III: SCA specifications and requirements

Requirement: *Stored Charge Retention*
Charge leakage or injection on each SCA capacitor shall be less than .05% during the readout interval ($\approx$ 10 ms).

Justification:
The stored charge leakage requirement arises because the charge must be retained on a capacitor to within 1/2 least significant quantization bit independently of when in the readout cycle it is actually read. This could be as long as 10 ms.

Requirement: *Readout Procedure*
The SCA shall be in read mode when the R/W signal is active in the R (read) state. Readout shall be initiated when a token is received the two TI (token input) line. Readout shall occur at the clock rate (approximately 3 MHz or 330 ns per sample). Channel 1 through channel 16 are multiplexed onto the analog signal output line. After each channel has been read out, the TO (token output) line shall go active enabling passing of the token to the next SCA.

All channels shall read out the same sample number while the token is active. A channel read consists of switching a channel capacitance array into the readout operational amplifier (op-amp) which drives the analog signal bus line for one clock interval. When the token is not active, the SCA amplifier shall be disconnected from the analog signal output line. When disconnected impedance shall be at least 10 MΩ.

Justification:
The readout clock rate is close to the minimum needed to operate the SVT at the required 100 Hz service rate ($<$10 ms readout time is available). The Hybrid area is limited. Multiplexing channel analog signal output lines is needed to reduce the number of traces and minimize the number of pads on the Hybrid. Token passing permits SCA controls to be daisy chained. This makes external multiplexing switches unnecessary and reduces the number of control signals, Hybrid traces and power consumption.

Requirement: *Multiplexing*
Each SCA shall be connected to (multiplexed with) 14 other SCAs (fifteen in all) and shall feed into a common low gain amplifier to an analog signal output line. Each SCA has 16 channels. This provides a total multiplex ratio of 240:1. Only one SCA, the one with the active token, shall drive the amplifier at any time.

Justification:
Each anode side of the SDD is served by one Hybrid and has 240 channels. The number of channels per SCA was set to 16. This is a compromise among issues of cost, production yield and chip size for the best available chip feature size (1.2

μm) technology. The 240 channels will require 15 SCAs of 16 channels each. The 15 SCAs are multiplexed onto a common analog signal line to reduce the number of Hybrid signal lines from 15 to 1. A Hybrid multiplex ratio of 240 to 1 reduces power and size by avoiding the need for 16 op-amp drivers.

Status:
Under discussion. ASIC includes correction by default.

Requirement: *Token Passing*
The first SCA shall receive an external token on a TI line as a START signal. All TOs of each SCA but the last are connected to the TI input of the following SCA. The START signal shall be initiated after every 240 readouts.

Justification:
Token passing simplifies the control structure and minimizes the number of interface signals in a interconnection-limited area.

Requirement: *Readout Termination*
The readout of each SCA shall be controlled by externally metering the clock during readout. (It is possible to repeat the readout sequence indefinitely, though the storage capacitor charges will degrade with time.)

Justification:
The readout may be interrupted at any time. If there are fewer than 4096 clocks per SCA, then all read values will be unique. This is desirable because the SCA can be returned to sampling (placed in the write mode) earlier to improve the event service rate. External readout control simplifies the SCA design and permits more flexible control.

25.2.3 Settling Time

Requirement: *Readout Settling Time*
Outputs shall settle to within 0.1% of final value.

Justification:
The physics requires 10 bits of accuracy, which is roughly equivalent to 0.1% of the largest signal value.

25.2.4 Cross Talk

Requirement: *Induced Signal*

Cross talk is the signal induced on an inactive channel (source held inactive) while one or more channels are driven at peak signal swing. The measured signal swing shall be $< 1\%$ of the peak signal swing applied to all other inputs singly or jointly.

Justification:
Rough calculations show that at a level of 2-3% crosstalk starts to cause degradation of position resolution.

25.2.5 Linearity

Requirement: *Small Signal Linearity*
When a signal swing of less than 10% of the SCA signal range is applied to the SCA input terminals the resulting differential readout signal swing shall deviate from linearity by less than 1%.

Justification:
Good linearity is needed for the range near minimum ionizing response to avoid degrading position resolution.

Requirement: *Large Signal Swing*
When a signal swing of 10% of the SCA signal range or larger is applied to the SCA input terminals the resulting differential readout signal swing shall deviate from linearity by less than 4%.

Justification:
Linearity for large signals (where S/N ratios are larger) can be corrected. Therefore the large signal linearity specification can be more relaxed than small signal linearity.

Requirement: *Differential Gain*
The ratio of the output signal swing to input signal swing over the SCA signal range shall be between 0.9 and 1.1, but shall be within 0.1% from channel to channel. Preferred sense of the gain shall be the same as for the PASA response to charge magnitude at the PASA input.

Justification:
The range of driver amplifiers and ADC is limited. A range of 0.9 to 1.1 is needed to avoid signal overload while preserving optimum dynamic range. A tolerance of 0.1% is needed to be able to measure charge accurately without correcting for each channel of the SCA device. The SCA output should vary directly as the amount of charge measured at the PASA input to take advantage of lower power dissipation afforded by low occupancy. Thus if the PASA inverts the signal such

that a high PASA output voltage represents low charge, the differential SCA gain should be negative so that a high input voltage is converted to a low input voltage to represent low charge.

25.2.6 Maximum Input Voltage

Requirement: *Overdrive*
The largest signal voltage permitted without causing latchup while the power is on shall be 0.4 V above the supply voltage (nominally 5 V). The SCA is not required to meet other functional requirements at this input level. The smallest signal voltage permitted shall be 0.4 V below analog ground. The SCA is not required to meet other functional requirements at this input level.

Justification:
Protection from transients.

25.2.7 Operating Input Voltage

Requirement: *Normal Voltage Levels at Input*
Input voltages shall normally range from +0.8 to +3.5 V DC. Specifications of this section shall be met over a full scale voltage swing. A full scale voltage swing shall be 2 V and shall range from 0.8 to 2.8 V. The input shall be DC coupled to the SCA output.

Justification:
The SCA op-amp works best within the range of 0.8 to 3.5 V. The PASA output over the required dynamic range shall be 0.8 to 2.8 V. The output stage of the proposed PASA is capable of driving up to 3.5 V, though the range above 2.8 V can have significant distortion.

Requirement: *Offset Voltage Level*
The DC level out of the SCA when a voltage representing a null charge level from the PASA is applied at the input shall range from 700 to 900 mV and shall have a maximum fluctuation of 0.35 millivolts RMS across samples within any channel. As a goal, the offset fluctuation from channel to channel or between SCA devices shall not exceed 0.5 mV RMS.

Justification:
This requirement avoids unnecessary pedestal corrections by keeping pedestal fluctuations below the system noise level. By keeping the offset below .35 mV rms the pedestal fluctuation for each channel can be the same for all samples. If channel to channel and inter-SCA offset fluctuations can be kept below 0.5 mV, then pedestal

correction will be a constant number for the entire system and so would be trivial and not require any special hardware (e.g., DAQ ASICs).

25.2.8 Power Dissipation

Requirement: *Maximum Power Dissipation*
Power dissipation shall not exceed 50 mW ($\approx$3 mW/channel).

Justification:
Detector performance is highly temperature sensitive and the ability to conduct waste heat is limited by physical factors (e.g., restrictions on size, radiation length, flow rate and temperature rise of coolant).

25.2.9 Clock Requirements

Requirement: *Clock Signal Definition*
The SCA clock shall be a single differential modified PECL line which carries the write clock ($\approx$27 MHz) during sampling and the read clock ($\approx$3 MHz) during readout.

Justification:
Differential PECL (positive emitter coupled logic) levels are used because of low switching levels (and therefore reduced EMI), high speed capability and the ability to drive a large number of SCAs on a single line. Different rates are used to provide the proper clocking frequency on a single line to avoid additional traces (2 traces per differential clock line). Previous SCA devices have used similar clock drives so the risk is low. The modification required to the PECL level is addressed in the next paragraph.

Requirement: *Adjustment to PECL State Voltages*
A logic 0 shall be less than 3.4 V. A logic 1 shall be greater than 4.1 V.

Justification:
The definition of PECL levels includes an adjustment because the SCA operates at 5 V rather than the standard 5.2 V normally used for PECL.

25.2.10 Input Capacitance

Requirement: *Capacitance Across Input Terminals*
The capacitance across the input terminals shall not exceed 10 pf.

Justification:

The PASA ability to drive capacitance at low power levels and wide bandwidth is limited. Low capacitance reduces the drive current that produces noise and can, at some level, contaminate the high gain input of the PASA

Requirement: *Inactive Drive Output Characteristics*
The output pad isolation to analog signal line shall be at least 10 MΩ and not more than 1 pf capacitance to ground or any power line when the corresponding channel is not active.

Justification:
This is typical of what CMOS circuits can achieve, so the risk is low. It is necessary because 15 SCA devices are daisy chained to the analog signal bus. Any load from an inactive channel must be driven by the active channel.

Requirement: *Active Drive Characteristics*
The output of the active signal channel shall be capable of driving a 30 pf capacitance (inactive outputs, buffer op-amp input and trace capacitance).

Justification:
The output must reach final levels by the end of the channel read interval while driving the necessary circuit loads. Failure to settle within specified time could degrade system accuracy. Because of ADC settling time, the full settling interval of 150 ns must be shortened.

25.2.11 Noise

Requirement: *Static SCA Noise at Each Storate Cell*
Noise is measured by applying a DC level to the input of the SCA across a large capacitor. When the SCA is alternatively written and read at or near the system write and read clock frequencies, the average output noise averaged over 256 cells shall not exceed 0.5 mV RMS. No one cell shall have noise exceeding 1 mV RMS. The noise is calculated by measuring total output noise and subtracting in quadrature measurement noise (ADC and test jig components which cannot otherwise be eliminated from the measurement).

Justification:
The SCA noise should not contribute a significant amount to total system noise. The original bandwidth at the sampling frequency is ≈20 MHz.

25.2.12 Input Aperture Time

Requirement: *Rise Time*

The time it takes the stored charge to rise from 10% to 90% of its final value shall not exceed 3 ns. (This may be measured with a fast rise time pulse applied to the input with delayed trigger. By incrementally delaying the pulse and observing the effect on the output measurement between samples, the rise time can be determined.)

Justification:
The time it takes to charge the input capacitor should not affect peaking time. 3 ns is of the order of 10% of peaking time and should therefore have negligible effect on position accuracy.

Status:
to be reviewed

25.2.13 Size

Requirement: *Chip Dimensions*
The maximum chip size is 3.6 mm by 5.0 mm.

Justification:
3.6 mm is dictated in the circumferential direction by available room on the Hybrid.

25.2.14 Power Supply Voltages

Requirement: *Number of Voltages and Voltage Levels*
The SCA shall operate on two 5 V inputs, one for analog circuitry and one for digital circuitry. Both voltages are referenced to separate grounds, i.e., analog and digital.

Justification:
Limiting to 2 operating supply voltages avoids multiple power supply runs to the chip through areas where the number of available lines are severely limited. Also, the two supply concept has been used in past designs successfully, so represents a low risk. Two supplies are the minimum needed to assure adequate decoupling between noisy digital switching circuits and charge sensitive analog circuits.

25.3 Hybrid

Last Updated: 15 June 1995

25.3.1 Function/Description

Requirement:
A multi-chip module that inputs signals from a SSD and outputs amplified and shaped signals to a carrier interface.

Justification:
The SSDs have no signal-drive capability.

25.3.2 Technololgy

Requirement:
Custom multi-layer thick film on ceramic substrate

Justification:
Mature technology permitting the necessary component densities.

25.3.3 Substrate

Requirement:
Beryllia (BeO)

Justification:
Excellent thermal conductivity, low radiation length, good stffness, and commonly utilized in the Hybrid manufacturing industry.

25.3.4 Dimensions

Requirement:
6 cm axial direction, 2 cm wide, 500 μm thick

Justification:
Axial dimension corresponds to Si detector length. Width is minimized to permit sufficient space for IC and passive components and signal trace routing, while still permitting overlapping of adjacent ladder assemblies. 500 μm is minimum thickness necessary to prevent extensive warping and breakage during Hybrid manufacturing. All dimensions have been minimized to minimize the additional radiation length.

25.3.5 Power Dissipation

Requirement:
Together with its associated carrier interface must dissipate less than 10mW/channel.

Justification:
The water cooling system is designed for a maximum of 1 kW (flow, pressure, tube diameter etc.) to minimize material contributions from the cooling system.

25.3.6 Operating Temperature

Requirement:
25 ^{o}C maximum controlled temperature

Justification:
Water cooling should keep temperature below 25 ^{o}C because higher temperatures cause heating of the SDDs, lower mobilities, and non linearities.

25.3.7 Accessibility

Requirement:
The on-detector Hybrid should only be accessible during detector down time (no RHIC operation), except when the control logic for a full Hybrid stick fails (960-1680 channels).

Justification:
Detector electronics replacement requires detector access. In the integrated STAR run plan the SVT information is prioritized such that access can only be granted if the SVT tracking information is degraded to a point where the TPC information is degraded as well. Simulations show that this is the case as soon as a Hybrid stick fails. A detailed access plan has to be worked out for STAR-TPC and STAR-SVT electronics.

25.3.8 Radiation Hardness

Requirement:
The electronics will not degrade the resolution requirements up to a level of 10^{11} neutrons, γ's or charged particles per cm^2 per RHIC year. The lifetime of the detector is set to be 10 years. The noise level has to be constant at any radiation level up to the level stated above.

Justification:

This results from calculations performed independently by the RHIC group (Alan Stevens) and the Los Alamos radiation group (Laurie Waters).

Status:
CMOS and bipolar specifications include radiation requirement.

25.3.9 Dynamic Range

Requirement:
The dynamic range for the Hybrid should be 40:1. Dynamic range is defined as being the highest to lowest ionizing level.

Justification:
capability of measuring 20 $\times$ minimum ionizing particles with a factor 2 headroom for fluctuations

Status:
included as specification in PASA and SCA design

25.3.10 Signal to Noise Ratio

Requirement:
the S/N ratio should be 60:1 for the amplitude anode in a minimum ionizing event. We expect around 24,000 electrons in one anode assuming no charge sharing. The noise level is therefore 400 rms electrons for the total Hybrid.

Justification:
Simulations show that the noise ratio quoted above, allows the position resolution not to degrade by more than 10%.

Status:
included as specification in PASA and SCA design

25.3.11 Position Resolution

Requirement:
The position resolution is supposed to be $\leq$ 25 μm $\times$ 25 μm. The electronics should contribute no more than 10% to this resolution.

Justification:

Primary vertex, secondary vertex, momentum and two track resolution depend on the position resolution. Above 25 μm $\times$ 25 μm the track efficiency also starts to degrade.

Status:
included as system specification

25.3.12 Redundancy

Requirement:
The cost of redundancy shall not exceed 10% of the total cost for the FEE.

Justification:
budgetary limitations

Status:
included in layout and test procedure

25.3.13 Hybrid Component: IC die

Requirement:

- 15 PASAs (44 pads)
- 15 SCAs (30 pads)
- 2 digital buffers
- 1 analog buffer

Justification:
Number of PASAs and SCAs (16 channel each) detemined by number of detector channels (240). One digital buffer needed for CMOS level signals and one for PECL level signals. Analog buffer necessary due to low capacitive drive capability of SCA output buffer.

25.3.14 Hybrid Component Specification: Passive Components

Requirement:

- 50 bypass capacitors

- 93 ink resistors

Justification:
Number of capacitors represents compromise between desired level of bypassing and limited available space on Hybrid. One resistor for biasing needed for each SCA, and 3 for each PASA. Two PECL pulldown resistors are needed, and one resistor for the analog buffer.

25.3.15 Number of Bonds

Requirement:
1500

Justification:
There are approximately 1200 die bonds and 300 Hybrid to detector bonds (240 channels bonds and 60 ground bonds). The bond number on die is determined by channel number on die. Substrate bonds reflect the layout of Hybrid logic.

25.3.16 Number of Conductor Planes

Requirement:
4

Justification:
The planes are for ground (1), power (1), and interconnect (2).

25.3.17 Conductor Material

Requirement:
Under discussion

Justification:
Under discussion

25.4 Carrier Interface

Last Updated: 15 June 1995

25.4.1 Function/Description

Requirement:
Provide the signal and power interface between the readout boards (RDO's) and the Hybrids located at each end of a carrier.

Justification:
The approximately 3 m separation between the Hybrids and readout boards necessitates the buffering of signals. Space constraints at the Hybrid and overall design simplification suggests a dedicated module to perform such functions.

25.4.2 Location:

Requirement:
One carrier interface at each end of Berrylium water channel adjacent to the end-located Hybrid.

Justification:
The location allows easy physical connection to the end-located Hybrid while permitting water cooling of carrier interface electronics.

25.4.3 Active Electrical Components

Requirement:
Digital signal buffers; analog signal drivers; thermsistors.

Justification:
Hybrid switched capacitor array IC's require five digital signals for operation. Each Hybrid drives one analog signal to the carrier interface. Carrier interface provides convenient real estate for temperature-monitoring thermsistors.

25.4.4 Power Dissipation

Requirement:
Together with the 2-4 associated Hybrids, must consume less than 10 mW/channel.

Justification:
The water cooling system is designed for a maximum of 1kW (flow, pressure, tube diameter etc.) to minimize material contributions from the cooling system.

25.4.5 Dimensions

Requirement:

2 cm wide.

Justification:
Cannot exceed width of Berrylium water channel. The RO electronics output to the SVT will be supplied through a common 50 pin IDC connector. This will supply power with 20 pins, timing and control with 10 pins, ID code input to RO with 8 pins plus 2 for reference ground, and 8 pins for 4 monitor inputs.

25.5 Readout Electronics

Last Updated: 15 June 1995

The readout electronics is responsible for the A/D conversion of the signals, intermediate buffering and possible storage of the converted data, and feeding the digital data via an optical fiber link (the HP Gigalink) to the DAQ electronics. In addition to this task, the readout electronics needs to provide regulated power to the FEE, provide timing and control signals for the SCAs on the Hybrids, and provide an interface for the trigger and slow control systems.

Requirement:
Each readout electronics will receive signals from 18 analog inputs and produce digitized values from the inputs. 24 readout electronics units are needed.

Justification:
Distribution of the front end electronics requires the use of 24 readout cards for a total of 416 analog lines from the FEE Hybrids. Therefore, each readout card needs to provide inputs for 18 analog signals.

Requirement:
The system will digitize to 10 bits with an accuracy $< 0.1\%$ of full scale, corresponding to 1 LSB for a 10 bit range.

Justification:
Justification of requirement

Requirement:
The readout electronics will accept the analog signals at a rate up to 100 full events/sec.

Justification:
STAR requirement.

Requirement:
The readout electronics will provide the digitized data to the DAQ electronics via an HP Gigalink optical fiber connection in a protocol specified by the FEE – DAQ interface document.

Justification:
STAR interface specification.

Requirement:
The readout electronics will provide an interface to the trigger system as specified in the Trigger – FEE interface document.

Justification:
STAR interface specification.

Requirement:
The readout electronics will provide an interface to the controls system via an HDLC link.

Justification:
This link will provide access to several monitors on the detectors that need to be presented to the operators to assure proper functioning of the SVT. In addition, this link provides access to an event memory on the readout electronics, so that an event can be readout via controls, or a pattern can be downloaded to the event memory for testing of the rest of the readout system. Provisions should be made for the readout of temperature sensors and motion/position sensors on the SDD ladder and a geometric ID of the electronics carrier via the slow controls.

Requirement:
The readout electronics will provide the clock and control signals for the SCAs on the Hybrids. These signals need to be driven 10 feet from the readout electronics to the carrier interface Hybrids on the ladders.

Justification:
Space constraints for the on-detector electronics requires that the control and clock signals for the SCA's be generated off the detector. The only connection to the FEE is via the readout card.

Requirement:
The readout electronics will provide for local storage of one full event. This storage can either be filled by the A/D converters or via the controls link. The event in

this storage area can be used as an alternative source for the fiber optic link. The data path will be controllable via controls.

Justification:
This feature needs to be available for testing and debugging of the readout and DAQ system.

Requirement:
The readout electronics will provide clean regulated power to the Hybrids.

Justification:
The Hybrids need +5D, +5A, -2, +6, -6 VDC. These voltages need to be generated and regulated by the readout electronics and sent to the carrier interfaces. The readout electronics require +5D, +5A, -5A, -5ECL VDC for internal operation. All voltages will be generated on the readout cards from $\pm$ 8 VDC supplied by power supplies located in the SVT racks.

25.6 Low Voltage Power Supply

Last Updated: 15 June 1995

Requirement:
24 power supplies in the SVT racks. Each provides $\pm$8 V (5 A). Regulation should be 5%.

Justification:
The Hybrids need +5D, +5A, -2, +6, -6 VDC. These voltages need to be generated and regulated by the readout electronics and sent to the carrier interfaces. The readout electronics require +5D, +5A, -5A, -5ECL VDC for internal operation. All voltages will be generated on the readout cards from $\pm$ 8 VDC supplied by power supplies located in the SVT racks.

Requirement:
72 power supplies to generate other voltages required by SDDs (E1, W0, W1, and S2). These supplies to be located in SVT racks. Each supply to provide -100 VDC. Power conditioners in the readout electronics will generate voltages required.

Justification:
The silicon drift detectors require various trimming and focusing voltages for operation. Typically W1 = -(60 - 100 VDC), E1 = -(10 - 20) VDC, S1 $\leq$ W1, and W0 = W1/2.

The low voltage power system consists of two sets of primary rack mounted supplies located in the SVT racks to deliver ± 8 VDC. Power cables connect from the racks to each RO chassis with Cinch-Jones 8 pin power connectors on each end.

The RO backplane will supply the primary power to the RO cards. Each card will have regulators to supply its power requirements. Additionally, the PTB card will have regulators to supply the power for the carrier interface which it is connected to. The regulator ICs are located near the side edge of the cards to allow sufficient conduction to the wedge clamp for transfer to cooling water.

25.7 High Voltage Power Supply

Last Updated: 15 June 1995

Requirement:
Each SDD must be provided high voltage.

Justification:
The SDD will not drift without high voltage.

Requirement:
72 high voltage power supplies with adjustable voltage range 0 to -2000 V, and stability ±0.1%.

Justification:
The silicon drift detectors need negative high voltage. Each end of each ladder is supplied high voltage from a separate source. There are 36 ladders, so 72 high voltage sources are required. Each high voltage channel connects to a high voltage divider board near a carrier interface.

LeCroy 1440 High Voltage system to provide at least 72 high voltage channels with adjustable voltage range 0 to -2000 V, and stability ±0.1%.
72 power supplies to generate other voltages required by SDDs (E1, W0, W1, and S1). These supplies to be located in SVT racks. Each supply to provide -100 VDC and sent to readout electronics where power conditioners will generate voltages required.

25.8 Monitoring

Last Updated: 15 June 1995

25.8.1 Carrier Interface

Requirement:
Each electronics carrier interface (144 total) will include provisions for the following 5 monitors: 2 temperatures on ladders (thermistors), 1 summed voltage on carrier (voltage across resistor chain), 1 SDD high voltage (to be determined), and 1 displacement on ladder (to be determined). The cabling for 3 of these monitors (all but 1 temperature) will be part of the readout electronics — carrier interface cable. The other temperature monitor will be routed with the calibration/high voltage cables to the readout electronics.

Justification:
The SDD drift times depend upon temperature, and temperature gradients on the SDDs cause nonlinearities for drift time versus position. Physical positions and dimensions are dependent upon temperature. Alignment and position of physical components of the SVT must be monitored at all times. The sensitivity required is that change that corresponds to a 10 μm contribution to the SVT position determination. Voltages on the Hybrid side of the carrier interface should be monitored. Voltages and temperature should be monitored on the readout electronics.

25.8.2 Readout Electronics

Requirement:
Each readout electronics (24 total) will contain provisions for the following 7 monitors: 1 temperature of readout boards (thermistor), 1 summed voltage on readout electronics (voltage across resistor chain), and 5 currents (to be determined).

Justification:
The proper functioning of the readout electronics requires temperature stability and stable input power.

Requirement:
Each readout electronics (24 total) will contain provisions to allow readout of the 34 monitors via Controls (HDLC).

Justification:
Each readout electronics (24 total) interfaces to 3 ladders (6 carrier interfaces). 27 monitor signals are routed from the 6 carrier interfaces to each readout electronics. Since each readout electronics also contains 7 monitors, a total of 34 monitor signals must be multiplexed and readout through the HDLC Controls interface on each readout electronics.
Multiplexing of 34 analog channels to a 12 bit Analog-to-Digital (ADC) converter on each of the 24 Power and Timing Boards of the Readout Electronics.

25.9 Calibration

Last Updated: 15 June 1995

Requirement:
Pulser system to distribute -(5-20) V, 10 μs long, pulses to the silicon drift detectors. Six (6) lines to each ladder from the pulser system.

Justification:
The silicon drift detectors must be calibrated by injecting known charge at a known time. The known charge will allow pulse height calibration. Together with the time information the injected charge leads to drift time calibration.
To be specified

25.10 Alignment

Last Updated: 15 June 1995

Requirement:
A system to monitor position of SVT with respect to STAR.

Justification:
The position of the SVT with respect to the TPC must be monitored at all times. The sensitivity required is that change that corresponds to a 10 μm contribution to the SVT position determination.
To be specified

25.11 Grounding and Shielding

Last Updated: 15 June 1995

Requirement:
statement of requirement

Justification:
Justification of the requirement.
To be specified

Chapter 26

Internal Electrical Interfaces

This section gives requirements for various interfaces wholely contained within the SVT.

26.1 Silicon Drift Detector–Hybrid

Last Updated: 15 June 1995

Requirement:
Each SDD must be electrically connected to a Hybrid.

Justification:
The ouput signals from the SDDs serve as input to the Hybrids.

26.2 Low Voltage Power – Readout Electronics

Last Updated: 15 June 1995

Requirement:
± 8 VDC from the SVT racks to the Readout Electronics.

Justification:
The Readout Electronics requires primary ± 8 VDC from the SVT racks to provide power both for the Readout Electronics and the Hybrids (through the Carrier Interfaces). The primary power will be supplied by a 50 foot cable using #12 wire and 8 pin 10 A Cinch-Jones connectors to limit the voltage drop to the RO chassis to less than 1 volt.

The power from each RO chassis to its SVT carrier interface will use two of the twisted pairs in the cable for each voltage +5D, +5A, +6, -6, and -2 VDC. The

PTB card in the RO chasis will have a 50 pin IDC conncctor. 20 pins will be used for the power and returns to increase reliability. The wire path in the cable will have two #26 wires to limit the voltage drop. The shield will be grounded on the one end nearest the common grounding point to minimize ground loops.

26.3 Silicon Drift Detector — High Voltage Power

Last Updated: 15 June 1995

To be specified

26.4 Carrier Interface – Readout Electronics

Last Updated: 15 June 1995

Requirement:
Interfaces between the Readout Electronics and the Carrier Interfaces are required.

Justification:
These interfaces are needed for power distribution to the Hybrids, high voltage distribution to the SDDs, low voltage distribution to the SDDs, Hybrid timing/control signals, monitor signals, and a path for the Hybrid analog outputs to the Readout Electronics.
This section discusses the Carrier Interface, power distribution to the ladders (low/high voltage), timing and control, etc.
An 8 pin Cinch-Jones plug power connector will be connected to the RO chassis to bring in the $\pm$ 8 VDC power.

+8V	pin1
+8Vn	pin2
-8V	pin3
-8Vn	pin4
-	pin5
-	pin6
-	pin7
-	pin8

The low voltage power to the SVT will be supplied through a common 50 pin IDC connector using two pins for each voltage and each return (20 pins total)

+5VD	pin 1,	pin3
+5VDn	pin 2,	pin4
+5VA	pin 5,	pin 7
+5VAn	pin 6,	pin8
+6V	pin 9,	pin 11
+6Vn	pin 10,	pin 12
-6V	pin 13,	pin 15
-6Vn	pin 14,	pin 16
-2V	pin 17,	pin 19
-2Vn	pin 18,	pin 20

Chapter 27

Data Acquisition

Last Updated: 15 June 1995

Note: All DAQ information contained in this section is preliminary and must be considered by the DAQ Group and incorporated appropriately into the STAR DAQ Specifications Document.

27.1 Trigger Rates

Requirement:
The DAQ will accept triggers requesting either SVT individual readout or in combination with other STAR detectors at a rate of 100 events/sec.

Justification:
STAR requirements. This is the same as for the TPC, since the SVT will use a design compatible with the TPC DAQ. The SVT FEE and RDO can produce up to 100 events/sec due to limitations in the SCA readout rate.

27.2 Readout Rates

Requirement:
The DAQ system is required to read SVT data at Rates up to 100 events/sec, and archive at least one compressed SVT event per second.

Justification:
Stated STAR requirement.

27.3 DAQ — SVT Cable Plant

Requirement:
The physical connection between the DAQ system and the SVT detector shall not allow any ground current return paths (i.e. ground loops) between the DAQ and the SVT electronics.

Justification: Electrical noise generated by such ground currents is unacceptable.

27.4 SVT Data Delivery to DAQ

Requirement:
SVT will deliver data of neighboring anodes to the same receiver board.

Justification
Conversion of ADC data to space points requires that responces from all adjoining anodes be available to the same CPU. This is essential for recognition of boundaries of clusters formed by a single particle trajectory passing through an SVT layer.

While limited information can be passed between receiver boards, a requirement for large-scale sharing of information will result in overheads which will adversely impact system performance.

27.5 DAQ System Data Processing

Requirement:
The DAQ system will be capable of performing the following operations on the 10-bit SVT data stream:

- Subbtraction of a programmable, per channel, per time bucket offset of up to 8 bits in magnitude
- Per channel, programmable compression of each time bucket 10-bit ADC value into an 8-bit quantity
- Programmable zero suppression of time bucket data that fall outside of programmable threshold, pre, and post hit criteria

These correction will all be performed in real time with no adverse affect on the data rates referred to in the triggering requirements section.

Justification:
These operations are required for reducing the magnitude of the event data early in the acquisition cycle. These reductions are necessary to meet data archiving performance requirements later in the system.

27.6 SVT Raw Data

Requirement:
The SVT readout system produces 10-bit ADC values; early in the DAQ readout sequence these 10-bit values are converted into an 8-bit compressed value. The DAQ system will be able to produce SVT raw data events that incorporate a variety of levels of compression. That is, the DAQ system will be able to produce events with:

- 8-bit compressed data, without pedestal subtraction or zero-suppression.
- 8-bit compressed data, with pedestal subtraction, no zero-suppression.
- 8-bit compressed data, without pedestal subtraction, zero-suppressed.
- 8-bit compressed data, with pedestal subtraction and zero-suppression.
- Any of the above formats with overall $\pm 5\%$ gain correction performed by scaling of 8-bit compression conversion algorithm.

Justification:
Hardware and system debugging require access to data at varying levels of processing. Although data will ultimately be acquired in its most efficient, compressed form, experiment staging and debugging will require some or all of the above formats.

27.7 Buffering of Raw Data

Requirement:
DAQ will provide buffering for 14 events which are in the level-3 pipeline. The buffering shall be designed in such a manner to allow upgrading to 14 events in the pipeline.

Justification:
It is necessary that all detectors have buffering which results in a consistent pipeline length.

27.8 DAQ Level-3 Processing

Requirement:
DAQ will provide required pre-processing of raw detector data to generate space point summary information to be used in the level-3 CPUs, as well as the level-3 CPUs themselves. There will be sufficient processing power available at this stage to handle the preprocessing of data and transport of summary information to level-3 CPUs at a rate of 100 events/sec.

Justification:
The raw data are found in buffers on DAQ receiver boards. Massive amounts of processing are required to convert anode responses to space points to be passed to tracking code in the level-3 CPUs; this proe-processing can occur in real time only with the help from custom-built hardware in the DAQ system.

27.9 Level-3 Track Reconstruction Performance

Requirement:
Level-3 trigger decisions are based on real-time processing of the data produced by each detector, separately. For the SVT, this corresponds to track reconstruction.

There are, as yet, no detailed SVT level-3 track reconstruction algorithm performance requirements. There is, however, a known time budget for this process. The TPC/SVT receiver boards will provide sufficient buffering for up to seven events. Therefore, given the maximum SVT event rate of 100 events/sec, any average event processing that exceeds 70 msec will result in increased DAQ system dead time. Although this does not yield a requirement for the processing power needed for level-3 algorithm processing, it does provide a time budget within which system performance will not be degraded.

Justification:
Overall performance of this stage of the event selection process is critical in achieving the 100 to 1 rejection required to achieve trigger performance requirements.

27.10 Event Selection Mechanism

Requirement:
Level-3 will allow event selection before event building, based on summary information extracted from the SVT and other detectors. The mechanism of this selection process will be a series of logical flags, which are set by the level-3 CPUs for each detector separately, which will vary according to the level-3 algorithm in place. A global level-3 decision will be based on some logical combination of all flags from all detectors involved.

At level-3, this will be the only way in which information from various detectors will be combined.

DAQ will make available, on a per-event basis, histograms of distributions of any quantities on which cuts are made in Level-3; this information will be included in the assembled (accepted) events.

Justification:
Level-3 is an opportunity to select events before incurring the enormous overhead of moving large amounts of data. Well-designed algorithms to summarize the data from each detector will allow characterization of that detector. However, combining information from various detectors before event building requires a communication overhead among the detectors which will adversely affect system performance, as well as an unrealistic requirement for coordination of level-3 software among the detector systems.

Availability of histogrammed distributions of quantities on which cuts are placed is essential for determination of trigger bias.

27.11 Level-3 Software Development

Requirement:
DAQ will provide a mechanism to port and test software which has been developed in a simulation environment to the embedded environment of the level 3 CPU. A high level language will be supported.

Justification:
Conditions in the simulation environment will be quite different from that encountered in the level-3 CPU. First, it is unlikely that TAS records will be supported in level-3. Second, the level-3 CPU does not have an attached keyboard and screen for debugging. Finally, support for memory swapping may not be provided by the operating system running on the level-3 processors.

27.12 SVT Channel Pedestal Value Calibration

Requirement:
The DAQ system will perform SVT channel pedestal value calibrations at the receiver board level. It will be capable of accumulating and calculating ADC pedestal offset values for each SVT anode's time bucket and loading internal pedestal memory. The resulting pedestal values, if requested, will be sent through the normal data stream for archiving or inspection. (Time limit?)

Justification:

Pedestal calibration events are essentially black SVT events and are very large. During normal operation, there is little need to inspect or save data from individual pedestal calibration events. They are primarily used as inputs to a simple algorithm that produces individual channel offset averages that can be loaded into local pedestal memory on the receiver boards. By placing the pedestal calibration algorithm as far upstream as possible, we lessen the need to move these large black events through the system. Thus, pedestal calibration is faster, easier and, hopefully, performed more frequently.

During debugging or when individual channel sigma's appear unacceptably large, pedestal offset values (i.e. the result of the pedestal calibration algorithm) can be inserted into the data stream for recording or further analysis. The only need for uploading pedestal values would be to artificially supress the data from a single channel. As there will be other DAQ system mechanisms to accomplish this, there is no need, during normal operations, to upload pedestal memory.

27.13 SVT Anode and FEE Related Gain Calibrations

Requirement:

Gain changes of up to $\pm 5\%$ can be specified on a channel by channel basis. Specified gain corrections will be applied to all samples within a channel.

Justification:

Channel-to-channel electronic variations as well as anode effects may require adjustment of individual channel signals.

27.14 SVT Calibration Errors

Requirement:

Errors in the above SVT pedestal value calibration procedure will be reported through both the normal DAQ error logging process as well as error indication at the DAQ system control level.

Justification:

Errors, consisting of channels that will not calibrate or have excessive sigma's can indicate both FEE and/or SVT malfunctions. These conditions must be made visible to the system operator in a timely fashion.

27.15 Geographical RDO System ID Verification

Requirement:
The DAQ system will be able to probe and verify the presence and geographical ID of all RDO systems of the SVT.

Justification:
Correct DAQ system operation requires an exact understanding of the connection of the RDO systems to the SVT. An automatic probe and verifcation of the geographical location of each SVT RDO system is required to provide this information in a concise and reliable manner. This capability is essential to identify errors resulting from incorrect connection of fibers carrying the detector raw data stream.

Figure 2 shows a top level view of the TPC and SVT DAQ system and how they are connected to each other.

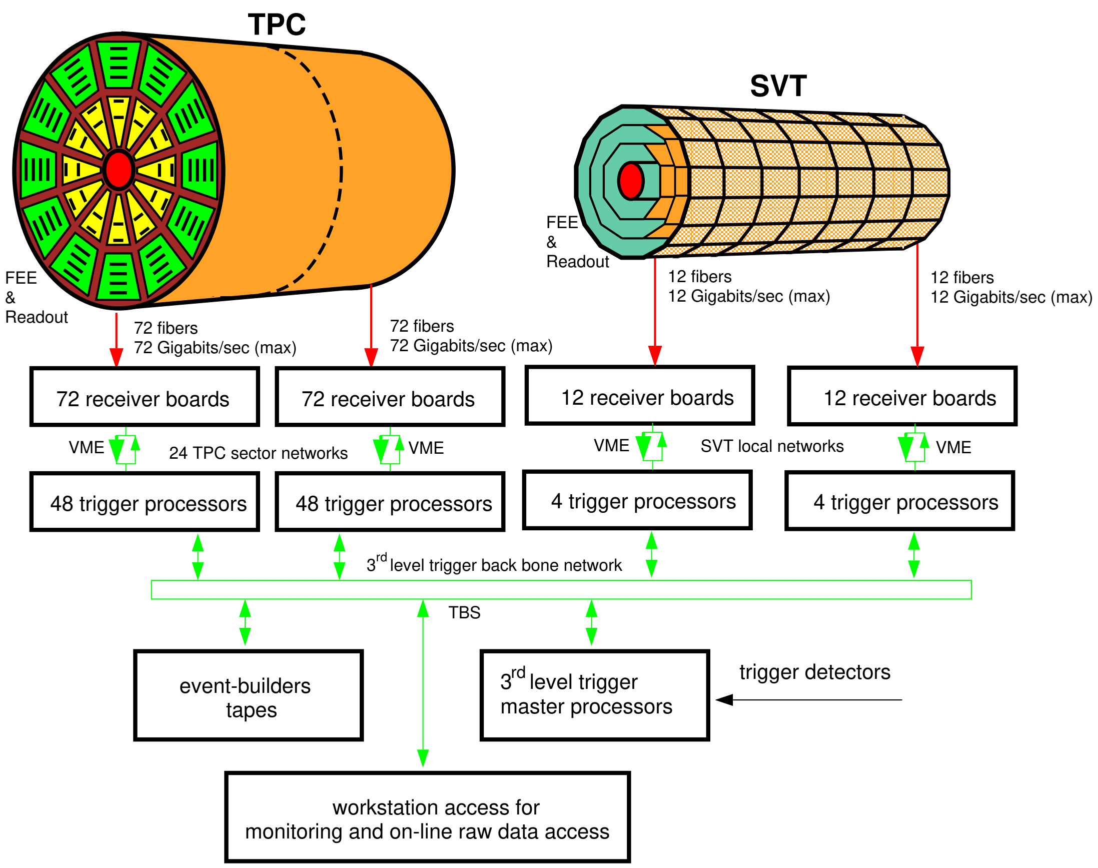

Figure 27.1: An overview of the TPC and SVT data acquisition system

The SVT DAQ system is similar in structure to the TPC DAQ system and processes the SVT data in parallel to the TPC data. The first time the TPC and SVT data are combined is at the time of the global level-3 trigger decission and at the event builder level via the level-3 backbone network. The SVT will contribute a set of logic flags to the global level-3 decission CPU, which are combined with the logic flags from the TPC and other detectors.

The whole SVT detector is divided into 8 logical sectors, which are processed in parallel in the DAQ in separate logical "sector crates". Each sector crate will contain 3 receiver boards for the 3 fibers of the readout systems in each sector, plus an undetermined number of level-3 processors (depending on the processor power needed for the SVT level-3 algorithms). Each sector crate will also contain a 68040 based "housekeeping" processor board to manage booting and configuration of the other CPU's in the crate, plus a bridge to the level-3 backbone network (this can possibly be accomplished by the housekeeping processor, if the choice of the level-3 trigger backbone network allows this).

Due to budget constraints 2 logical sector crates will be combined in one physical VME crate, sharing the housekeeping processor and network bridges. Figure 3 shows one of 4 SVT sector crates.

The level-3 processors will be off-the-shelf RISC processor boards. The choice of the specific processor will be delayed as late as possible in order to get the most processing power for the alloted budget. The only requirements on these processor boards are that they are available with the appropriate network connection (currently, the choice for the sector crate network is VME64), and that they provide the necessary software developement environment to port the level-3 algorithms to them (probably some Unix derivative or a realtime operating system). These processors will be supported by the DAQ group.

The receiver boards in the sector crates are custom built by the DAQ group and provide for the level-3 pre-processing, i.e. cluster and space point finding. Figure 4 shows the information entering and leaving the receiver card.

Each receiver card will receive data from one readout system via the HP Gigalink fiber, and provide space point summary information for all 18 detector halfs serviced by the readout systems to the level-3 CPU's. In addition each receiver card has interfaces to trigger and to the event builder(s), plus capabilities to configure it and exchange the tables needed for level-3 pre-processing. Figure 5 shows a top-level view of one of the 24 SVT receiver cards.

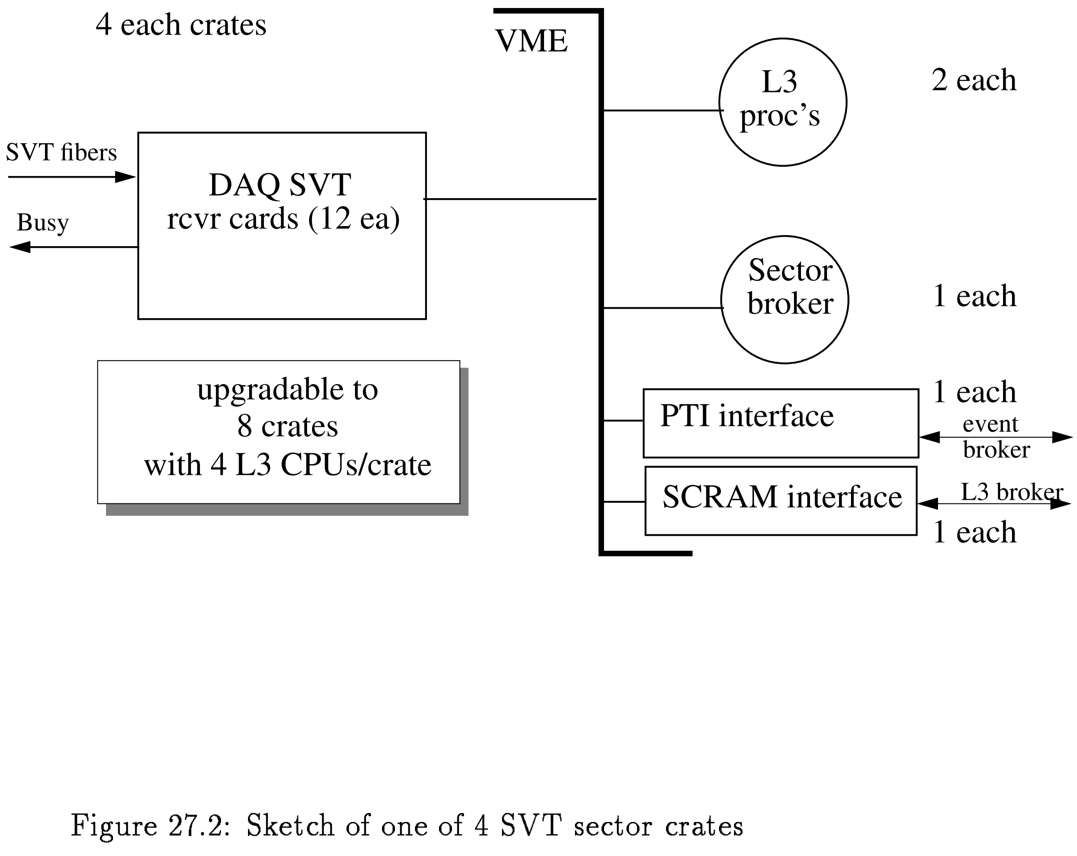

Figure 27.2: Sketch of one of 4 SVT sector crates

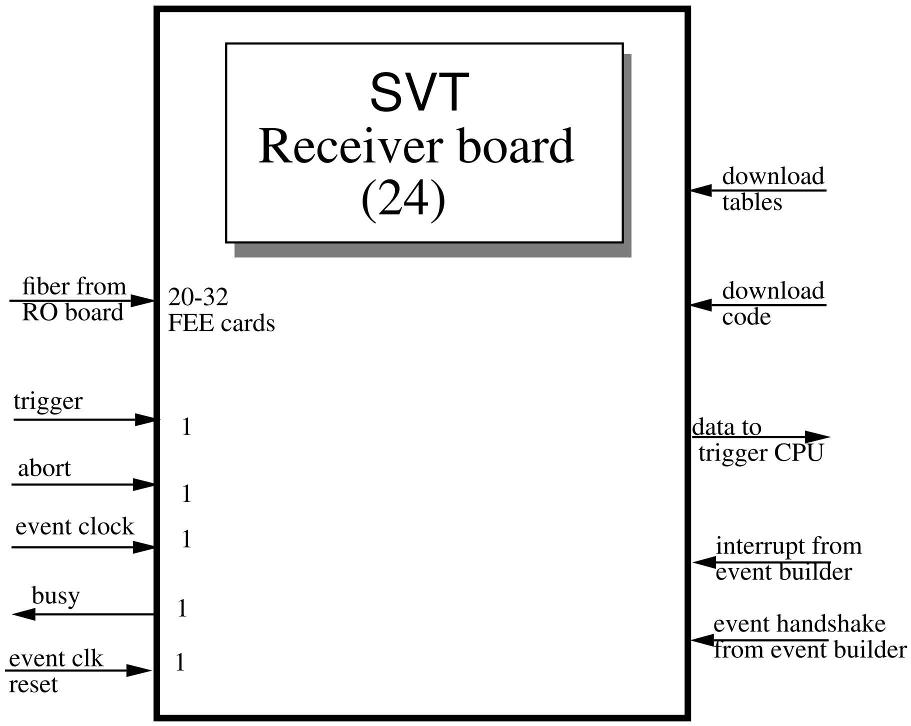

Figure 27.3: The interfaces of the receiver board

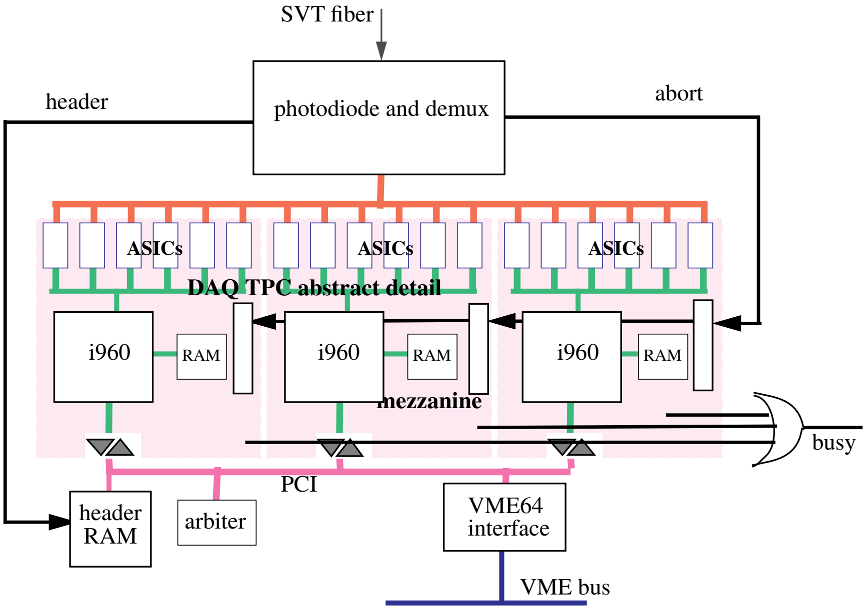

Figure 27.4: Top level of the receiver card used for TPC and SVT

Each receiver card consists of a mother board which houses 3 identical mezzanine cards. The mother board contains the Gigalink receiver logic and deserializer plus demultiplexing circuitry to distribute the raw data to the 3 mezzanine cards. The three mezzanine cards will be connected to the mother board via a global bus. Currently, this global bus is chosen to be a PCI bus with PMC style connectors. The PCI bus provides the connection to the VME64 backplane via a PCI-VME64 bridge chip. Additionally, the PCI bus will provide access to a global RAM on the mother board, which can be used to store the space point information. The hardware to accomplish the level-3 preprocessing itself is contained on the mezzanine cards.

The details of the Gigalink receiving logic on the mother board are shown in Figure 6.

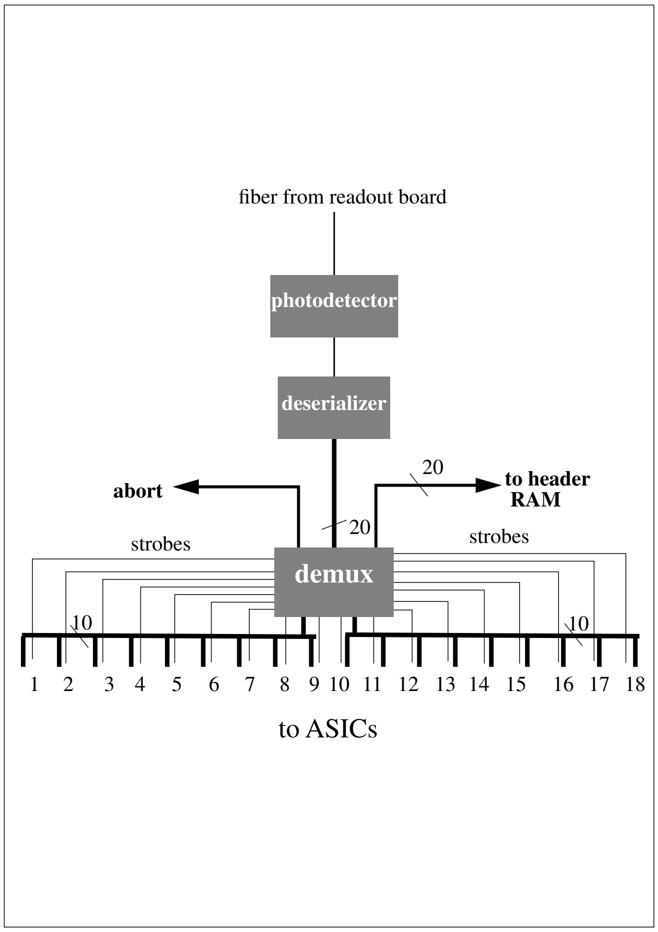

Figure 27.5: Details of the receiving logic on the receiver mother board

The Gigalink fiber from the readout system is connected to the Gigalink photodetector. The output of the photodetector is connected to the deserializer chip which provides the received data on a 20-bit bus. This 20 bit bus is split into 2 separate paths. One of these paths leads to a separate storage for the header information (possibly just a FIFO), which makes the header information available to the PCI bus for later retrieval. The other part of the bus is connected to a demultiplexing logic. The demux splits the 20-bit data words into two 10-bit data paths and strobes these 10-bit data words into 9 ASIC's for each 10-bit path. The ASIC's are addressed sequentially via the data strobes to reduce the write rate into each individual ASIC to 1/9th of the incoming Gigalink rate.

One of three mezzanine cards of a receiver board is shown in Figure 7.

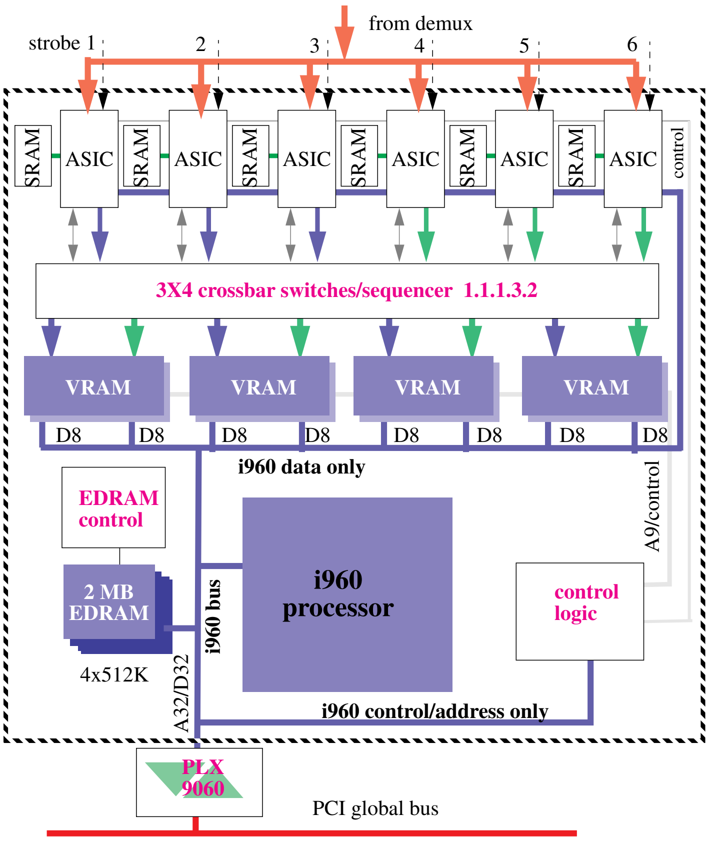

Figure 27.6: One of 3 mezzanine cards of the receiver board containing the ASIC's and the i960 for level-3 pre-processing

The mezzanine cards are the actual workhorses to accomplish the level-3 preprocessing. Each mezzanine card contains 6 ASIC's and one embedded RISC processor (currently, the choice for the RISC processor is the Intel 80960, the "i960"). The ASIC's do the first stage of the level-3 proe-processing. Each ASIC will receive the complete raw data from one detector Hybrid (1/2 of an SDD). For each 10-bit data word the ASIC will subtract an 8-bit pedestal value (stored in an external SRAM and addressed by the ASIC via the sum of the time index plus a pedestal offset delivered in the event header), and then convert the 10-bit value to an 8-bit value via an external lookup table (also stored in the external SRAM). The storage requirement for the pedestal values is: 256 anodes $\times$ 128 timebuckets = 32 kB. To store the translation lookup table we need: 256 anodes $\times$ 1024 lookup-values = 256 kB (the number 256 arises, because this lookup table also allows for anode-by-anode gain corrections by changing the lookup values for each anode appropriately). Therefore the total size of the external SRAM attached to each ASIC has to be at least 278 kB, which will require 3 external chips (128 kB each).

As the ADC data are being acquired 256 cluster pointer lists are being compiled: Each ADC value, after translation is compared with a common threshold value, THRESH_LO. Clusters are defined as sequences of consecutive timebins (for a single anode) whose translated values exceed the threshold. A qualifier, N_SEQ_LO, is used to specify that only sequences of N_SEQ_LO+1 timebins above threshold define a cluster. A second threshold, N_SEQ_HI, and associated qualifier, N_SEQ_HI, are used to further qualify the cluster before it is included in the cluster list. For this second threshold, N_SEQ_HI+1 timebins (not necessarily consecutive) must exceed THRESH_HI, during the interval in which N_SEQ_LO is being satisfied.

For sequences which meet both criteria, the beginning of a sequence t_{beg} is defined as the number of the first timebin to exceed TRESH_LO, or timebin 0 when its value exceeds the threshold value. The end of a sequence t_{end} is defined as the number of the timebin whose translated value exceeds the threshold, but the following value does not, or timebin MAX_TIMEBIN, provided its value exceeds the threshold.

The cluster RAM stores 256 lists; each list is composed of up to 8 pairs of 10-bit numbers, representing the first and last timebin in a qualifying sequence. Once the capacity of the anode (8 clusters total per anode) is reached, no further data are written to the cluster RAM for this anode.

The output of this procedure as well as the translated ADC values are stored in 8 VRAM chips via 2 3x4 crossbar switches (The number of VRAMs can be increased to allow for more events to be stored in the receiver cards). Currently, these VRAM's provide for storage of up to 7 events on the receiver cards.

The VRAM's are also connected to a bus that is accessable by the i960 on the mezzanine card. A program running in the i960 will use the information stored in the cluster-pointers and the (translated) ADC values to compile 2-dimensional clusters. It will then use a simple moment analysis to extract the centroids of these

2-dimensional clusters, a measure of the total charge of a cluster, and a measure for deciding if the cluster resulted from a single or many particles traversing the SDD. The centroid will be used as the space point for this particle crossing and will be stored in the global RAM to be passed on to the level-3 processor(s) for further processing (tracking).

The 2MB EDRAM associated with each i960 will be used to store a program and data memory for the i960. This memory will be made accessable via the VME bus to assist in bootstrapping and starting the i960 from the housekeeping processor in the sector crate.

27.16 ASIC Functional Specification

Requirement:
Application Specific Integrated Circuit (ASIC)s on DAQ Receiver Boards.

Justification:
An integrated circuit is needed on the front end of DAQ for pedestal subtraction, 10 bit to 8 bit conversion of SDD ADC data, and zero suppression.

Status:
A document entitlied **Specification for the STAR "Cluster-Finder" ASICS** (Revision E, July 3, 1995 *Baseline Copy*) by InnovASIC, Inc. gives the specifications for the ASICs to be used by both TPC and SVT.

Chapter 28

Mechanical

Last Updated: 15 June 1995

This section provides requirements for mechanical aspects of the SVT.

28.1 Support Structure

Requirement:
The support structure should be made of a low radiation length material, so that the average radiation length of the complete device (including cable, connector, cooling) does not exceed 4%.

Justification:
Multiple coulomb scattering affects position and resulution.

Status:
After thorough evaluation of the possible materials we decided to design a Beryllium structure consisting of detector carriers (DC) and adjacent electronics carriers (EC). Two EC and one DC constitute one ladder. In three barrels we have 36 ladders. An alternative to the Beryllium structure would be a Graphite-Epoxy structure. The structure would be thicker which causes problems in determining the angle of incident for tracks. The ladders are held in place by two Beryllium endcaps. The endcap radiation length is also minimized to allow useful data taking in forward rapidities (XTPC, EMC endcap, forward calorimeter).

Requirement:
The support structure has to be removable without breaking vacuum.

Justification:
If the SVT is removed, running should be possible without extended down time.

Status:
The SVT group decided to design a clamp-shell design based on the ALEPH and DELPHI experience.

Requirement:
The structure should be deflection, displacement or sag should be less than the position resolution (below 20 micron)

Justification:
Physics simulations regarding matching efficiency and particle identfication via de/dx.

Status:
Finite element analysis (FEA) of all relevant parts was performed. None of the structural parts of the SVT fails to meet the requirement.

Requirement:
The structure should also host the first stage frontend electronics (FEE).

Justification:
This allows multiplexing on the detector to ease readout and integration, and makes it easier to meet noise and power requirements.

Status:
A hybrid structure was designed and is described in the hybrid system design chapter of this document.

Requirement:
The structure should also host the carrier interface and the HV interface.

Justification:
proper signal readout

Status:
Interfaces were designed and are described in the interface system design chapter of this document.

28.2 Cooling System

Requirement:

The temperature gradient on the wafer has to be held to less than 0.3 °C.

Justification:
Physics simulations show position resolution degradation above 0.3 °C

Status:
The wafer implants were chosen to not exceed the required gradient. An air cooling system was designed to carry away on detector heat due to ambient temperature, leakage current and electronics. A water cooling system was chosen to cool the electronics to a constant operating temperature.

Requirement:
The electronics have to operate at a constant temperature near room temperature

Justification:
Uncooled electronics heats up to 80 °C in a short time interval. The performance becomes erratic at these temperatures. Very high temperatures on the EC also affect the wafer on the DC.

Status:
After thorough evaluation of three options (water, evaporative and air cooling), the group decided to design a water cooling system.

Requirement:
The cooling system has to meet the radiation length requirements

Justification:
physics simulations

Status:
The present design leads to an average radiation length of 3.2% for the completed SVT.

Requirement:
The water system has to allow a Be structure and it should be leakless.

Justification:
The Be structure is the most rigid structure with the least radiation length. The water has to be treated to avoid oxidation. An under pressure system is a standard configuration to prevent detector malfunction due to water leaks.

Status:
A leakless water system with special water purifiers and heat exchangers has been developed.

Requirement:
A water manifold system has to be integrated to the detector.

Justification:
Water manifolds ease the water supply to the distributed water cooling system.

Status:
The water is being supplied from one side of the detector and flows out to the other side. The two manifolds also host the HV divider boards for each ladder. The radiation length of the two manifolds was optimized to allow physics measurements at forward rapidities.

28.3 Assembly

Requirement:
A feasible assembly plan for the ladder assembly has to be established.

Justification:
The detector has to be bonded from all four sides on the top of ladder HV daisy chained in beam direction, signal readout perpendicular to the beam direction in both directions). In addition the HV has to be daisy chained on the bottom side of the ladder.

Status:
Assembly tools have been developed to hold and carry each ladder during and after bonding, respectively.

Requirement:
A feasible assembly plan for the complete detector has to be established A plan for transporting single ladders between assembly steps has to be established.

Justification:
The overall assembly plan has to allow local alignment of the wafers to better than the position resolution. The ladders have to be transported from their assembly stage to the detector assembly stage.

Status:

A tooling addition to a coordinate measuring machine was developed.

28.4 Installation

Requirement:
A cone structure to attach the SVT to STAR has to be developed. The cone structure has to be stiff enough to hold the detector in its aligned position throughout operation. It also has to be sufficiently rigid to carry the cable load.

Justification:
The SVT supply lines (HV, LV, water, signals) will run along the cone before distribution at the detector to keep the forward region free of material. The cable load is minimized by multiplexing on the detector. Still the cable load exceeds the detector weight by an order of magnitude.

Status:
Several graphite epoxy designs were compared. Graphite epoxy was chosen to minimize the radiation length. A solid cone was chosen to increase rigidity.

Requirement:
A light barrier to enclose the SVT has to be developed.

Justification:
The device has to be light tight.

Status:
black foam parts were chosen to enclose the structure around the air duct support

Requirement:
A support system to slide the detector into place after completion of the TPC installation has to be developed.

Justification:
The SVT will be mounted after the installment of the TPC has been finalized. That means the area of the TPC (4m along the beam) is not accessible. The SVT has to be located along the beam in the center of the TPC to an accuracy of less than 1 mm in beam direction.

Status:
A UNISTRUT system has been developed.

Requirement:
Fiducial points and adjustments have to be included in the design to allow alignment of the SVT.

Justification:
The position of the SVT has to be known to a value better than its position resolution to not degrade its performance. Because of the various stages of the installation as well as the alignment determination various gadgets have to be designed.

Status:
The detector and its assembly and installation tooling allow three different ways of adjusting the complete device throughout and after installation. Fiducial points and their location are being defined as part of the overall design.

Requirement:
A monitoring system for the SVT location has to be included in the mechanical design.

Justification:
The location and relative alignment of the detector has to be monitored during operation. Past experience with microvertex detectors has shown that displacement up to centimeters are possible (due to magnet ramping etc.)

Status:
A system comparable to the CDM system of DELPHI is being considered. This system foresees integration of capacitive probes at the end of certain selected ladders.

Requirement:
The SVT cabling plan (incl. the water and air supply) has to fit into the STAR integration plan.

Justification:
The access to the inner STAR detectors is restricted due to the design of the solenoidal magnet.

Status:
Present SVT space requirements are part of the STAR integration plan.

28.5 Alignment/Position

It is planned to align all wafers with respect to each other and with respect to the SVT support structure **before** the placement in STAR. Details of this plan were presented in the conceptual design report. The relevant part of the CDR is attached to this plan.

The present provisions in the mechanical design of the SVT are described in the following:

There are in total 36 carrier assemblies, which are designed to support detectors and FEE's. These beryllium carriers are tiled to make three concentric super layers around the beam pipe. Two pairs of precision end rings (outer and inner end rings) and standoffs assemblies are provided on both ends of the carrier assemblies to support these carrier assemblies. In-between the end rings, there are four .02 inch thick beryllium sheets (which are quadrants of a 1 inch diameter beryllium pipe) to maintain the parallelism of these two pairs of end rings. The whole assembly then will be assembled to and supported by two water manifolds through connecting elements, such as brackets, rods, and screws. The whole assembly (up to the manifolds) is a clamp shell design, which is held together by a lock mechanism. The water manifold is then mounted onto a cone support structure (made of composite material) with four sets of screws on each side. The SVT assembly will be secured onto the TPC support wheel, with one end fixed to the TPC support wheel and the other end simply supported (to eliminate the stress due to thermal expansions). The cone support structure is not separable and should be installed before the installation of beam pipe. The ends of the cone will be covered by light barriers and air duct support structures.

Requirement:
All requirements can be described by five parameters: displacements in x and z and the rotational displacements around axis perpendicular to the wafer.

Justification:
It is assumed that there are no contributions by 'bows' and 'twists' due to the stiffness of the carrier. The wafer thickness was measured to be within 5% of the avarage value (305 μm). Therefore no displacement in y has to be considered.

Status:
A coordinate system based on the BABAR coordinate system was adapted.

Requirement:
The relative uncertainty between wafers should be less than 20 μm in x and z and less than 1 mrad in all three rotational coordinates. The uncertainty is defined as the offset of all wafers with respect to the origin (middle) of the detector carrier.

Justification:
An uncertainty comparable to the intrinsic resolution of the detector leads to sufficiently small degradation in the impact parameter resolution. The assembly accuracy adds in quadrature to the position resolution.

Status:
Fiducial marks at each corner of each wafer and each end of each carrier are contained in the present design. Subsequent use of existing coordinate measuring machines (CMM) during the assembly meet the requirements. Details can be found in the mechanical design documents.

Requirement:
The gravitational sag ('bow') of each detector carrier is estimated to be less than 5 μm.

Justification:
This sag is in accordance with the maximum degradation factor of the impact parameter resolution.

Status:
Finite element analysis shows that the present setup meets the requirement. Test have to be conducted on prototypes.

Requirement:
fiducial marks have to be located at the following locations for local alignment:

- at each end of the detector carrier to locate position of carrier relative to center of barrel and to end rings.
- at each edge of a wafer to locate the wafers with respect to the detector carrier.
- on each manifold to line up the locking mechanism

Justification:
These fiducial marks are needed to meet the 20μm accuracy requirement

Status:
Fiducial marks are being provided in the wafer design and the mechanical design

Requirement:

The SVT has to be fully assembled (detector plus cone support) outside of the main detector. The accuracies specified above have to be met after the cone supports are installed.

Justification:
A unistrut is used during the assembly to lower the cost

Status:
The design and an assembly plan were drafted accordingly

Requirement:
The position of a wafer with respect to its carrier has to meet the same requirements than the stability of wafer positions with respect to each other.

Justification:
The stability of absolute wafer position enters into the position resolution in the same way than the relative wafer position.

Status:
The assembly plan based on the accuracy of the coordinate measuring machine will meet all requirements.

Requirement:
The internal survey of the assembled part has to meet the same requirements than the wafer positioning accuracy.

Justification:
The survey accuracy enters into the position resolution in the same way than the relative wafer position.

Status:
The accuracy of the coordinate measuring machine will meet the survey requirements.

28.5.1 Global Alignment Hardware Requirements

Requirement:
The placement of each wafer in the global coordinate system of STAR should have an error of less than 500 μm with respect to the global origin.

Justification:

This error allows fast tracking for trigger purposes without software correction

Status:
Under discussion

Requirement:
The lock mechanism has to allow x-y adjustments to about 500 μm with a 25μm accuracy.

Justification:
The two halfs of the SVT have to be adjusted to an accuracy of 25μm to meet the requirement that the misalignment error is on the order of the intrinsic resolution.

Status:
The present lock mechanism allows adjustments that meet the requirements

Requirement:
The position of the SVT relative to the beam pipe has to be adjustable to correct the deflection of the cone structure under stress and the position error of the manifold. The suggested y-adjustment range is about 5 mm with a 680 μm accuracy..

Justification:
The position with respect to the center of the collision has to be known to about 1 mm so that the misalignment error is on the order of the intrinsic resolution.

Status:
An y-adjustment is provided between the manifold and the cone structure.

Requirement:
The position of the SVT relative to the beam pipe has to be adjustable with respect to the collision center. The suggested z-adjustment range is about 5 mm with a 250 μm accuracy.

Justification:
The position with respect to the center of the collision has to be known to about 1 mm so that the misalignment error is on the order of the intrinsic resolution.

Status:
A z-adjustment is provided between the manifold and the cone structure. A second z-location adjustment is provided at the end of the support cone (stop) to match

the middle of the SVT detector to the collision point. The maximum range is about 3 cm.

Requirement:
After the first installation all adjustment tools have to be locked into position

Justification:
Locking the default values eases subsequent installations.

Status:
The adjustments can be locked to their accuracies after the first installation.

Requirement:
fiducial marks have to be located at the following locations for global alignment.

- several marks on each end ring to locate SVT position relative to the beam pipe (in x-y direction)
- a mark on the TPC support wheel to locate SVT position relative to the beam pipe and the TPC (in z-direction)

Justification:
These fiducial marks are required to survey the detector to the required precision

Status:
Fiducial marks are being provided in the mechanical design. Presently four (4) precision 0.062 inch diameter holes are foreseen on each endring.

Requirement:
The global alignment has to be monitored to an accuracy better or equal than the default errors (1 mm).

Justification:
Experience in past collider detector systems show that cycling the power in the magnet or temperature variations in the environment lead to sizeable position shifts in microvertex detectors.

Status:
We plan to adapt the DELPHI capacitive monitoring system for the STAR-SVT.

Requirement:

The detector axis has to be aligned parallel to the magnetic field to better than 10 mrad.

Justification:
This uncertainty meets the momentum resolution requirement without further correction

Status:
Under discussion

Requirement:
The detector x-y location has to be aligned to better than 1 mm with respect to the TPC center.

Justification:
The TPC is aligned to the magnet with a 1 mm uncertainty in the x-y location. The SVT-TPC alignment should contribute less to the accumulated error.

Status:
Under discussion

Requirement:
The detector z-location has to be aligned to better than 1 mm with respect to the most probable interaction point as determined by the VPD.

Justification:
the VPD will generate the trigger accept for the SVT based on the its determination of the interaction point.

Status:

Requirement:
The detector has to be aligned to a 5% uncertainty with respect to a default position.

Justification:
Alignment with respect to default position allows repeatibility of installation

Status:
Under discussion

Requirement:
The fiducial marks on the SVT endcap have to be visible for the survey without major rearrangements of the STAR detector

Justification:
It is anticipated that the SVT will be removed from the main detector for maintenance purposes. The requirement ensures fast and easy relocation.

Status:

Requirement:
The survey tools have to be on axis with the SVT reference points

Justification:
Allows repositioning of SVT without remapping of the exact location.

Status:

Requirement:
All SVT reference points have to be accessible to the surveyers.

Justification:
Allows removal and repositioning of SVT into STAR.

Status:

Requirement:
The exact locations of reference points on the main detector and the floor have to be determined by the SVT group and the STAR integration group before the main detector is positioned in the experimental hall

Justification:
The feasibility of the positioning of the SVT to its specifications has to be simulated, based on accessibility of fiducial marks, before the main detector is in place.

Status:

Chapter 29

Integration

This section provides requirements associated with integration the SVT into STAR.

29.1 Space

Last Updated: 16 February 1995

The space requirements for integrating the SVT subsystem are detailed in this section. NOT discussed is the space required for the 24 READOUT ELECTRONICS locations and the space required for the SVT and its physical support structure.

Space is required for the following SVT subsystem interconnections:

- Electrical CABLES from the SVT RACKS to the SVT READOUT ELECTRONICS or passed through the READOUT ELECTRONICS to the SVT CARRIERS OR CARRIER INTERFACES
- Electrical CABLES from the SVT READOUT ELECTRONICS to the SVT CARRIER INTERFACES
- OPTICAL FIBERS from the SVT READOUT ELECTRONICS to the COUNTING HOUSE (DATA ACQUISITION)
- WATER LINES to the SVT WATER MANIFOLDS
- AIR DUCTS to the SVT LIGHT PLATES
- RACK space for power supplies, TRIGGER distribution electronics, CALIBRATION electronics, SLOW CONTROLS, WATER system, etc.
- OTHER space needs

For the discussion in this section: the RACKS location is on the NORTH PLATFORM, SECOND LEVEL; the READOUT ELECTRONICS locations are on the TPC endcaps near the ends of the SVT SUPPORT CONES; the CARRIERS and CARRIER INTERFACES are located near each end of the SVT; and CABLE refers to either a single conductor cable or a multiconductor cable.

29.1.1 Executive Summary

Tables 1-6 summarize electrical CABLE requirements, optical FIBER requirements, WATER line requirements, AIR DUCT requirements, RACK requirements, and OTHER space requirements for the SVT. These requirements are justified below. In estimating the cross sectional area of cable paths required, cables were treated as having **square** cross sections of area $A = diameter^2$.

For **each** RACKS to **individual** READOUT ELECTRONICS location (i.e., 24 **separate** paths, 12 to **each** end of the TPC) the integrated cross sectional area of the required CABLES (11 CABLES) is 3 in^2.

All CABLES entering **each** end of the SVT SUPPORT STRUCTURE (360 CABLES) have an integrated cross sectional area of 35 in^2. WATER lines require an additional 6 in^2 of space in **each** end, so at least 41 in^2 is required through **each** end of the SVT SUPPORT STRUCTURE. The cross sectional area of a 1 in wide ring with an outer radius of 7.8 in (the radius at the small end of the "CONE") is 46 in^2.

Two OPTICAL FIBERS from **each** of the 24 READOUT ELECTRONICS locations go directly to DATA ACQUISITION in the COUNTING HOUSE. Sharp turns must be avoided and **each** of the 24 paths requires a cross sectional area of 0.1 in^2.

Two WATER lines (1.5 in, inside diameter, each) must connect the supply side of the SVT HEAT EXCHANGER (located outside the experimental hall) to two WATER MANIFOLDS near one end of the SVT SUPPORT STRUCTURE; from each MANIFOLD 5 – (0.75 in, outside diameter, **each**) WATER lines enter the SUPPORT STRUCTURE (10, total) and go to another WATER MANIFOLD near the SVT. An identical requirement exists at the other end of the SVT in order to return the water to the HEAT EXCHANGER (via a low pressure water system located on the NORTH PLATFORM, THIRD LEVEL). This water cooling system must be independent from any other cooling system. SPACE is required for the mechanical part of this system.

Large AIR DUCTS must be located at **each** end of the SVT SUPPORT STRUCTURE for SDD surface cooling. These DUCTS connect to the SVT LIGHT

PLATES which make the SVT light tight. The SVT AIR CONDITIONING system must be independent from any other air conditioning system. SPACE is required for the MECHANICAL part of this system.

NOTE: A multi-conductor (number of conductors to be determined) must run from the RACKS to the Capacitive Displacement Measuring System (CDMS) located on the SVT ladders.

NOTE: In addition, WATER must be provided to **each** of the 24 READOUT ELECTRONICS locations for electronics cooling. The TPC WATER system which cools the TPC READOUT ELECTRONICS will provide the SVT READOUT ELECTRONICS cooling WATER. **Each** (24 total) READOUT ELECTRONICS area will generate about 100 Watts of power.

29.1.2 Electrical Cables from the SVT Racks to the SVT Readout Electronics or passed through the Readout Electonics to the SVT Carriers or Carrier Interfaces

Requirement:
The required CABLES to **each** of the 24 READOUT ELECTRONICS locations are listed in Table I. The total number of CABLES required is 24 times the numbers in Table I. The cross sectional area of the bundle of CABLES that runs from the RACKS to **each** of the 24 READOUT ELECTRONICS LOCATIONS (11 CABLES) is 3.0 in^2.

Function	Conductors	Diameter (inches)	Number
HIGH VOLTAGE	1 Coaxial	0.25	3
CALIBRATION	6 shielded pair	0.5	3
LOW VOLTAGE	4 conductor	0.75	2
TRIGGER Distribution	8 shielded pair	0.5	1
SC (HDLC) LINK	4 shielded pair	0.5	1
SPARE	8 shielded pair	0.5	1

Table I: CABLES required from SVT RACKS to **each** READOUT ELECTRONICS locations or passed through READOUT ELECTRONICS to CARRIERS OR CARRIER INTERFACES. There are 24 READOUT ELECTRONICS locations on the TPC end caps. 12 are on right side and 12 are on the left side. The HIGH VOLTAGE CABLES pass through the READOUT ELECTRONICS locations, through the SVT SUPPORT STRUCTURE, to HIGH VOLTAGE DIVIDER BOARDS near the ends of the SVT LADDERS. The CALIBRATION CABLES pass through the READOUT ELECTRONICS locations, through the SVT SUPPORT STRUCTURE, to the CARRIER INTERFACES. All CABLES are plenum rated.

Justification:
THE SVT LOW VOLTAGE power supplies, HIGH VOLTAGE power supplies, TRIGGER/CLOCK distribution point, SDD CALIBRATION-source electronics, and the SLOW CONTROLS system are located in the RACKS. Electrical CABLES must connect these systems to the SVT READOUT ELECTRONICS, the CARRIERS, and the CARRIER INTERFACES.

The SVT contains 36 ladders. Near the water manifolds close to both ends of each ladder are voltage DIVIDER BOARDS. A separate HIGH VOLTAGE line connects to each DIVIDER BOARD, so that a total of 72 HIGH VOLTAGE lines is needed. Since there are 24 READOUT ELECTRONICS locations at each TPC endcap, 3 HIGH VOLTAGE lines from the RACKS through **each** of the 24 READOUT ELECTRONICS locations are required. The HIGH VOLTAGE lines pass through the READOUT ELECTRONICS locations, through the SVT SUPPORT STRUCTURE, to DIVIDER BOARDS located near the ends of the SVT LADDERS.

[From each DIVIDER BOARD a flex cable with 50 voltage levels runs to the first detector on its side of the ladder. Each detector has about 500 cathodes, and each 10th cathode is supported externally. The voltage lines are then *daisy chained* to the other detectors on the ladder. The actual number of Silicon Drift Detectors associated with each of the 72 HIGH VOLTAGE lines is 2, 3, or 4. The number of 50-line HIGH VOLTAGE distribution cables from the water manifolds to the ladder is 72.]

Each SDD requires 6 CALIBRATION signals. A total of 72 – (6 shielded pair) CABLES are required. **Each** cable goes to one end of **each** ladder and the 6 CALIBRATION signals are *daisy chained* to either 2, 3, or 4 SDDs on that end of the ladder. Since there are 24 READOUT ELECTRONICS locations (12 on **each** TPC endcap), 3 CALIBRATION signal lines are routed from the RACKS through **each** of the 24 READOUT ELECTRONICS locations, through the SVT SUPPORT STRUCTURE, to the CARRIER INTERFACES.

Each READOUT ELECTRONICS location requires LOW VOLTAGE power for POWER CONDITIONERS that generate -1,+4, +5A, +5D, +12, -12 VDC for use by the READOUT ELECTRONICS and the HYBRIDS. These 6 voltages will be provided to **each** READOUT ELECTRONICS location using 2 – (4-conductor) cables from power supplies in the RACKS. [The additional 2 conductors are for 2 grounds (A&D).]

Each READOUT ELECTRONICS location requires 1-(4 shielded pair) from the CLOCK/TRIGGER distribution tree.

Each READOUT ELECTRONICS location requires 1-(4 shielded pair) to interface the READOUT ELECTRONICS to the SLOW CONTROLS (HDLC).

In addition 1–(8 shielded pair) should be provided to **each** READOUT ELECTRONICS location for SPARE, SAFETY, INTERLOCK, ETC., purposes.

NOTE: A multi-conductor (number of conductors to be determined) must connect **one** of the RACKS to the Capacitive Displacement Measuring System (CDMS) located on the SVT ladders.

29.1.3 Electrical Cables from the SVT Readout Electronics to the SVT Carrier Interfaces

Requirement:
The required CABLES from **each** READOUT ELECTRONICS location to to the SVT CARRIERS or CARRIER INTERFACES are listed in Table II. The cross sectional area of the bundle of CABLES (360 CABLES) (from 12 READOUT ELECTRONICS locations) that enters **each** end of the SUPPORT STRUCTURE is 35 in^2 (including 36 HIGH VOLTAGE and 36 CALIBRATION CABLES, Table I).

Function	Conductors	Diameter (inches)	Number
LOW VOLTAGE	8 conductors	0.4	6
TIMING/CONTROL	8 shielded pair	0.25	6
MULTIPLEXED ANALOG	4 shielded pair	0.25	6
CARRIER ID, MONITORS	10 conductor	0.2	6

Table II: CABLES required from **each** SVT READOUT ELECTRONICS location to SVT CARRIERS or SVT CARRIER INTERFACES. There are 12 READOUT ELECTRONICS locations on **each** of the two TPC endcaps. The total number of CABLES entering the SVT SUPPORT STRUCTURE from **each** end is therefore **12 times** the numbers in this table **plus** 36 HIGH VOLTAGE and 36 CALIBRATION CABLES passed through the READOUT ELECTRONICS locations. All CABLES are plenum rated.

Justification:
The SVT has 142 CARRIER INTERFACES. **Each** READOUT ELECTRONICS must connect with 6 CARRIER INTERFACES. **Each** CARRIER INTERFACE requires LOW VOLTAGE (8 conductor, same as required for READOUT ELECTRONICS), TIMING/CONTROL (8 shielded pair), MULTIPLEXED ANALOG lines (4 shielded pair), and CARRIER ID, MONITORS lines (10 conductor).

The total number of CABLES required for **each** side of the SVT is 12 times the numbers in Table II, **plus** 36 HIGH VOLTAGE and 36 CALIBRATION CABLES listed in Table I.

29.1.4 Optical Fibers from the SVT Readout Electronics to the Counting House (Data Acquisition

Requirement:
Table III shows the OPTICAL FIBERS, per **each** READOUT ELECTRONICS location, that connect the READOUT ELECTRONICS to DATA ACQUISITION RECEIVERS in the COUNTING HOUSE. A path with a square cross sectional area of 0.1 in^2 is required from **each** READOUT ELECTRONICS location to DAQ. Sharp bends must be avoided.

Function	Diameter (inches)	Number
FIBER LINK	0.2	2

Table III: OPTICAL FIBERS required from **each** SVT READOUT ELECTRONICS location to DATA ACQUISITION (COUNTING HOUSE) RECEIVER ELECTRONICS. There are 12 READOUT ELECTRONICS locations on **each** of the two TPC endcaps. The total number of OPTICAL FIBER CABLES arriving at DAQ is 48.

Justification:
The READOUT ELECTRONICS interface to the DATA ACQUISITION RECEIVER ELECTRONICS via OPTICAL FIBER links. **Each** READOUT ELECTRONICS requires a dual fiber link to DAQ; a total of 48 OPTICAL FIBERS are required.

29.1.5 WATER LINES to the SVT WATER MANIFOLDS

Requirement:
Table IV gives WATER line requirements at **each** end of the SVT for SDD/HYBRID cooling. The SVT must have its own water cooling system.

Function	Diameter (inches)	Number
HEAT EXCHANGER to STAR	1.5 (inside)	2
STAR to WATER MANIFOLD	0.75 (outside)	10

Table IV: WATER requirements at **each** end of SVT for cooling.

Justification:
The SVT Silicon Drift Detectors (SDDs) and CARRIER ELECTRONICS must be maintained at a constant temperature. Cooling WATER will be provided by a dedicated water system. Two 1.5 *in* (inside diameter) WATER lines must go from the HEAT EXCHANGER of a HIGH PRESSURE water system located OUTSIDE the experimental hall to 2 WATER MANIFOLDS (about 4 $in \times 4\ in \times 4\ in$, each) located near one TPC endcap region. Each MANIFOLD connects to 5 – 0.75 *in* (outside diameter) WATER lines for entry into the SUPPORT STRUCTURE. These 10 lines connect to a WATER MANIFOLD near the SVT CARRIER INTERFACES. On the other side of the SVT SUPPORT STRUCTURE an identical arrangement **returns** the water THROUGH a LOW PRESSURE water system (located in the experimental area on the NORTH PLATFORM, THIRD LEVEL) to the HEAT EXCHANGER located outside the experimental hall. The TPC water cooling system is inadequate for use by the SVT for SDD/HYBRID cooling.

NOTE: In addition, WATER must be provided to **each** of the 24 READOUT ELECTRONICS locations for electronics cooling. The TPC WATER system which cools the TPC READOUT ELECTRONICS will provide the SVT READOUT ELECTRONICS cooling WATER. **Each** READOUT ELECTRONICS area will generate about 100 Watts of power.

29.1.6 Air Ducts to the SVT Light Plates

Requirement:
AIR DUCT requirements at **each** end of the SVT SUPPORT STRUCTURE are given in Table V. These DUCTS attach to the SVT LIGHT PLATES at **each** end of the SVT SUPPORT STRUCTURE. The SVT must have its own AIR CONDITIONING system.

Function	Diameter (inches)	Number
AIR FLOW to SVT	TBD	4

Table V: AIR DUCTS required at **each** end of SVT SUPPORT STRUCTURE

Justification:
AIR flow through the SVT is required to provide surface cooling of the Silicon Drift Detectors. The STAR AIR CONDITIONING is inadequate for SVT use.

29.1.7 Rack Space for Power Supplies, Trigger distribution, Calibration distribution, Hardware Controls, Water System, etc.

Requirement:
RACK space requirements are given in Table VI. A total of 8 RACKS is required. The RACKS are located on the NORTH PLATFORM, SECOND LEVEL. The RACKS are assumed to be standard width (19 *inch*) and height (about 6 *feet*).

Function	Number
HIGH VOLTAGE Power Supplies	1
LOW VOLTAGE Power Supplies	3
Slow Controls	2
TRIGGER Distribution, CALIBRATION	1
WATER, Misc.	1

Table VI: RACK space required for SVT.

Justification:
The SVT uses HIGH VOLTAGE power supplies, LOW VOLTAGE power supplies, WATER cooling, AIR cooling, READOUT ELECTRONICS, CALIBRATION electronics, TRIGGER distribution electronics, SLOW CONTROLS electronics, and DATA ACQUISITION electronics.

29.1.8 OTHER space needs

Requirement:
The SVT HIGH PRESSURE water system requires a floor space of 5 $ft \times 5$ ft outside the experimental hall. The SVT LOW PRESSURE water system requires a floor space of 3 $ft \times 3$ ft on the NORTH PLATFORM, THIRD LEVEL. The SVT AIR CONDITIONING system requires a floor space of 2 $ft \times 5$ ft and its location remains to be determined.

Justification:
The WATER cooling system and the AIR conditioning systems require space.

29.2 SVT–Water and Air Systems

Last Updated: 15 June 1995

This section contains information concerning water and air system requirements.

Requirement:
Short statement of requirement.

Justification:
Justification of the requirement.

29.3 SVT–TPC Integration

Last Updated: 15 June 1995

Requirement:
The space between the point of highest voltage on the TPC-IFC and the outermost layer of the SVT structure has to be at least 25 cm.

Justification:
We assume a maximum voltage of 85,000 Volts on the detector. The reduction of the voltage through the gas gap filled with atmospheric air is set to be 4,000 V/cm. By setting the maximum voltage to 100 kV we allow a slight margin for risk reduction.

Status:
Presently the distance between the graphite epoxy tubes connecting the two cone halfs and the IFC of the TPC is slightly more than 32 cm. Even by taking into account the suggested resistor chain at the TPC, the distance will reduce only to about 29 cm.

Requirement:
The air cooling for the SVT has to run at atmospheric pressure and should not exceed a pressure of 4 mb.

Justification:
Higher pressure might lead to implosion of the TPC-IFC

Status:
We are trying to combine the air cooling of the SVT with the air stream through the TPC gas gap.

Requirement:

The surface of the SVT structure towards the TPC should not have any sharp edges.

Justification:
Sharp edges might lead to HV sparks.

Status:
We consider a conductive layer of aluminized mylar on top of the cable routing and the graphite epoxy tubes of the SVT structure.