The CDF Silicon Vertex Tracker

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The Silicon Vertex Tracker (SVT) is presently being built as part of CDF upgrades. It is the online tracker which will reconstruct 2D tracks using information from the Silicon Vertex Detector (SVXII) and the Central Outer Chamber (COT). The precision measurement of the track impact parameter will allow to select high statistics b samples at trigger level and attack the study of CP violation in the b sector (i.e. in the $B_d^0 \rightarrow \pi^+\pi^-$ decay) and of B_s^0 mixing. We discuss the overall architecture, algorithms and hardware implementation of the system.

1. Introduction

The Tevatron $p\overline{p}$ Collider and the CDF detector are presently being upgraded for Run II operation (to begin in the year 2000). The Tevatron center-of-mass energy will be increased from 1.8 TeV to 2.0 TeV and the instantaneous luminosity by almost one order of magnitude, to reach 1-2$\times10^{32}$ cm^{-2} sec^{-2}, with the goal to take 2 fb^{-1} of data [1]. The bunch spacing will be reduced from 3.7 μs to 132 ns.

To cope with the higher rate of interaction, all the Data Acquisition will be fully replaced with faster devices.

The SVT will work in the level 2 of CDF trigger chain and will refine the level 1 track processor (XFT) information, which uses data from the central drift chamber COT, by combining it with the Silicon Vertex Detector (SVXII) hits[2]. Since the SVT has to complete track reconstruction within 10 μsec, the design of the device has exploited parallelization of the various tasks (reconstruction of the hit coordinates from the strip pulse heights, pattern recognition and final precision track fitting).

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The SVT is built on 9U Eurocard boards which implement VMEbus interface for diagnostic and control. The architecture is data driven and many functions overlap in the internal processor pipeline. Specification require 30 MHz operation for each module with an asinchronous data transfer rate of 630 Mbit/s on custom data paths.

2. SVT tracking strategy and architecture

The SVT receives sparsified and digitized pulse heights from the SVXII front end electronics via optical G-links. The Hit Finder board sincronizes data coming from the G-links, subtracts pedestals and suppresses hot channels. Cluster centroids are found calculating the charge center of gravity. Hits from the Hit Finder and COT tracks from the XFT are sent simultaneously to the Associative Memory board and the Hit Buffer.

The Associative Memory matches COT track candidates (about 3 per event on average) to SVXII hits performing a first pattern recognition with a limited spatial resolution[3]; for this pur-

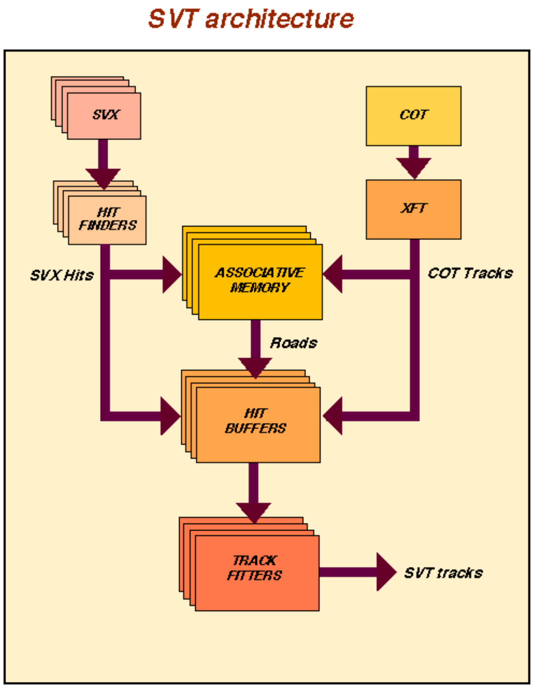

Figure 1. The Silicon Vertex Tracker architecture.

pose the SVXII is segmented into 250 μm wide superstrips. Three low-resolution tracks (roads) per event are found on average by the Associative Memory and sent to the Hit Buffer, where each road is associated to the list of full resolution hits ($\sim$15 μm) which have generated it [4]. The road-info packet (road+hits) is sent to the Track Fitters which perform a full resolution fit using a fast linearized algorithm implemented in hardware. The output of the Track Fitters is the list of track parameters (p_t, ϕ and impact parameter) measured with offline quality resolution: $\sigma_{p_t} = 0.003 \cdot p_t^2$, $\sigma_\phi = 1$ mrad and $\sigma_d = 35$ μm (at $p_t = 2$ GeV/c). SVT tracks are sent to the CDF level 2 processors for trigger decision.

2.1. System Topology

The SVXII detector is divided into 6 barrels along the z direction and each barrel in 12 wedges (sectors), each covering 30 degrees in azimuthal angle. Each of the 72 wedges is read independently and feeds one Hit Finder. All the hits from the 6 wedges at the same ϕ and the XFT tracks found in the same region are sent to the same Associative Memory bank and Hit Buffer. So the SVT has in total 12 AM banks and 12 HB. Each HB sends road-info packets to one Track Fitter and the complete Track List from the 12 Track Fitters is used to build different level 2 physics triggers.

2.2. Communication protocol

Data flow through the SVT with a uniform protocol. The system is data-driven, there is no handshake other than the data flow: each block starts to process data as soon as it receives them and outputs results as soon as they are ready. Data flow through unidirectional differential lines on a flat cable using a simple transfer driven by an asynchronous clock as communication protocol. At every clock cycle data are pushed into a FIFO on the receiving end. The "Almost Full" signal issued by the FIFO is interpreted by the source as a "Hold" and provides a loose handshake. The source responds to the Hold signal by suspending the data flow, that is resumed as soon as the Hold goes out.

On the cable there are 21 data bits, a Clock, a Hold, End Packet (EP) and End Event (EE) signals. The EP bit marks the last word of a packet, the EE bit marks the end of data corresponding to one event. Each module sends out the EE word after it has received an EE word on all its inputs.

3. Associative Memory system

The Associative Memory system is made of one control board (the Associative Memory Sequencer) and two Associative Memory boards. The AM system has the function of performing pattern recognition, that is to select for further processing only hit combinations representing good track candidates. This part of SVT data processing is the most computationally-intensive and is performed by comparing input data with a stored set of patterns in a completely parallel way, using a dedicated custom VLSI chip[5]. In this way pattern recognition is carried "on-the-fly" during detector readout and the results are available shortly after the end of the input phase.

The Sequencer board is the interface between the Associative Memory system and the rest of the SVT and provides the proper opcode sequences to the Associative Memory boards through a custom P3 backplane. The AM board has two operating modes. "VME mode" is used to load patterns into the associative memory at power-up and for diagnostics; the board operates on an internal (slow) clock and ignores signals coming from the P3 backplane. In "running mode" the board is controlled by the AM Sequencer through the P3 bus and runs with the fast clock distributed on the backplane by the AM Sequencer.

The AM board holds 128 AMchips and in running mode the board distributes the opcodes and the data received on P3 to all AMchips and queues data output by all chips to the P3 bus. To this purpose two tree-like structures have been created, one for input and one for output, with 128 AMchips at the bottom level[6].

4. Hit Buffer

The Hit Buffer receives data from two input streams, the Hit stream and the Road stream and sends output data on the road-info stream. Within the Hit buffer, hits are stored in a structured data base built on the fly (Hit List memory), so that each road number can then be used as a key to access lists of hits. Incoming hits are sorted into a number of classes, called Super Strips, according to their value ranges. There is one Hit List for each Super Strip and all these lists are filled as the hits are received in input.

Hit Buffer operation is in two different phases: the "Write Mode" and the "Read Mode". In "Write Mode" the hits received in input are organised in the Hit List Memory, depending on the Super Strip they belong to. Roads are defined as the combination of Super Strips, one Super Strip per layer. In "Read Mode" each Road received by the Hit Buffer requires that the associated Hit Lists are sent from the Hit List memory on the output stream.

The Hit Buffer sends the first output data at the first clock cycle following road reception, one word (hit) per clock cycle. A very fast access to the Hit List Memory is provided by large look-up-tables, where pointers into the Hit List Memory are stored. The "Super Strip Map" contains the starting address of the Hit List where each hit must be written when it arrives, while the "Associative Memory Map" provides the starting addresses of the Hit Lists to be sent on output for each road. All the hits retrieved in this way and the road number make the road-info packet, with the road number being the last word of the packet. Basically the two maps contain the same information, but they implement different data base structures with different addressing schemes.

5. Track Fitter

The main function of the Track Fitter is the calculation of the track parameters (d, ϕ, p_t) and the track χ^2. This is done using the full resolution measurement of the SVXII hits and of the track curvature and azimuthal angle by the XFT. Track parameters are calculated with a linear approximation:

$$p_i = \vec{f_i} \cdot \vec{x} + q_i \tag{1}$$

where p_i is one of the track parameters and $\vec{x}$ is the array containing hit positions and track curvature and azimuthal angle. The parameters $\vec{f_i}$ and q_i are constant within one wedge.

With the current technology, the calculation of eq. (1) is too overloaded when the full resolution measurement of the SVXII hits and XFT track parameters is restored. To reduce the load of calculation, the following algorithm is used:

$$p_i = \vec{f_i} \cdot (\vec{x}_0 + \vec{d}) + q_i \tag{2}$$

$$p_{0i} + \delta p_i = (\vec{f_i} \cdot \vec{x_0} + q_i) + \vec{f_i} \cdot \vec{d} \tag{3}$$

where $p_{0i} = \vec{f_i} \cdot \vec{x}_o + q_i$ and $\delta p_i = \vec{f_i} \cdot \vec{d}$. In eq. (3) the p_{0i} is the value of the track parameter with the hits at the lower edge ($\vec{x}_0$) of the Super Strips in the road. The value of the p_{0i} is precalculated and stored in a look-up-table. The Track Fitter then has to calculate the δp_i and add the value of the p_{0i} from the look-up-table. Since the $\vec{d}$ varies within the Super Strip edges (~250 μm wide), a lower number of bits is necessary to have the full hit resolution. The calculation is performed with currently available FPGA (Altera Flex10K).

6. SVT Timing

Timing performances have been estimated under the assumption that each board in the system will be able to operate at a 30 MHz rate and using the transit delay (input connector to output connector) measured on the real boards. A bit-level simulation of the SVT has been used to reconstruct both real CDF data and simulated b-jets events. Real data are from CDF run I and thus correspond to run I detector geometry, while MonteCarlo data use run II geometry. Estimated overall processing time is respectively 11 μsec and 9 μsec for b-jet events generated at $p_t > 20$ GeV/c and $p_t > 10$ GeV/c, while for real data with a low expected content of b-jets, time is $\sim$6 μsec.

7. Error handling

There is a number of error conditions that can be detected by SVT while processing data, for example something can go wrong in the data transfer and the input FiFo on one board can become full, or some of the data received in input by one board are outside the valid range. The system can set error flags in the VME register of the single board or propagate error flags in the data stream setting appropriate bits on the End Event word. The SVT is also equipped with a powerful tool for diagnostics, the Spy Buffers, where data flowing through each input and output stream of each board are continuosly copied. The Spy Buffers act as built in logic state analyzers hooked to internal SVT data streams and help system monitoring and diagnosis. As a consequence of error conditions the Spy Buffers can be frozen and read through the VME interface without causing any interference to the data flow. The freezing of the Spy Buffers is coordinated by the Spy Control boards.

8. Tracking performance and Physics prospects

Tracking performance has been tested reconstructing real CDF data using the SVT simulation. This has been possible because run I Silicon Vertex Detector (SVX) and Central Tracking Chamber (CTC) had a similar geometry to run II detectors. It has been proved that SVT tracks are very close to offline tracks and the SVT efficiency is close to 97 % of tracks with 4 reconstructed hits in SVX. Resolution on track parameters is in the expected range.

8.1. All hadronic B decay trigger

The measurement of impact parameters at trigger level allows the design of physics triggers to select events with secondary vertices, like B hadrons decay. We have studied a trigger to select all hadronic B decays, such as $B_d^0 \to \pi^+\pi^-$ [7], which is of fundamental importance in the study of CP violation in the Standard Model. The use of this trigger has then been extended to similar decay channels like $B_s^0 \to D_s^-\pi^+$, $B_s^0 \to D_s^-\pi^+\pi^-\pi^+$ with the D_s^- fully reconstructed through hadronic decays ($D_s^- \to \phi\pi^-$ and $D_s^- \to K^{*0}K^-$), which would allow to attack the problem of B_s mixing [8]. Further studies have shown a similar trigger to be effective also in the selection of a sample of $Z^0 \to b\bar{b}$ decays [9].

The trigger strategy is to select two stiff ($p_t > 2$ GeV/c) opposite charge XFT tracks at level 1, requiring some separation in the azimuthal angle ($\delta\phi < 135$) in order to remove back-to-back pairs produced in dijets events. At level 2 the trigger requires two SVT tracks with impact parameter > 100 μm and a positive decay length of the two track vertex. Trigger simulation shows that trigger rates are well within DAQ bandwidth with expected signal yields of the order of 15,000 for the $B_d^0 \to \pi\pi$ decay and 25,000 for the B_s^0 decays in 2 fb^{-1} of integrated luminosity. With preliminary estimates for backgrounds, the expectation is to reach a sensitivity of $\sim$0.15 on the CP asimmetry and $\sim$60 [8] on the x_s mixing parameter.

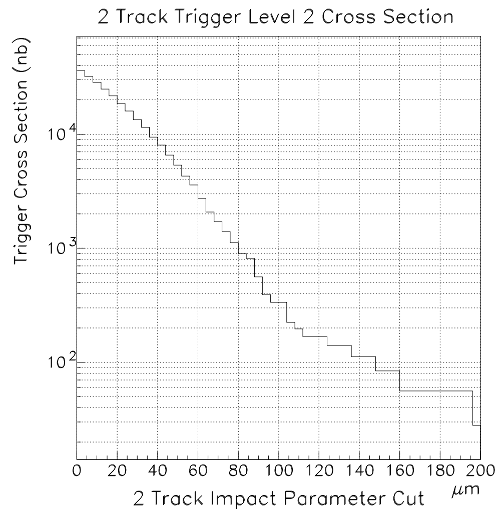

Figure 2. Level 2 cross section of the all hadronic B decay trigger as a function of the impact parameter cut applied on both tracks. The plot is obtained applying trigger cuts on a sample of real CDF run I data reconstructed with the SVT simulation.

9. Conclusion

The design and the status of the CDF Silicon Vertex Tracker have been reviewed. Construction and tests of most component boards are about to be completed and production is close to start. The expectation is to have the system ready in time for CDF run II data taking in the year 2000.

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