Fabrication of prototype imaging arrays for SCUBA-2 ⋆

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Abstract

Prototype imaging subarrays for SCUBA-2 (the Submillimeter Common-User Bolometer Array) have been fabricated and tested. The pixel count (1280) of these wafer-scale imagers is significantly larger than any other low-temperature detectors produced to date, and represents a major step forward for the low-temperature detector community. These transition-edge-sensor (TES) based imagers utilize several innovations including in-focal-plane superconducting quantum intereference device (SQUID) multiplexers, micromachined Si block absorbers, and superconducting wafer hybridization. In this paper, we review the fabrication processes developed for these imagers and present recent optical data from a prototype imaging subarray.

Key words: Transition edge sensor, SQUID multiplexer, Imaging array
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1. Introduction

The convergence of detectors utilizing TESs, SQUID multiplexers, Si micromachining, and indium wafer hybridization (bump-bonding) has enabled the development of a new generation of large-area imaging detectors for use in submillimeter band imaging. These new detectors are planned as replacements for current state-of-the-art detectors such as SCUBA [1]. Here we present an overview of the fabrication processes developed for these imagers and briefly discuss results on the first two prototype imagers.

The focal plane for the SCUBA-2 camera will consist of two tiled imaging arrays, one each for the 450 μm and the 850 μm wavebands. Each array is made

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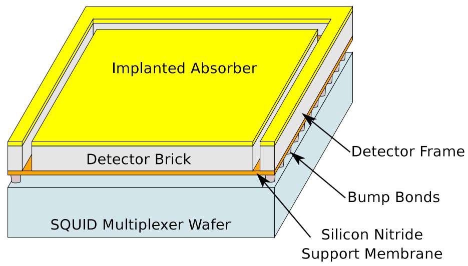

Fig. 1. Schematic drawing showing one pixel of the hybridized imager array. The upper detector wafer consists of a quarter-wave absorbing brick formed by an ion-implanted Si absorbing region on the upper surface and TES thermometer on the lower surface. The brick is supported by a thin Si_3N_4 membrane connecting the brick and the supporting Si frame. Electrical and thermal contact between the detector wafer and the underlying SQUID multiplexer wafer is made by the In-In bonds distributed throughout the multiplexer wafer and the detector frame.

up of four closely tiled 1280 (40 $\times$ 32) pixel subarrays. For simplicity in fabrication, the subarrays for each waveband are identical in all aspects except for absorber thickness and TES transition temperature.

Fig. 1 shows a sketch of the pixel structure. The completed detector consists of two hybridized (bump bonded) wafer-scale circuits. The bottom wafer is the SQUID multiplexer that is used to amplify the TES signals and perform time-division multiplexing, reducing the number of output channels to 32 [2,3]. The upper wafer-scale circuit consists of 1280 bolometer pixels, each comprised of a silicon frame, a Si_3N_4 thermal isolation membrane, and a radiation absorbing Si "brick" /TES structure. Each brick has a degenerate-doped layer on the upper surface (impedance matched to free-space), and a metallic TES on the bottom surface. The thickness of the brick is controlled to make a $\lambda/4$ absorbing cavity for the chosen waveband. Incident radiation is absorbed in the upper doped layer of the brick, causing the brick to heat with the subsequent temperature rise measured by the TES. Thermal isolation between the brick and frame is provided by etching a 10 μm wide gap between the brick and frame causing all thermal conduction to be through the thin supporting silicon nitride membrane. Electrical and thermal contacts between the TES wafer and the multiplexer are made by cold-welded indium contacts. The frame surrounding each pixel contains roughly 80 contacts, with an additional 200,000 thermal contacts forming a band around the array.

2. Fabrication

Fabrication of this complex structure takes place in three fabrication facilities requiring nine shipping steps of partially completed wafers. The formation and micromachining of the detector wafer is performed at the Scottish Microelectronics Centre (SMC); the fabrication of the superconducting circuitry and TESs occurs at NIST; and wafer hybridization is done at Raytheon. Because of the large hybridized area, particular care is taken to ensure wafer flatness, and to control stress and thermally induced wafer bowing.

The multiplexers are fabricated using the standard NIST SQUID process [4], with additional wiring and passivation layers for compatibility with subsequent hybridization steps. Because this 10-layer process requires relatively small (0.8 μm) minimum feature sizes, lithography is carried out using an i-line stepper.

The detector wafer fabrication has fewer lithography levels (8), but is considerably more complicated[5]. Initially a wafer is doped by ion-implantation, oxidized, and the oxide is patterned as a mask for the subsequent micromaching etch to form the bricks and frame. This wafer is then fusion bonded to a handle wafer. The composite wafer is then ground to the correct thickness for the quarter-wave cavity, and repolished. The silicon nitride membrane is deposited and the wafer is sent to NIST for TES fabrication. We use our standard Mo/Cu TES process [6] with the inclusion of two additional layers: SiO_2 passivation is deposited over the TES, as well as an additional Mo layer. The Mo layer is used as a superconducting shield between the TES and SQUID circuitry, and is used as the interconnect wiring for the hybridization process.

After completion of TES fabrication, flatness-matched multiplexer-detector wafer pairs are sent to Raytheon for hybridization. This is performed using Raytheon's standard In-based process. Here, thick ($\approx$ 10μm) indium pads are deposited on each wafer, and cold-welded under pressure. The hybridized wafer pair is returned to the SMC, where two separate etches are performed. This first removes the handle wafer from the back of the detector wafer, and the second etch forms the brick and frame. In the final prior to focal plane integration, the hybrid wafer is laser diced to the final size. Fig. 2 show photographs

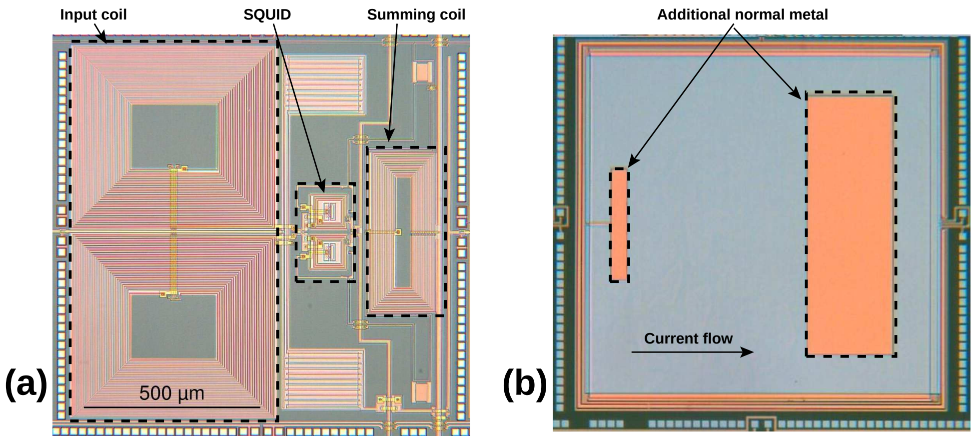

Fig. 2. Optical micrographs of a unit cell of the (a) SQUID multiplexer wafer and (b) TES side of the detector wafer. The large input coil couples the TES to the first-stage SQUID. The output of the SQUID is summed with the signals from other pixels in a column in the summing coil. In (b) we show one of the six varieties of TES pixels implemented in the 450 μm prototype. Here additional normal metal is used to suppress superconductivity in regions where flux from the input transformer and summing coil would interact with the TES. Additionally an electrically isolated superconducting shield is placed over the remainder of the TES to shield it from the SQUID circuitry. Note that the locations of coils on the SQUID and normal metal on the TES are mirror-imaged because the wafers are hybridized facing each other.

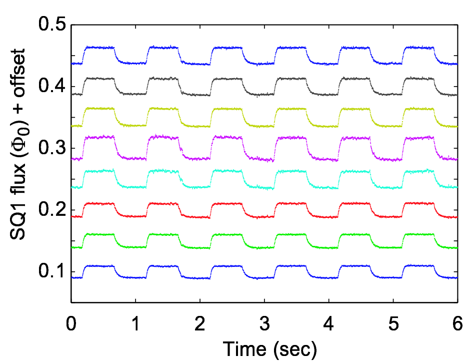

Fig. 3. Plot showing multiplexed optical response of 8 pixels to chopped narrowband 450 μm wavelength illumination. The incident optical power on each pixel is 1.8 fW. Plots are offset for clarity.

of the multiplexer and TES unit cell.

3. Results and Conclusions

We have successfully fabricated and measured both 850 μm and 450 μm prototype arrays. In both cases there were large non-working regions due to understood (and since corrected) processing defects. For each imager the operational portions of the arrays worked as expected. More complete data on the 850 μm prototype is presented elsewhere [7,8]. Because small interactions between the multiplexer and TES were observed in the 850 μm prototype, the 450 μm prototype was designed with six different pixel types, intended to minimize this interaction. Measurements show that the addition of normal metal regions and superconducting shielding to protect the TES from stray multiplexer fields were successful in eliminating the previously observed interaction, with the most effective design being the one shown in Fig. 2b. In Fig. 3 we show the response of eight of these pixels to chopped narrowband illumination.

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