SNAPSTRATE AND SOCKET FOR CHIP-ON-BOARD PROGRAMMABLE TECHNOLOGIES

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I. Introduction

The use of bare dice on flight hardware enables designers to use the most advanced integrated circuit (IC) technologies in the smallest possible footprint. The only way to get the dice affordably is to buy them the way industry does-as untested material. This requires designers of high reliability hardware to find inexpensive, quick turn-around, and straightforward strategies for testing the dice and assembling them onto boards. Having known good dice is especially important for complex designs or expensive parts, with high numbers of interconnections where rework would be expensive. It is even more important when the part requires programming at the field level.

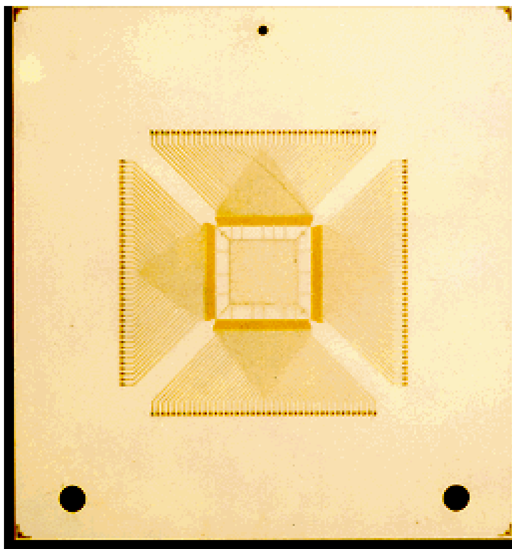
In the drive to exploit the benefits of using bare dice, a method for testing the dice prior to their integration into flight hardware is required. The Snapstrate was designed to provide a cost-effective vehicle for testing bare dice and producing Known Good Die.

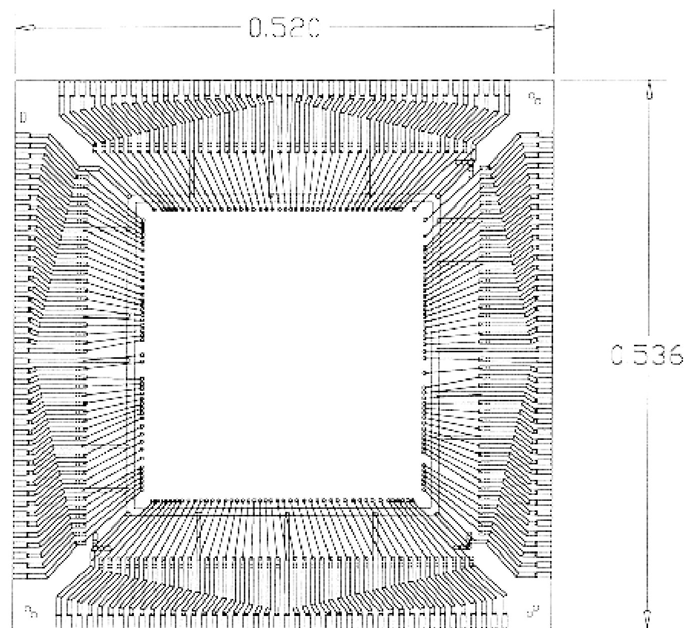
II. Background on Snapstrate Design

Many bare die sockets, also called Known Good Die sockets, are on the market to enable users to verify and program IC's at the die level. They tend not to be attractive to flight projects because they require device specific interfaces which are inherently difficult and expensive to produce. The Snapstrate, originally developed by Lockheed Martin Missile Systems, provides a simple, flexible, interface for testing a variety if dice.

The Snapstrate system uses a thin (15 mils), metallized ceramic substrate with perforations that border the die mount location (Figure 1). The IC die is attached to the center of the substrate and wire bonded to the inner trace ends. The die is then covered with epoxy to protect it from moisture and light which will negatively affect a programmed part. The traces fan out across the top of the substrate to the outer edge. Alignment holes are drilled at three locations on the substrate. The substrate is then positioned, up side down, in a commercial-off-the-shelf (COTS) socket which has conducting fingers which touch the end of each fanned out trace (Figure 2). A metal lid is laid on top of the substrate and the clips on either side of the socket are pushed into an indent on the top of the lid. Three alignment pins are used to control the position in which the substrate is placed into the socket and to limit movement of the lid while the clips are moved into place. The fingers are routed through the socket to a conversion PC board which has a standard pin grid array foot print, exactly like the one used for the packaged part sold by the part manufacturer. When all testing and programming is finished, the substrate is removed from the socket and the perforations are "snapped". This leaves a die, attached and wire bonded to a very small substrate, just slightly larger than its own footprint. The substrate is then attached and wire bonded directly to the PC board.

The candidate dice used to evaluate the Snapstrate system was an Actel FPGA that was intended to be used in Johns Hopkins Applied Physics Laboratory's C&DH in Your Palm, a C&DH system using chip-on-board and packaged parts. A purchase from Lockheed Martin was attempted but was not successful due to the small quantities required. The design of the substrate was then sent to a MCM substrate house and a small lot was made for the evaluation. Procurements were placed using industry standard practices and materials which were as close to





a) Snapstrate: trace width 6.5 mils, spaced 8.5 mils at the die end and 24 mils at the fan out end.

b) Wire Bond Diagram of a Excised Part

Figure 1. Snapstrate - KGD Carrier Substrate

the original concept as possible. This second set was populated with dice and was tested for electrical continuity and functionality. Dimensions for the lids were taken from one used by a prior build of socket assemblies that were used with Lockheed Martin Snapstrates. The socket assemblies were procured using the same part numbers as used for the prior build.

III. Problems Encountered

During assembly several problems were found relating to the routing of the conversion board and the mechanical dimensions of the socket assembly. After the routing error was compensated for, by repositioning the substrate in the socket, some of the socket pins were still not connecting to the substrate traces correctly. Each socket-to-PGA circuit path was probed and found to be good. An investigation of the wiping registration was performed and it was found that though some of the contact points (socket spring finger-to-trace land) were slightly off-set almost all were making sufficient contact. A few were not and it was thought that the spring fingers were not being compressed sufficiently or that they were insufficiently co-planar (Figure 3).

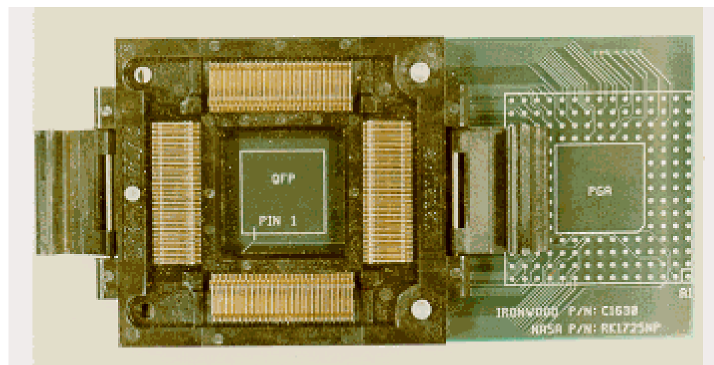


Figure 2a. Snapstrate Test Socket (topside)

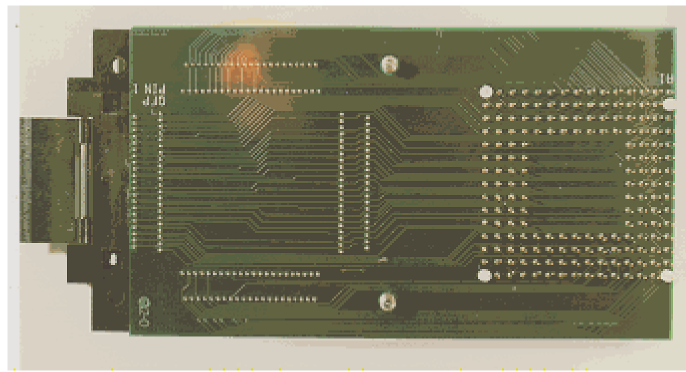


Figure 2b. Snapstrate Test Socket (bottomside)

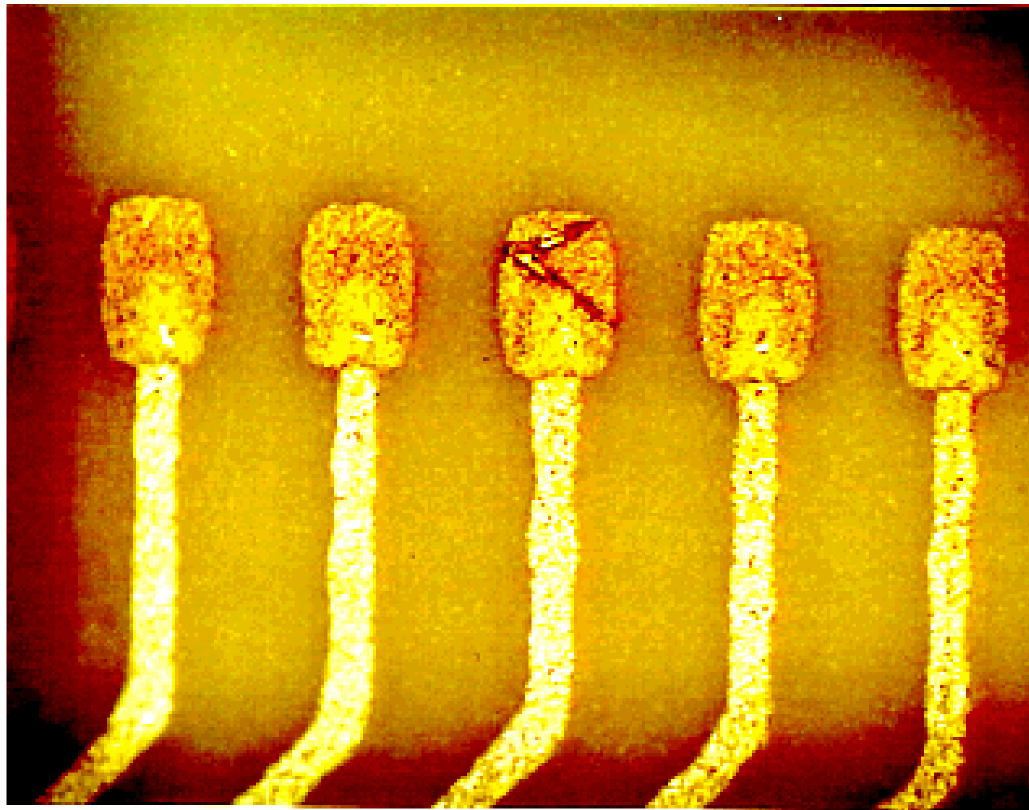


Figure 3a. Little contact between the spring fingers and snapstrate lands.

Examination by both GSFC and the socket manufacturer, Nepenthe, revealed that several problems existed with the lid design. It was too thick and caused the substrate to crack during application of the socket side clips. The indents on the metal lid were not designed to allow the clips to slowly move into place but to do so abruptly. These two problems caused the lid to push the snapstrate to one side (opposite to whichever side was clipped first) which caused the traces to loose alignment with the spring fingers on the socket. Finally, the three alignment pins were not sufficient to keep the socket lid aligned. An alignment edge is required on the socket base to establish alignment via a primary socket feature rather than through the pins. The pins had outer diameter tolerance slop and were not positioned by a dimension that determined the spring fingers' position. Nepenthe provided a sketch of a possible redesign of the lid (Figure 4).

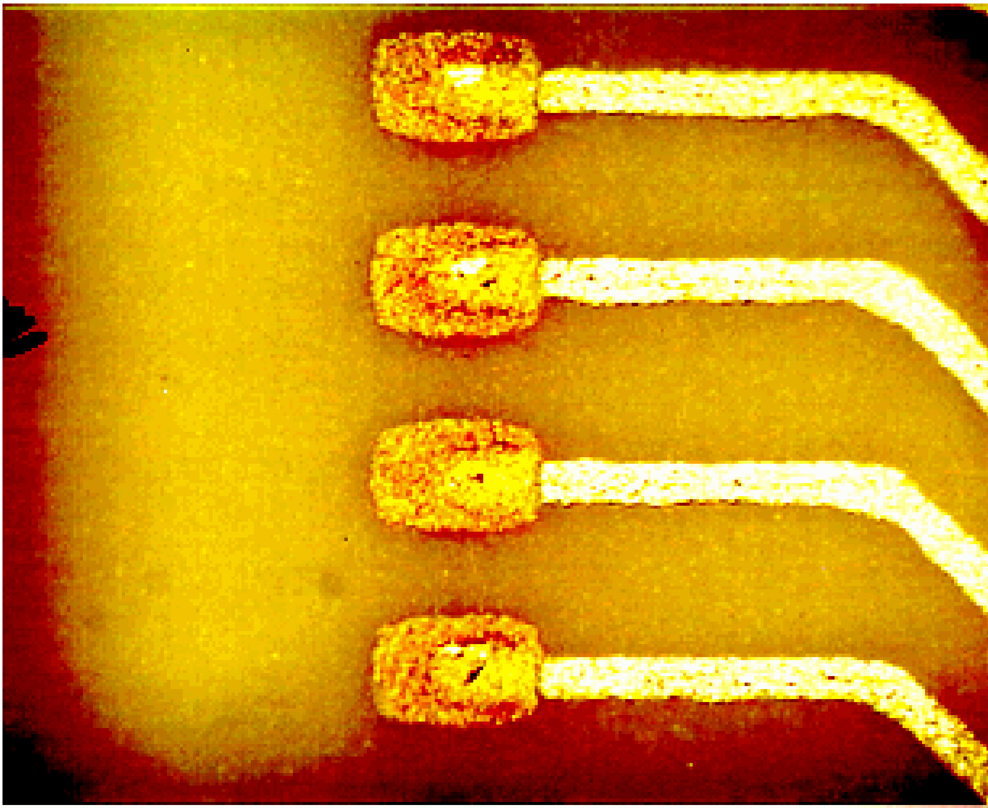


Figure 3b. Good alignment and good contact

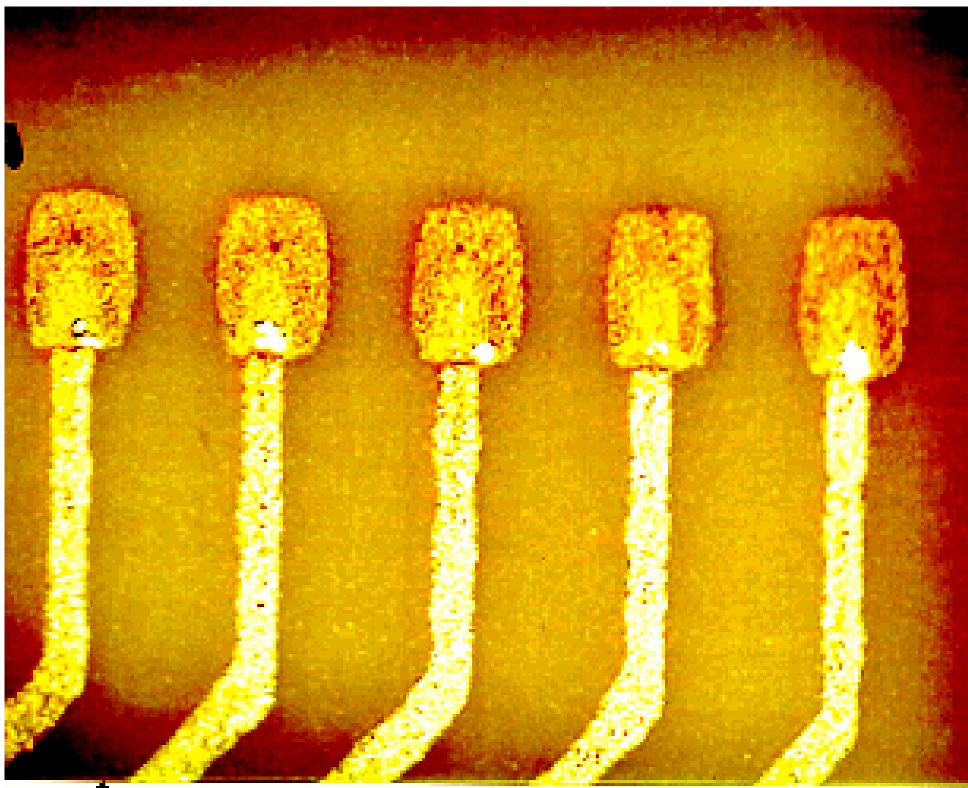
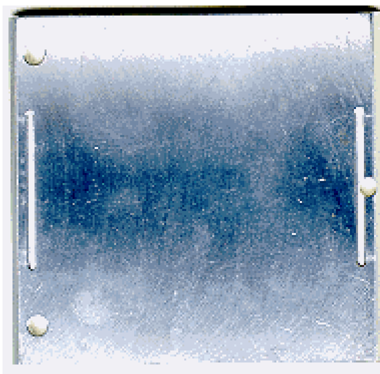


Figure 3c. Poor alignment and good contact


>(a) original lid

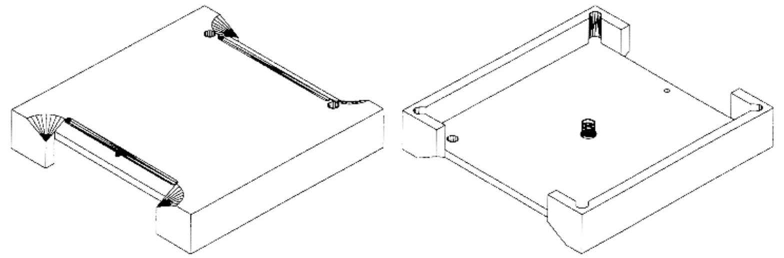

(b) suggested new lid

Figure 4. Socket Lid

IV. Summary

The snapstrate KGD carrier concept is a useful one, especially for programmable parts such as FPGA's. The metallized substrate can be easily and affordably designed and procured in small quantities. Designing with a sufficiently high number of pin-outs will allow it to be used for other dice as well without additional engineering costs.

By using the commercial socket and adaptor board, costs can be further reduced and small quantities can be bought. The burden exists in designing the hardware which adapts the socket from one that is made for leaded parts, to one that is usable with a metallized substrate. This seems possible but requires engineering design and validation of the lid system. Though this is not trivial, once completed, it should work for the commercial socket as long as the spring finger coplanarity is maintained. This may or may not be possible since it is a COTS product. Also, new lids would have to be designed if a different socket were required. Though this may seem expensive, it is less costly than absorbing the non-recurring engineering costs associated with a commercial socket manufacturer's design and fabrication of a special socket for the Snapstrate.

V. Recommendations

As chip-on-board becomes more commonly used in space flight hardware, the lid system for the Nepenthe socket should be studied and a new lid designed and validated.

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