ROD Cost and Schedule

December 17, 1999

Wisconsin

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Lukas Tomasek

Material Covered:

Comparison of Old and Cost to Complete Schedule

Specifics of Cost to Complete Schedule

Comparison of Old and Cost to Complete Cost Estimate

Specifics of Cost to Complete Cost Estimate

Contingency of Cost to Complete

ROD Cost and Schedule

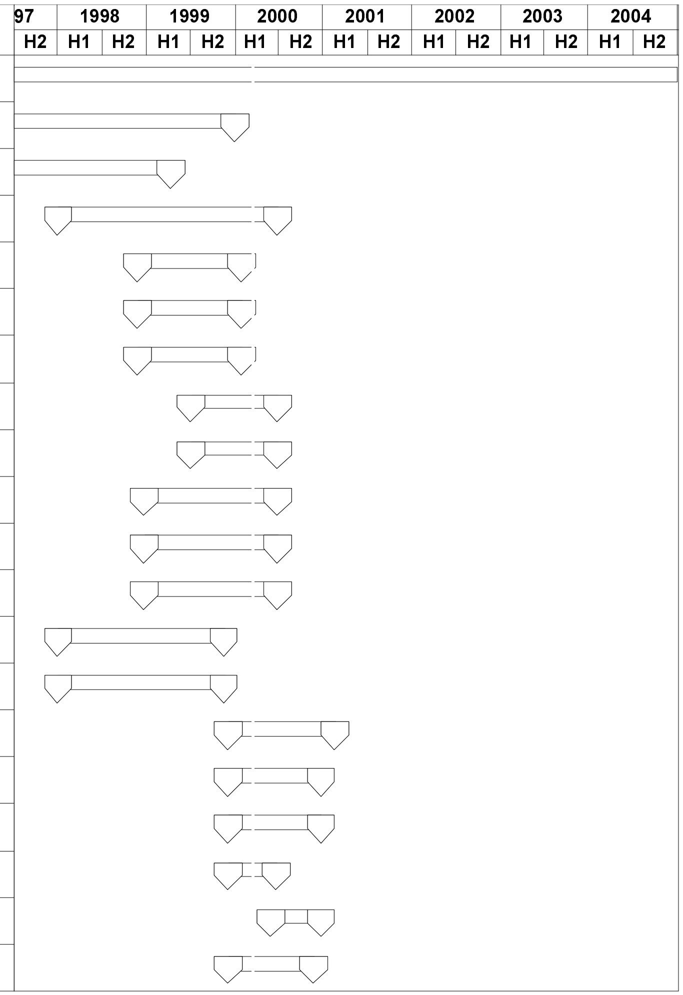
Comparison of Old and New Schedule

Task Name	Old Dates	New Dates
Design Rod Card	10/97-4/00	12/98 to 7/00
ROD Prototypes	9/99 to 12/00	4/99 to 2/01
ROD Fabrication	7/00 to 3/03	2/01 to 5/02
ROD Installation	5/02 to 10/04	5/01 to 10/04

ROD Cost and Schedule

Old Schedule

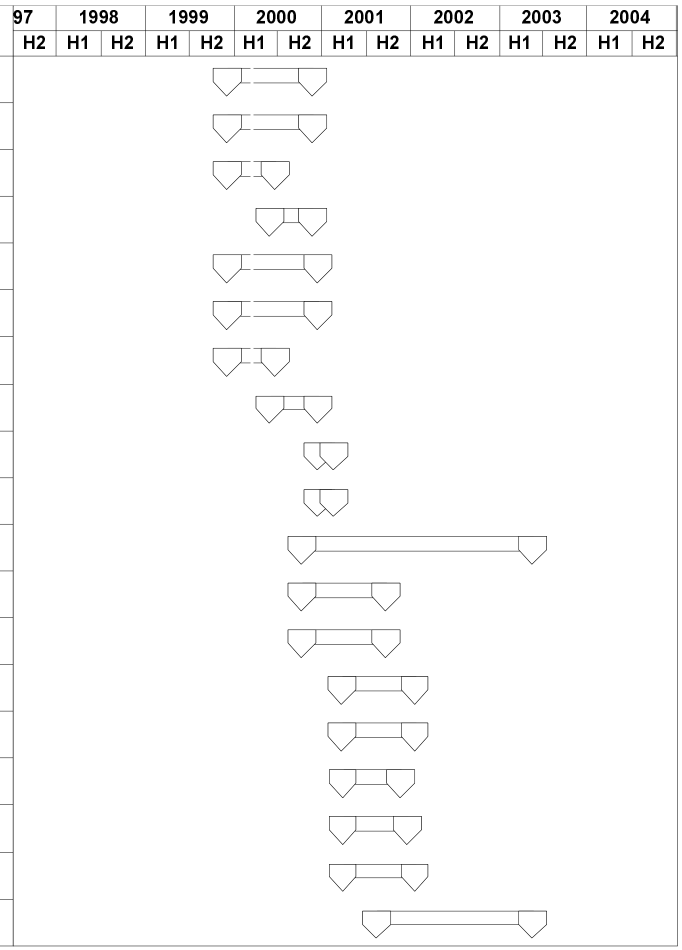
ID	WBS	Task Name	Duration	Start	Finish
1	1.1.3	ROD Design & Fabrication	2349 d	Mon 10/2/95	Thu 9/30/04
2	1.1.3.1	Test Beam Support	1044 d	Mon 10/2/95	Thu 9/30/99
7	1.1.3.2	ROD System Design	529 d	Wed 1/1/97	Mon 1/11/99
22	1.1.3.3	Design ROD Cards	652 d	Wed 10/1/97	Thu 3/30/00
23	1.1.3.3.1	Common design	311 d	Mon 8/24/98	Mon 11/1/99
29	1.1.3.3.2	Strip design	311 d	Mon 8/24/98	Mon 11/1/99
34	1.1.3.3.3	Pixel design	311 d	Mon 8/24/98	Mon 11/1/99
39	1.1.3.3.4	Test stand design	261 d	Thu 4/1/99	Thu 3/30/00
40		Resources	261 d	Thu 4/1/99	Thu 3/30/00
63	1.1.3.3.6	Strip Specific ASIC Design	397 d	Mon 9/21/98	Wed 3/29/00
67	1.1.3.3.5	Pixel Specific ASIC Design	398 d	Mon 9/21/98	Wed 3/29/00
68		Resources	398 d	Mon 9/21/98	Wed 3/29/00
75	1.1.3.3.7	Preprototype ROD	493 d	Wed 10/1/97	Fri 8/20/99
76		Resources	493 d	Wed 10/1/97	Fri 8/20/99
106	1.1.3.4	ROD Prototypes	319 d	Fri 9/3/99	Wed 11/22/00
107	1.1.3.4.1	ROD Common Prototypes	277 d	Fri 9/3/99	Mon 9/25/00
108		Resources	277 d	Fri 9/3/99	Mon 9/25/00
111		Common Prototype	144 d	Fri 9/3/99	Wed 3/22/00
126		Common Preproduction Mode	154 d	Wed 2/23/00	Mon 9/25/00
140	1.1.3.4.2	ROD Strip Prototypes	256 d	Fri 9/3/99	Fri 8/25/00



ROD Cost and Schedule

Old Schedule

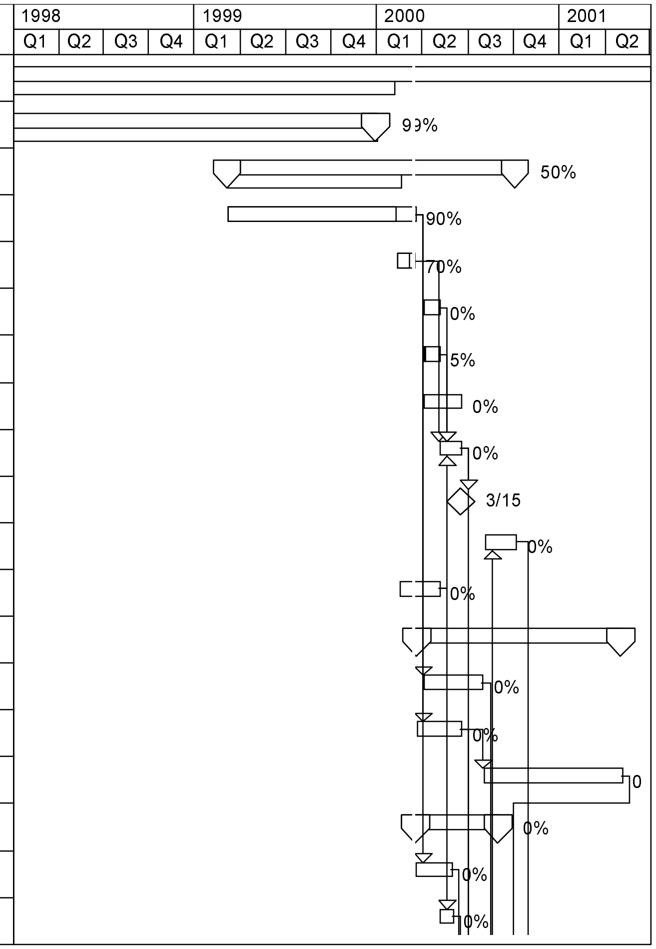
ID	WBS	Task Name	Duration	Start	Finish
140	1.1.3.4.2	ROD Strip Prototypes	256 d	Fri 9/3/99	Fri 8/25/00
141		Resources	256 d	Fri 9/3/99	Fri 8/25/00
144		Strip Prototype	144 d	Fri 9/3/99	Wed 3/22/00
159		Strip Preproduction Model	133 d	Wed 2/23/00	Fri 8/25/00
173	1.1.3.4.3	ROD Pixel Prototypes	267 d	Fri 9/3/99	Mon 9/11/00
174		Resources	267 d	Fri 9/3/99	Mon 9/11/00
177		Pixel Prototype	144 d	Fri 9/3/99	Wed 3/22/00
192		Pixel Preproduction Model	144 d	Wed 2/23/00	Mon 9/11/00
207	1.1.3.4.4	ROD System Test	53 d	Mon 9/11/00	Wed 11/22/00
208		Resources	53 d	Mon 9/11/00	Wed 11/22/00
221	1.1.3.5	ROD Fabrication	685 d	Thu 7/6/00	Wed 2/19/03
227	1.1.3.5.2	ROD Strip ASIC Fab	252 d	Thu 7/6/00	Fri 6/22/01
235	1.1.3.5.1	ROD Pixel ASIC Fab	252 d	Thu 7/6/00	Fri 6/22/01
245	1.1.3.5.3	ROD 5% Production	218 d	Wed 12/20/00	Fri 10/19/01
246		Resources	218 d	Wed 12/20/00	Fri 10/19/01
249		5% Common Board	174 d	Wed 12/20/00	Tue 8/21/01
265		5% Strip Board	194 d	Wed 12/20/00	Tue 9/18/01
286		5% Pixel Board	217 d	Wed 12/20/00	Fri 10/19/01
300	1.1.3.5.4	ROD 95% Production	464 d	Fri 5/11/01	Wed 2/19/03



ROD Cost and Schedule

Cost to Complete Schedule

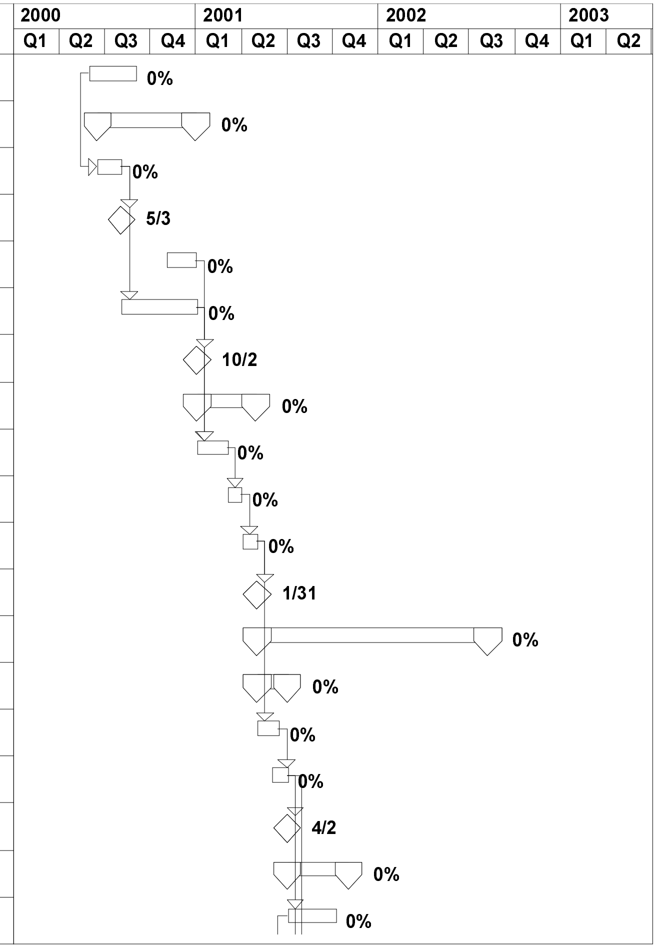
ID	WBS	Task Name	Duration	Start	Finish
1	1.1.3	ROD Design & Fabrication	2346 d	Sun 10/1/95	Mon 9/27/04
2	1.1.3.1	Test Beam Support	1044 d	Sun 10/1/95	Thu 9/30/99
22	1.1.3.3	Design ROD Cards	415 d	Thu 12/3/98	Wed 7/5/00
23	1.1.3.3.1	Formater Design	270 d	Thu 12/3/98	Wed 12/15/99
24	1.1.3.3.2	Event Fragment Builder design	25 d	Wed 11/10/99	Tue 12/14/99
25	1.1.3.3.3	Multiplexer Design	22 d	Mon 1/3/00	Tue 2/1/00
26	1.1.3.3.4	ROD Controler Design	22 d	Mon 1/3/00	Tue 2/1/00
27	1.1.3.3.5	DSP Processor Design	53 d	Mon 1/3/00	Wed 3/15/00
28	1.1.3.3.6	Board Level Simulation	31 d	Wed 2/2/00	Wed 3/15/00
29	1.1.3.3.6	Complete Board Level Simulation	0 d	Wed 3/15/00	Wed 3/15/00
30	1.1.3.3.7	Pisel specific Formater VHDL	45 d	Thu 5/4/00	Wed 7/5/00
31	1.1.3.3.8	RPD Schematic and PC Layout	57 d	Mon 11/15/99	Tue 2/1/00
32	1.1.3.4	ROD Test Stand	295 d	Mon 12/20/99	Fri 2/2/01
33	1.1.3.4.1	Test Stand Hardware	85 d	Mon 1/3/00	Fri 4/28/00
34	1.1.3.4.2	SCT Test Stand Software	64 d	Mon 12/20/99	Thu 3/16/00
35	1.1.3.4.,3	Pixel Test Stand Software	200 d	Mon 5/1/00	Fri 2/2/01
36	1.1.3.5	ROD Prototypes	120 d	Thu 12/16/99	Wed 5/31/00
37	1.1.3.5.1	ROD Protoype Parts Order	52 d	Thu 12/16/99	Fri 2/25/00
38	1.1.3.5.2	ROD Prototype PC Order	20 d	Wed 2/2/00	Tue 2/29/00



ROD Cost and Schedule

Cost to Complete Schedule

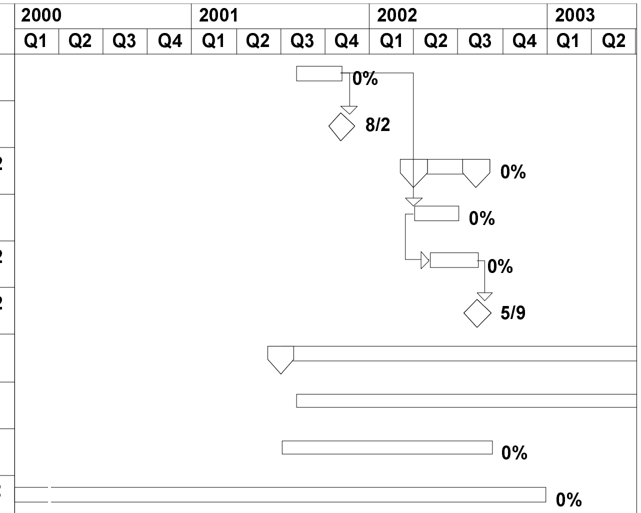
ID	WBS	Task Name	Duration	Start	Finish
39	1.1.3.5.3	ROD Prototype PC Loading	66 d	Wed 3/1/00	Wed 5/31/00
40	1.5	**ROD Prototype Evaluation**	**142 d**	**Fri 3/17/00**	**Mon 10/2/00**
41	**1.1.3.6**	**SCT Prototype Testing**	**34 d**	**Fri 3/17/00**	**Wed 5/3/00**
42	**1.1.3.6.1**	**Complete SCT ROD Testing**	**0 d**	**Wed 5/3/00**	**Wed 5/3/00**
43	**1.1.3.6.2**	**Pixel Prototype Testing**	**44 d**	**Tue 8/1/00**	**Fri 9/29/00**
44	**1.1.3.6.3**	**User Evaluation of ROD**	**108 d**	**Thu 5/4/00**	**Mon 10/2/00**
45	**1.1.3.6.3**		**0 d**	**Mon 10/2/00**	**Mon 10/2/00**
46	**1.1.3.7**	**Rod Production Model**	**87 d**	**Tue 10/3/00**	**Wed 1/31/01**
47	**1.1.3.7.1**		**43 d**	**Tue 10/3/00**	**Thu 11/30/00**
48	**1.1.3.7.2**		**21 d**	**Fri 12/1/00**	**Fri 12/29/00**
49	**1.1.3.7.3**		**23 d**	**Mon 1/1/01**	**Wed 1/31/01**
50	**1.1.3.7.3**		**0 d**	**Wed 1/31/01**	**Wed 1/31/01**
51	**1.1.3.8**	**ROD Fabrication**	**331 d**	**Thu 2/1/01**	**Thu 5/9/02**
52	**1.1.3.8.1**	**ROD 5% Production**	**43 d**	**Thu 2/1/01**	**Mon 4/2/01**
53	**1.1.3.8.1.1**		**30 d**	**Thu 2/1/01**	**Wed 3/14/01**
54	**1.1.3.8.1.2**	**ROD 5% Production Debuggin**	**22 d**	**Thu 3/1/01**	**Fri 3/30/01**
55	**1.1.3.8.1.2**	**Rod 5% Production complete**	**1 d**	**Mon 4/2/01**	**Mon 4/2/01**
56	**1.1.3.8.2**	**ROD 45% Production**	**89 d**	**Mon 4/2/01**	**Thu 8/2/01**
57	**1.1.3.8.2.1**		**70 d**	**Mon 4/2/01**	**Fri 7/6/01**



ROD Cost and Schedule

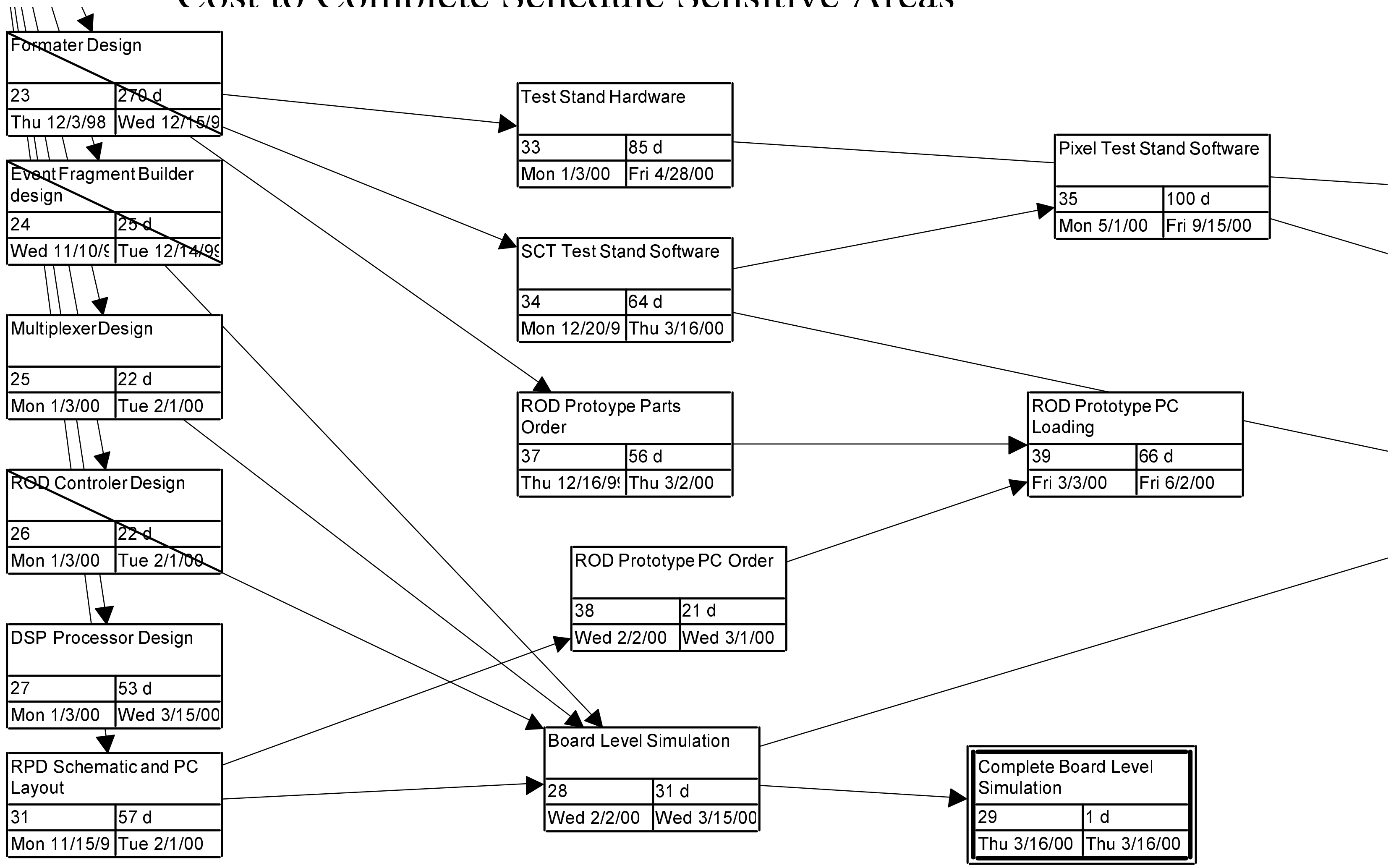
Cost to Complete Schedule

ID	WBS	Task Name	Duration	Start	Finish
58	1.1.3.8.2.2	ROD 45% Production Debuggin	68 d	Tue 5/1/01	Thu 8/2/01
59	1.1.3.8.2.2	ROD 45% Production complete	0 d	Thu 8/2/01	Thu 8/2/01
60	**1.1.3.8.3**	**ROD 50% Production**	**93 d**	**Tue 1/1/02**	**Thu 5/9/02**
61	**1.1.3.8.3.1**		**65 d**	**Tue 1/1/02**	**Mon 4/1/02**
62	**1.1.3.8.3.2**		**70 d**	**Fri 2/1/02**	**Thu 5/9/02**
63	**1,.1.4.8.3.2**	**ROD 50% Production Comple**	**0 d**	**Thu 5/9/02**	**Thu 5/9/02**
64	**1.1.3.9**		**911 d**	**Mon 4/2/01**	**Mon 9/27/04**
65	**1.1.3.9.1**	**ROD Installation and Repair**	**890 d**	**Tue 5/1/01**	**Mon 9/27/04**
66	**1.1.3.9.2**	**ROD Shipping**	**310 d**	**Mon 4/2/01**	**Fri 6/7/02**
67	**1.1.3.10**	**Project Management**	**780 d**	**Fri 10/1/99**	**Thu 9/26/02**



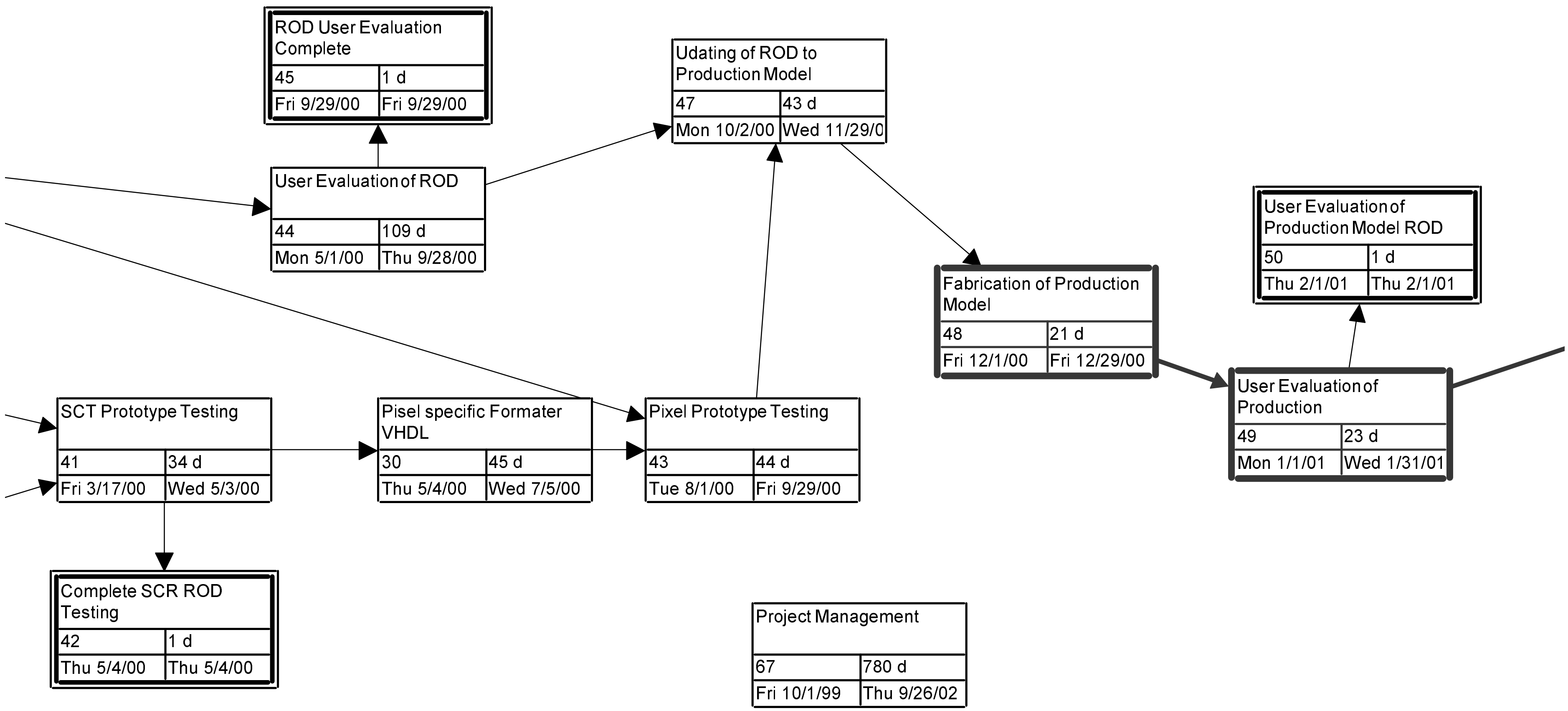
ROD Cost and Schedule

Cost to Complete Schedule Sensitive Areas



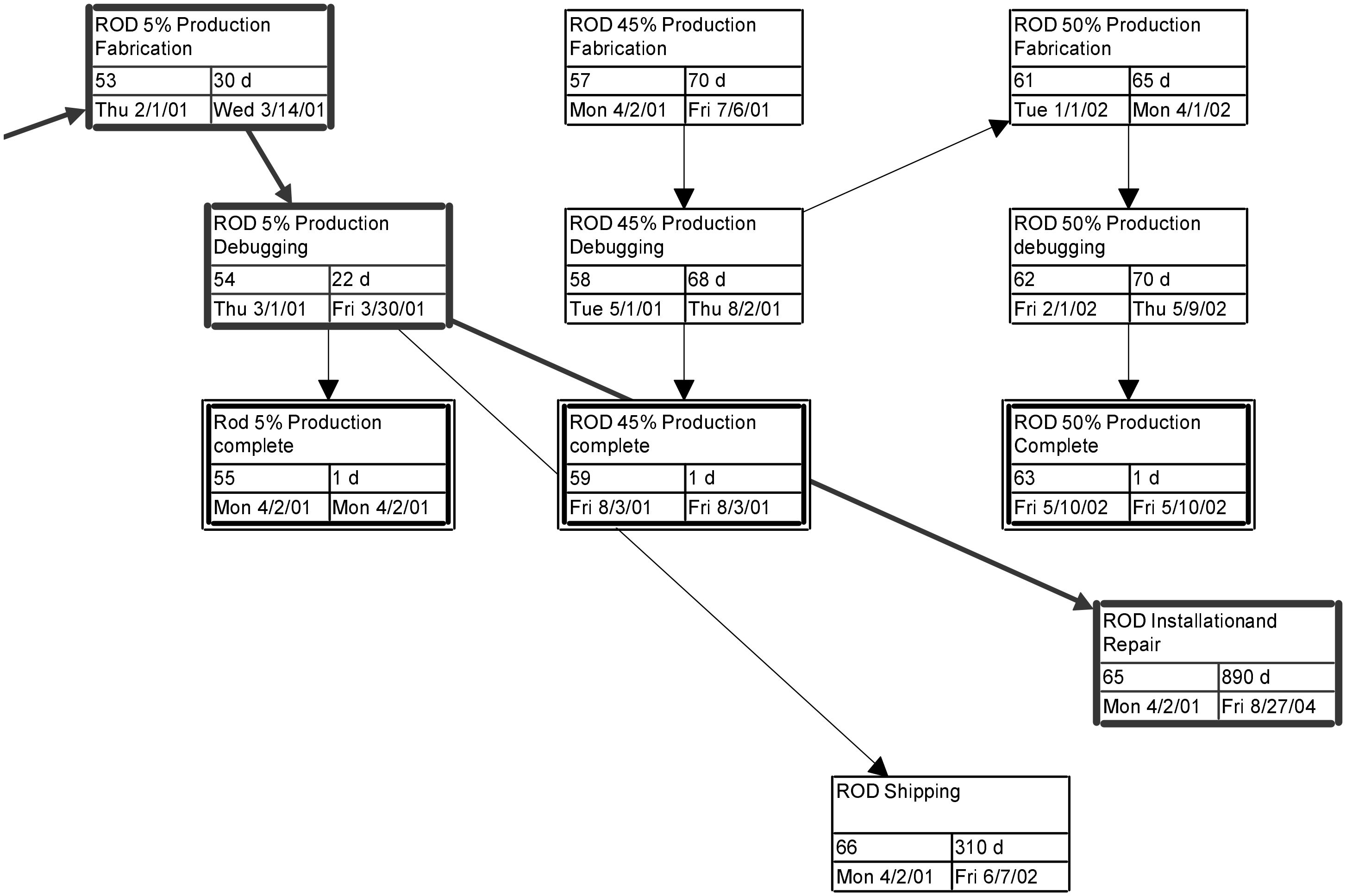
ROD Cost and Schedule

Cost to Complete Schedule Sensitive Areas



ROD Cost and Schedule

Cost to Complete Schedule Sensitive Areas



ROD Cost and Schedule

Comparison of Costs

Old Cost With Contingency (FY97)		3,700 k$
Funding Spent to 10/1/99	630k$	
Cost to Complete 10/1/99 to End	3308k$	
Total Cost to Complete with contingency(FY00)		3,938k$

ROD Cost and Schedule

Specifics of Cost to Complete

U.S. ATLAS E.T.C.
WBS Summary Cost Estimates

Funding Source: All **Funding Type:** Project 12/17/99 7:01:29 AM

Institutions: All

WBS Number	Description	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
1.1.3	RODs	2669	639	24	3308	862	160	167	1480	7.4	0.1
1.1.3.1	Test Beam Support	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.1.1	Strip Test Beam Support	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.1.1.1	Strip TBS UCI	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.1.1.2	Strip TBS UW	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.1.2	Pixel Test Beam Support	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.1.2.1	Pixel TBS UCI	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.1.2.2	Pixel TBS UW	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.2	ROD System Design	3	0	0	3	3	0	0	0	0.0	0.1
1.1.3.2.1	ROD Requirements	3	0	0	3	3	0	0	0	0.0	0.1
1.1.3.2.1.1	Requirements UCI	3	0	0	3	3	0	0	0	0.0	0.1
1.1.3.2.1.2	Requirements UW	0	0	0	0	0	0	0	0	0.0	0.0

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ROD Cost and Schedule

Specifics of Cost to Complete

WBS Number	Description	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
1.1.3.2.2	ROD Essential Model	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.2.2.1	Essential Model UCI	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.2.2.2	Essential Model UW	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.2.3	ROD Implementation Model	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.2.3.1	Implementation Model UCI	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.2.3.2	Implementation Model UW	0	0	0	0	0	0	0	0	0.0	0.0
1.1.3.3	**ROD Design**	329	92	28	421	329	0	0	0	2.2	0.0
1.1.3.3.1	Formater Design	15	4	28	20	15	0	0	0	0.1	0.0
1.1.3.3.2	Event Fragment Builder Design	38	11	28	49	38	0	0	0	0.2	0.0
1.1.3.3.3	Multiplexer Design	31	9	28	39	31	0	0	0	0.2	0.0
1.1.3.3.4	ROD Controller Design	46	13	28	59	46	0	0	0	0.3	0.0
1.1.3.3.5	DSP Processor Design	31	9	28	39	31	0	0	0	0.2	0.0
1.1.3.3.6	Board Level Simulation of the S	34	9	28	43	34	0	0	0	0.2	0.0
1.1.3.3.7	Pixel specific Formater VHDL D	77	21	28	98	77	0	0	0	0.5	0.0
1.1.3.3.8	ROD Schematic and PC Layout	57	16	28	73	57	0	0	0	0.5	0.0
1.1.3.4	**ROD Test Stand**	147	37	25	184	61	0	0	86	0.4	0.0
1.1.3.4.1	Test Stand Hardware	101	24	24	125	15	0	0	86	0.1	0.0
1.1.3.4.2	SCT Test Stand Software	15	4	28	20	15	0	0	0	0.1	0.0
1.1.3.4.3	Pixel Test stand Software	31	9	28	39	31	0	0	0	0.2	0.0
1.1.3.5	**ROD Prototypes**	136	38	28	175	25	0	13	99	0.2	0.0
1.1.3.5.1	ROD Prototype Parts Order	110	31	28	140	10	0	0	99	0.1	0.0
1.1.3.5.2	ROD Prototype PC order	17	5	28	22	4	0	13	0	0.0	0.0
1.1.3.5.3	ROD Prototype PC Loading	10	3	28	13	10	0	0	0	0.1	0.0

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ROD Cost and Schedule

Specifics of Cost to Complete

WBS Number	Description	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
1.1.3.6	ROD Protype evaluated	83	23	28	106	76	0	7	0	0.5	0.0
1.1.3.6.1	SCT prototype testing	35	10	28	45	35	0	0	0	0.2	0.0
1.1.3.6.2	Pixel proto type testing	20	6	28	26	20	0	0	0	0.1	0.0
1.1.3.6.3	User evaluation of ROD	27	8	28	35	20	0	7	0	0.1	0.0
1.1.3.7	ROD Production Model	134	29	22	163	105	0	30	0	0.8	0.0
1.1.3.7.1	Updating of ROD to Production	44	10	23	54	44	0	0	0	0.3	0.0
1.1.3.7.2	Fabrication of production Mode	51	10	19	61	25	0	26	0	0.2	0.0
1.1.3.7.3	User evaluion of production mo	39	9	24	48	35	0	4	0	0.2	0.0
1.1.3.8	ROD Fabrication	1459	350	24	1809	0	160	4	1295	1.3	0.0
1.1.3.8.1	ROD 5 % Production	107	26	24	132	0	52	0	55	0.4	0.0
1.1.3.8.1.1	ROD 5% Production Fabricati	81	19	24	100	0	26	0	55	0.2	0.0
1.1.3.8.1.2	ROD 5% Production Debug	26	6	24	32	0	26	0	0	0.2	0.0
1.1.3.8.2	ROD 45 % Production	465	112	24	577	0	52	0	413	0.4	0.0
1.1.3.8.2.1	ROD 45% Production Fabricat	422	101	24	523	0	9	0	413	0.1	0.0
1.1.3.8.2.2	ROD 45% Production Debug	43	10	24	54	0	43	0	0	0.3	0.0
1.1.3.8.3	ROD 50% Production	695	167	24	862	0	56	4	636	0.5	0.0
1.1.3.8.3.1	ROD 50% Production Farbicat	606	145	24	751	0	9	0	597	0.1	0.0
1.1.3.8.3.2	ROD 50% Production Debug	89	21	24	111	0	47	4	39	0.4	0.0
1.1.3.8.4	Purchase ROD Crates	192	46	24	238	0	0	0	192	0.0	0.0
1.1.3.9	ROD Installation, Repair and Ship	197	47	24	244	172	0	25	0	1.3	0.0

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ROD Cost and Schedule

Specifics of Cost to Complete

WBS Number	Description	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
1.1.3.9.1	ROD Installation and Repair	181	43	24	224	163	0	18	0	1.2	0.0
1.1.3.9.2	ROD shipping	16	4	24	20	10	0	7	0	0.1	0.0
1.1.3.10	Project Management	92	22	24	114	92	0	0	0	0.6	0.0

WBS Number: 1.1.3 **Description:** RODs

Institution : **Contact:** R. Jared

This item covers the design of the Read Out Drivers (ROD) and test beam support. The RODs are the interface card between the pixel and silicon strip front end electronics and the Data Acquisition (DAQ) components of ATLAS. Card size is 9U by 400 mm deep . There are two main functions of the card. One is to provide for the distribution of ATLAS control, clock and trigger information to the front end (on detector) electronics modules. The other function is to collect event data from multiple front end modules and package events that are transmitted to the DAQ. The US provides all of the cards. Remaining cost is provided by the European collaborators that will design and fabricate the back of the crate card (optical interface) for the SCT RODs. The design of the back of the crate card for the pixels will be done by our European collaboraters.

Test beam support is the design and fabrication of electronics to support the development of the integrated circuits for the silicon and pixel front end electronics. Silicon strip and pixel test beam activities are supported by the design and fabrication of so called DSP(digital signal processor) cards that interface the front end electronics to the readout system. There are 50 of these cards; 40 for the silicon strip and 10 for the pixel electronics. The other effort is to design and fabricate cards that directly support the developing front end ASICs. Silicon strips require a simple front end card. There are 40 of these cards. Pixels require a much more complex card that supports the functionality that will eventually be incorporated into the ASIC. There are 3 generations of this card that must be designed and fabricated. There are 9 copies of the card required. Additional test beam support is provided by non-US collaborators in the form of purchase of more DSP cards, software support and
the design and fabrication of some aspects of the pixel test beam support systems.

Details of Estimate: This item covers the design of the Read Out Drivers (ROD) and test beam support. The US provides all of the 225 ROD cards.

Number of Items - RODs

Number of RODs 225 (10% spares)

Number of Test Stands 3

Number of Items - Test Beam Support

Number of DSP Modules 50
Number of Pixel support cards 9
Number of strip support cards 40

COST SUMMARY: (Project)	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	2669	639	24	3308	862	160	167	1480	7.4	0.1

MANPOWER SUMMARY:	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
MFG P	0	944	0	0	1104	174	0	0	0	0	0	0	159.967
MFG B/I	0	1	0	0	0	0	0	0	0	0	0	0	0.088
EDIA P	0	7847	0	0	2968	0	0	0	0	0	0	0	861.741
EDIA B/I	0	106	0	0	0	0	0	0	0	0	0	0	5.605
	0	8898	0	0	4072	174	0	0	0	0	0	0	1027.401

ROD Cost and Schedule

Selected Cost Book Items

U.S. Atlas Cost Book 12/12/99 9:35:06 PM

WBS Number: 1.1.3.3 **Description:** ROD Design

Institution : **Contact:** R. Jared

This item contains all the Material and labor to design the ROD cards.

Details of Estimate: This item contains all the Material and labor to design the ROD cards.

Formater Design Simulation 1.1.3.3.1
Note 103k$ needs to be added to this item in FY99 to balance the spending on the preprototype ROD. This will make the previous spending agree with actuals.
The formater VHDL was finished in FY99. The remaining task is to simulate the code.
Labor
174 hr EE to perform the simulation

Event Fragment Builder Design 1.1.3.3.2
This is the module that gathers the data from the links and places the data in one record.
Labor
261 hr EE to code the VHDL
174 hr EE to simulate the code.

Multiplexer 1.1.3.3.3
This is the module that receives the data from the event fragment builder and directs the data to the S-link and or the DSPs
Labor
174 hr EE to write the VHDL code
174 hr EE to simulated the code

ROD Controller 1.1.3.3.4
This is the module that communicate between VME and the ROD.
Labor
348 hr EE to write the VHDL code
174 hr EE to simulate the code.

DSP Processor Design 1.1.3.35
These are the engines that monitor errors, monitor data and perform calibration functions.
Labor
174 hr EE to define the communication protocol
87 hr EE to help in the SCT software development
87 hr EE to help in the pixel software development

Board Level Simulation of the SCT ROD Design 1.1.3.3.6
The simulation of the board and comparisons with the C code model are needed to comfirm that the board will perform as expected.
Labor
384 hr EE to simulate the board.

Pixel specific Formater VHDL Design 1.1.3.3.7
The pixels have two different formats. One is a single 80 MHz optical link that arrives at the ROD as two 40 MHz serial lines that round robins the data. The other is a two 80 MHz optical link that arrives at the ROD as four 40 MHz serial lines that round robins the data.
Labor
348 hr EE to write the VHDL code for the 4 input case
174 hr EE to simulate the VHDL code for the 4 input case
174 he EE to write the VHDL code for the 2 input case
174 hr EE to simulate the VHDL code for the 3 input case
Total of 870 hr EE

ROD Cost and Schedule

Selected Cost Book Items

U.S. Atlas Cost Book 12/12/99 9:35:06 PM

ROD Schematic and PC Layout 1.1.3.3.7
Labor
174 hr EE to oversee the schematic and PC layout
348 hr ET to enter the schematic
348 hr ET to procude the PB layout

COST SUMMARY: (Project)	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	329	92	28	421	329	0	0	0	2.2	0.0

MANPOWER SUMMARY:	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
EDIA P	0	3255	0	0	696	0	0	0	0	0	0	0	328.520
	0	3255	0	0	696	0	0	0	0	0	0	0	328.520

ROD Cost and Schedule

Selected Cost Book Items

WBS Number: 1.1.3.4 **Description:** ROD Test Stand

Institution : **Contact:** R. Jared

This item contains the material and labor to design and fabricate the ROD test stand. It is composed of a crates, National Instruments interface and IBM PCs.

Details of Estimate: This item contains the material and labor to design and fabricate the ROD test stand. It is composed of a crates, National Instruments interface and IBM PCs. Three test stands will be fabricated. One each for ROD, pixel and SCT use. The ROD has been designed to provide for its own generation of input data and trapping of output data. The crate back plane is being layed out in England. We will fabricated 10 copies for use in the SCT and Pixel communities.

Crate, National Instruments interface and IBM PC
Labor:
87 hr EE to oversee the back-plane and test stand hardware selection
122 hr ET to coordinate and assemble test stands

Material:
$36,000 Crate 3 ea. Resent quotes in England are at $12,000 per crate.
$13,500 Back plane (1.5k NRE + 1200 x 10 + 13.5k)
$11,000 IBM PC (3.5k x 3 = 11k)
$16.200 Notional Instruments interface (5.4k x 3)
Total Materials $73,000

SCT Test Stand Software
Labor:
174 EE

Pixel Test Stand Software
Labor:
348 EE

COST SUMMARY: (Project)

Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
147	37	25	184	61	0	0	86	0.4	0.0

MANPOWER SUMMARY:

	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
EDIA P	0	609	0	0	122	0	0	0	0	0	0	0	60.971
	0	609	0	0	122	0	0	0	0	0	0	0	60.971

MATERIAL SUMMARY:

	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
MFG P	77	0	0	0	0	0.0	85.701
	77	0	0	0	0	0.0	85.701

ROD Cost and Schedule

Selected Cost Book Items

WBS Number: 1.1.3.5 **Description:** ROD Prototypes

Institution : **Contact:** R. Jared

This item contains the material and labor to fabricate prototypes of the ROD cards.

Details of Estimate: This item contains the material and labor to fabricate prototypes of the ROD cards. One iteration of the ROD prototype is performed. Resent experience with cards of similare complexity is sufficient. A second iteration is planned in the production model phase to correct small defects. 12 sets of parts are ordered and 10 PC cards are fabricated. 9 cards are loaded.

ROD prototype parts order:
Labor:
174 hr ET to order parts
Material:
$88,992 ($4944 production parts cost x 1.5 small order factor x 12 parts sets = $88,992)

ROD prototype PC fabrication
Labor:
20 hr EE to oversee the PC fabrication
40 hr ET to coordinate the PC fabrication
Material:
$11.500 (NRE 2.5k + 0.8 x 10 = 10.5K)

Loading of 9 RODs (There will be two phase of loading, one card and 9 cards)
Labor:
30 hr EE to oversee the loading
122 hr ET to coordinate the loading
Material:
$8300(2k NRE + 9 x 700 = $8300)

COST SUMMARY: (Project)	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	136	38	28	175	25	0	13	99	0.2	0.0

MANPOWER SUMMARY:	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
EDIA P	0	50	0	0	336	0	0	0	0	0	0	0	24.602
	0	50	0	0	336	0	0	0	0	0	0	0	24.602

MATERIAL SUMMARY:	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
MFG P	89	0	0	0	0	0.0	99.048
MFG B/I	89	0	0	0	0	0.0	99.048
EDIA P	12	0	0	0	0	0.0	12.802
EDIA B/I	8	0	0	0	0	0.0	9.238
	198	0	0	0	0	0.0	220.136

ROD Cost and Schedule

Selected Cost Book Items

WBS Number: 1.1.3.6 **Description:** ROD Protype evaluated

Institution : **Contact:** R. Jared

The ROD prototype is tested and evaluated.

Details of Estimate: The ROD prototype is tested and evaluated. There are three distinct tests. The first test is of the SCT specific ROD. The second test is of the Pixel specific ROD. The third component of the testing is the user evaluation by the pixel and SVT communities. These tests are very important for they will form the basis of changes that will be incorporated in the production model ROD.

Test of the SCT specific ROD
Labor:
348 hr EE to test the SCT ROD and update the user manual
80 hr ET to provide lab support

Test of the pixel specific ROD
Labor:
174 hr EE to test the Pixel ROD(The labor is low because much of the card has been tested)
80 hr ET to provide lab support

User evaluation of the RODS
Labor:
174 hr EE to participate in the user evaluation.
80 hr ET to provide lab support
Material:
$6000 for travel to CERN (two trips)

COST SUMMARY: (Project)	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	83	23	28	106	76	0	7	0	0.5	0.0

MANPOWER SUMMARY:	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
EDIA P	0	696	0	0	240	0	0	0	0	0	0	0	75.727
	0	696	0	0	240	0	0	0	0	0	0	0	75.727

MATERIAL SUMMARY:	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
EDIA P	0	0	6	0	0	0.0	7.200
	0	0	6	0	0	0.0	7.200

ROD Cost and Schedule

Selected Cost Book Items

WBS Number: 1.1.3.7 **Description:** ROD Production Model

Institution : **Contact:** R. Jared

The design is updated and 3 production model cards are fabricated, debuged, evaluated by the user community . This is the system test for the ROD,

Details of Estimate: The design is updated and 3 production model cards are fabricated, debugged and evaluated by the user community . This is the system test for the ROD,
Preceding this activity 9 prototype RODs have been fabricated and evaluated by the user community. Changes that are needed will be incorporated into the ROD and 3 units will be fabricated for testing. The review at the end of this activity will give permission to start fabrication.

Updating of the ROD is to make changes to the PC board and the VHDL code.
Labor:
348 hr EE to update the VHDL code and supervise the drafting effort
174 hr ET for drafting effort.

Fabrication and debugging of the production model ROD
Labor:
40 hr EE for supervision of the fabrication effort.
134 hr EE for debugging of the cards.
80 hr of ET for lab support and debugging of the cards.
80 hr of ET for purchasing of parts and coordinating fabrication.

Material:
$5000 for fabrication of the PC boards (2.5k NRE + 3x900 = $5000)
$14,799 for parts (4933 production parts x 1.5 small volume factor) x 3cards =$14,799)
$ 3,500 for loading of card (2k NRE = 3 x 500 = $3,500)

User evaluation/ system test
Labor:
348 hr EE to participate in the user test, and write a report.
80 hr of ET for lab support

Material:
$3000 for a trip to CERN

COST SUMMARY: (Project)	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	134	29	22	163	105	0	30	0	0.8	0.0

MANPOWER SUMMARY:	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
EDIA P	0	906	0	0	414	0	0	0	0	0	0	0	104.682
	0	906	0	0	414	0	0	0	0	0	0	0	104.682

WBS Number: 1.1.3.8 **Description:** ROD Fabrication

Institution : **Contact:** R. Jared

This item contains the material and labor needed to fabricate the ROD. This production is in two phases. The early production is to provide cards for early testing of modules.

Details of Estimate: This item contains the material and labor needed to fabricate the ROD. This production is in two phases. The early production is to provide cards for testing . The main production is to provide the ROD for ATLAS. Boards are tested at UW.
The cost of purchasing the 16 crates (8 ea. SCT and 8 ea. Pixel) to house the RODs is contained in this item.
A detailed implementation model of the ROD card has been completed to provide a basis for the cost estimate.

ROD Fabrication is for a total of 90+10 SCT RODs and 110+15 pixel RODs.

There has been significant simulation of ROD with an event generator and C code model of the ROD and front end modules. This study was used to define the number of RODs for several layers in the SCT and pixels detectors. The study defined the number of ROD for each part of the detector and the processing power needed in the formatter FPGA. The error bar the result is very small (a few percent). The ROD numerology is listed below:

SCT barrel: 2112 modules with 48 modules per ROD
44+5 RODs
each with 8 400 series FPGAs for formatting

SCT forward: 2 * 988 modules with <= 48 modules per ROD
46+5 RODS
NO patch panel has been assumed. With a patch
panel there are 42+5 RODs.

SCT ROD Total 90+10(They all have the same parts)
100 RODs

Pixel barrel: 1274 modules with 26 modules per ROD
49+5 RODs

Pixel forward:
Disks 1, 2 and 3: 2 * 198 modules with 32 modules per ROD
13+3 RODs

Disks 4 and 5: 2 * 108 modules with 24 modules per ROD
9+3 RODs

B-layer: 234 modules with 6 modules per ROD
39+4 RODs

Pixel ROD Total 125 (They have different numbers and sizes of FPGAs loader)

ATLAS ROD ELECTRONICS
COST ESTIMATE

K. Dao, D. Fasching, R.C. Jared, K. Marks, M. Nagel

MATERIALS

Common parts on all ROD boards:

ITEM#	PART DESCRIPTION	QTY / BOARD	UNIT COST	COST / BOARD
1	XCV200-5FG456C: Event Fragment Bulider	1	150.00	150.00
2	XCV200-5FG456C: Router	1	150.00	150.00
3	XCV400-5FG676C: ROD Controller	1	328.00	328.00
4	XCV150-5FG256C: Configuration & Diagnostic Control	1	115.00	115.00
5	XC1801PC20C: Programmable ROM	2	6.00	12.00
6	AM29LV040B: 512x8 Flash RAM	3	6.00	18.00
7	CY7C4265V: Synchronous FiFo 16kx18 (EFB)	4	38.00	228.00
8	CY7C960-ASC: VME Interface	1	37.00	37.00
9	CY7C964-ASC: Vme Interface	4	15.00	60.00
10	TMS320C6201GJL: Master DSP	1	109.00	109.00
11	TMS320C6701GJC: Slave DSP	2	169.00	338.00
12	Epson-SG-636: High Frequency Crystal Oscillator	3	4.00	12.00
13	MT2LSDT432U-10: SDRAM module 4Mx32	3	45.00	135.00
14	MAX811MEUS: Supervisory Circuit	1	1.60	1.60
15	0.1 uf CKO5	300	0.02	6.00
16	0.01 uf CKO5	20	0.01	0.20
17	100 uf TANT	20	1.00	20.00
18	MPC974FA: Motorola PLL Clock Driver	3	17.00	51.00
19	Harting 02-01-160-2101: 160 pin DIN Connector	3	16.64	49.92
20	IDT71V632: SRAM Diagnostic Memory 64Kx32	8	5.30	42.40
21	20 pin PLCC sockets	2	2.00	4.00
22	74FCT163245CPV	4	1.33	5.32
23	74FCT163374CPV	42	0.80	33.60
24	Fuses: 1.8V, 3.3V, & 5V	3	0.90	2.70
25	DC/DC or regulator: (48V to 1.8V)	1	10.00	10.00
26	Test headers- 16pin gold, Sullins	21	1.00	21.00
27	Test points- for GND	20	0.31	6.20
28	Hex Dip Switch	2	2.00	4.00
29	Resistors: network	6	0.11	0.66
30	Resistors: discrete	30	0.02	0.60
31	LEDs- Lite On	20	0.21	4.20
32	LED-light pipe	20	0.50	10.00
33	LEDs- Dialight	20	2.00	40.00
34	Reset Switches	1	1.00	1.00
35	40 MHz crystal oscillator	1	5.00	5.00
36	Socket for 40 MHz oscillato	1	0.33	0.33
			Total:	$ 2,006.40

SCT Boards: QTY=90
Board specific parts:

ITEM#	PART DESCRIPTION	QTY / BOARD	UNIT COST	COST / BOARD
1	XCV400-5FG676C- Formatter	8	328.00	2,624.00
2	CY7C4425-15AC- Dynamic Mask FiFo	8	15.00	120.00
			Total	2744.00

Pixel Board Type1: QTY=49 (Barrel)
Board specific parts:

ITEM#	PART DESCRIPTION	QTY / BOARD	UNIT COST	COST / BOARD
1	XCV150-5FG676C- Formatter	7	115.00	805.00
2	CY7C4425-15AC- Dynamic Mask FiFo	7	15.00	105.00
			Total	$ 910.00

Pixel Board Type2: QTY=13 (Forward discs 1,2 and 3)

Board specific parts:

ITEM#	PART DESCRIPTION	QTY / BOARD	UNIT COST	COST / BOARD
1¸	XCV150-5FG676C- Formatter	8	115.00	920.00
2¸	CY7C4425-15AC- Dynamic Mask FiFo	8	15.00	120.00
			Total	$ 1,040.00

Pixel Board Type3: QTY=9 (Forward discs 4)
Board specific parts:

ITEM#	PART DESCRIPTION	QTY / BOARD	UNIT COST	COST / BOARD
1	XCV150-5FG676C- Formatter	6	115.00	690.00
2	CY7C4425-15AC- Dynamic Mask FiFo	6	15.00	90.00
				Total:¸ $ 780.00

Pixel Board Type4: QTY=39 (B layer)
Board specific parts:

ITEM#	PART DESCRIPTION	QTY / BOARD	UNIT COST	COST / BOARD
1	XCV150-5FG676C- Formatte	2	115.00	230.00
2	CY7C4425-15AC- Dynamic Mask FiFo	2¸	15.00	30.00
				Total:¸ $ 260.00

Note: all parts have been obatined from vendors (web cost, phone quoat or formal quoat).

Miscellaneous notes on part selection:

1. Xilinx packages FG256, FG456, FG676 are layout compatible (i.e. we can load any of these items on the board footprint)

2. For the formatter FPGAs, the virtexE parts would provide better internal memory structure. However, availablitiy is uncertain.

3. If available, the TMS320C6711GFN would be ¼ of the cost for the SLAVE DSP, and enhanced DMA.

4. If available, the TMS320C6202GJL would be preferred for the master DSP because it provides more program memory and wider host port (i.e. 32 bits).

FABRICATION
PC Board: 12 layer, 9Ux400mm
PC fabrication $525 each (engineering judment)
Front pannel $75 each (engineering judment)

BOARD LOADING

FGA 12 ea.	12 x 676 pins x $.015/pin	= 122
IC 130 ea.	130 x 70 pins x $0.01/pin	= 91
Res/cap 360 ea.	360 x 0.05	= 18
Miscelanious		=20¸ (engineering judment)
		Total = $251/board

The multipying factors were obtained from a phone converstaion with a board loader.

BOARD COST:
Commom parts

Common parts	2006
PC board and front pannel	600
Board Loading	215
Total commmon parts	2857

SCT RODs 90+10 ea.

Total common parts	2857
Specific parts	2744
Total board cost	5601
Total cost 100 RODs	560k$

Pixel barrel RODs (49+5 ea.)

Total common parts	2857
Specific parts	910
Total board cost	3767
Total cost 54 RODs	203k$

Pixel froward discs 1, 2 and 3 (13+3 ea.)

Total common parts	2857
Specific parts	1040
Total board cost	3897
Total cost 16 RODs	62k$

Pixel froward Disc 4 (9+3 ea.)

Total common parts	2857
Specific parts	780
Total board cost	3637
Total cost 12 RODs	44k$

Pixel B-layer (39+4 ea.)

Total common parts	2857
Specific parts	260
Total board cost	3117
Total cost 43 RODs	134k$

Total CostSCT RODs 100 ea.		560k$
Pixel barrel RODs (54 ea.)	203k$	
Pixel froward discs 1, 2 and 3 (16 ea.)	62k$	
Pixel froward Disc 4 (12 ea.)	44k$	
Pixel B-layer (43 ea.)	134k$	
Total pixel Cost		443k$
Total Cost All RODS		1003k$

BOARD TESTING
Estimate 4hrs/board (engineering judment)

COST SUMMARY: (Project)	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	1459	350	24	1809	0	160	4	1295	1.3	0.0

MANPOWER SUMMARY:	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
MFG P	0	944	0	0	1104	174	0	0	0	0	0	0	159.967
MFG B/I	0	1	0	0	0	0	0	0	0	0	0	0	0.088
EDIA P	0	41	0	0	40	0	0	0	0	0	0	0	0.088
	0	986	0	0	1144	174	0	0	0	0	0	0	160.143

MATERIAL SUMMARY:	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
MFG P	84	0	0	954	0	192.0	1295.417
EDIA P	0	0	3	0	0	0.0	3.601
	84	0	3	954	0	192.0	1299.018

WBS Number: 1.1.3.8.1 **Description:** ROD 5 % Production

Institution : **Contact:** R. Jared

This item contains the material and labor to fabricate 5% of the RODs

Details of Estimate: This item contains the material and labor to fabricate 5% of the RODs.

Material:
The cost per board is contained in 1.1.3.8

SCT RODs 5 ea. for $28,005
Pixel Barrel RODs 2 ea. for $7,534
Pixel Forward Discs1,2 and 3 1 ea. for $3,897
Pixel Forward Disc 4 1 ea. for $3,637
Pixel B-layer 2 ea. for $6,234
Total $49,307

Fabrication Labor:
174 hr EE Corrdination effort and fabrication negotiations
174 hr ET Cordination effort

Debugging Labor:
174 hr EE to debug the 11 cards
174 hr ET to help debug and training for later debugging

COST SUMMARY: (Project)

Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
107	26	24	132	0	52	0	55	0.4	0.0

MANPOWER SUMMARY:

	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
MFG P	0	348	0	0	174	174	0	0	0	0	0	0	51.570
EDIA P	0	1	0	0	0	0	0	0	0	0	0	0	0.088
	0	349	0	0	174	174	0	0	0	0	0	0	51.658

MATERIAL SUMMARY:

	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
MFG P	49	0	0	0	0	0.0	54.879
	49	0	0	0	0	0.0	54.879

WBS Number: 1.1.3.8.2 **Description:** ROD 45 % Production

Institution : **Contact:** R. Jared

This item contains the material and labor to fabricate 5% of the RODs

Details of Estimate: This item contains the material and labor to fabricate 5% of the RODs.

Material:
The cost per board is contained in 1.1.3.8

SCT RODs, 40ea.	for	$224,040
Pixel Barrel RODs, 22ea.	for	$82,874
Pixel Forward Discs1,2 and, 3, 5 ea.	for	$19,485
Pixel Forward Disc 4, 3ea.	for	$10,911
Pixel B-layer, 17 ea.	fro	$52,989
Total		$390,299

Fabrication Labor:
44 hr EE Corrdination effort
87 hr ET Cordination effort

Debugging Labor:
254 hr EE to debug the 87 cards
348 hr ET to debug cards 4 hr x 87 = 348 hr

COST SUMMARY: (Project)

Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
465	112	24	577	0	52	0	413	0.4	0.0

MANPOWER SUMMARY:

	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
MFG P	0	298	0	0	435	0	0	0	0	0	0	0	52.395
	0	298	0	0	435	0	0	0	0	0	0	0	52.395

MATERIAL SUMMARY:

	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
MFG P	0	0	0	390	0	0.0	412.936
	0	0	0	390	0	0.0	412.936

WBS Number: 1.1.3.8.3 **Description:** ROD 50% Production

Institution : **Contact:** R. Jared

This item contains the material and labor needed to fabricate the late 50% production of the ROD.

Details of Estimate: his item contains the material and labor to fabricate 50% of the RODs.

Material:
The cost per board is contained in 1.1.3.8

SCT RODs, 55ea. for $308,055
Pixel Barrel RODs, 30ea. for $113,010
Pixel Forward Discs1,2 and, 3, 10 ea. for $38,970
Pixel Forward Disc 4, 8ea. for $29,096
Pixel B-layer, 24 ea. fro $74,808
Total $563,939

Fabrication Labor:
44 hr EE Corrdination effort
87 hr ET Cordination effort

Debugging Labor:
254 hr EE to debug the 102 cards
408 hr ET to debug cards 4 hr x102 = 408 hr

COST SUMMARY: (Project)	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	695	167	24	862	0	56	4	636	0.5	0.0

MANPOWER SUMMARY:	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
MFG P	0	298	0	0	495	0	0	0	0	0	0	0	56.002
MFG B/I	0	1	0	0	0	0	0	0	0	0	0	0	0.088
	0	299	0	0	495	0	0	0	0	0	0	0	56.090

MATERIAL SUMMARY:	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
MFG P	35	0	0	564	0	0.0	635.602
EDIA P	0	0	3	0	0	0.0	3.601
	35	0	3	564	0	0.0	639.203

WBS Number: 1.1.3.8.4 **Description:** Purchase ROD Crates

Institution : **Contact:** R. Jared

All costs to purchase the ROD crates are contained in this item.

Details of Estimate: The ROD crates (16 ea.) are purchased in two phases FY 01 (8ea.) and FY 02 (8 ea.). The phased purchasing is to match the needs of housing the production RODs.

Material
192k$ (16x12k$ ea. = 192k$) The 12k$ cost per crate was obtained by Roy Wastie from Viener and is consistent with the cost of crates for STAR.

Labor
40 hr ET to order and test crates.
40 hr EE to arrange for the purchasing.

COST SUMMARY: (Project)

Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
192	46	24	238	0	0	0	192	0.0	0.0

MATERIAL SUMMARY:

	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
MFG P	0	0	0	0	0	192.0	192.000
	0	0	0	0	0	192.0	192.000

CONTINGENCY FACTORS:

Risk				*Weight*			
Technical	Cost	Schedule	Design	Technical	Cost	Schedule	Cont %
4	4	4	8	2	1	1	24

WBS Number: 1.1.3.9.1 **Description:** ROD Installation and Repair

Institution : U. of Wisconsin, Madison **Contact:** R. Jared

This item contains the labor and material to install the RODs and to make repairs.

Details of Estimate: This item contains the labor and material to install the RODs. The labor costs are to cover the repair of defective cards and installation support at CERN. The duration of this activity is over 1.5 years. Technical labor will be used to train and guide physicists doing much of the installation..
Technical personnel are required for board repair. We estimate that about 10% of the boards will require repar, and that about 3 mandays per board will be required for each repair.

Travel is the cost associated with trips to CERN to find problens
5% one trip 3k, FY01
45% one trip 3k, FY01
50% three trip 3k, FY02, FY03 and FY04

Labor is for repair of cards and installation at CERN
240 hr ET for repair FY 01
240 hr ET for repair FY 02
240 hr ET for repair FY 03
240 hr ET for repair FY 04
296 hr EE for installation/repair FY 01
296 hr EE for installation/repair FY 02
296 hr EE for installation/repair FY 03
296 hr EE for installation/repair FY 04

COST SUMMARY: (Project)

Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
181	43	24	224	163	0	18	0	1.2	0.0

MANPOWER SUMMARY:

	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
EDIA P	0	1193	0	0	960	0	0	0	0	0	0	0	162.783
	0	1193	0	0	960	0	0	0	0	0	0	0	162.782

MATERIAL SUMMARY:

	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
EDIA P	0	0	15	0	0	0.0	18.001
	0	0	15	0	0	0.0	18.001

CONTINGENCY FACTORS:

Risk				*Weight*			
Technical	Cost	Schedule	Design	Technical	Cost	Schedule	Cont %
4	4	4	8	2	1	1	24

WBS Number: 1.1.3.9.2 **Description:** ROD shipping

Institution : U. of Wisconsin, Madison **Contact:** R. Jared

This item contains the material and effort needed to ship the RODs to CERN.

Details of Estimate: This item contains the material and effort needed to ship the RODs to CERN and elsewhere. The ROD cards are shipped to various institution around the world and CERN. The Institutional shippments are for testing of modules. These cards will later be shipped to CERN by the institutes. The shipment is for 24 boxes that are 2x2x2 feet and weigh about 50 pounds each. There will be 30 md of physics labor to arrange for the shipment from the institutions to CERN.

Material 24 crates x $250ea. = 6k$

Labor 20 days for arrangement and packaging.
100hr ET FY01
60 hr ET FY 02

COST SUMMARY: (Project)

Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
16	4	24	20	10	0	7	0	0.1	0.0

MANPOWER SUMMARY:

	S.W. Prof (hrs)	EE (hrs)	ME (hrs)	Design (hrs)	ET (hrs)	MT (hrs)	Admin. Super. (hrs)	Other Admin. (hrs)	Contract Labor (hrs)	Shops (hrs)	Tech. Serv. (hrs)	Student (hrs)	Total w/ overhead (k$)
EDIA P	0	0	0	0	160	0	0	0	0	0	0	0	9.618
	0	0	0	0	160	0	0	0	0	0	0	0	9.618

MATERIAL SUMMARY:

	Pur. Mat. (k$)	Stores (k$)	Travel (k$)	Low Level (k$)	R + D (k$)	High Level (k$)	Total w/ overhead (k$)
EDIA P	6	0	0	0	0	0.0	6.678
	6	0	0	0	0	0.0	6.678

CONTINGENCY FACTORS:

Risk				*Weight*			
Technical	Cost	Schedule	Design	Technical	Cost	Schedule	Cont %
4	4	4	8	2	1	1	24

ROD Cost and Schedule

Contingency

U.S. ATLAS E.T.C.
WBS Contingency Summary

Funding Source: All **Funding Type:** Project 12/9/99 1:45:14 AM

Institutions: All

WBS Number	Description	Institution	Risk Tech	Risk Cost	Risk Sched	Risk Design	Weight Tech	Weight Cost	Weight Sched	Cont %	Base Cost (k$)	Basis of Estimate
1.1.3	RODs									24	2629	
1.1.3.1	Test Beam Support									0	0	
1.1.3.1.1	Strip Test Beam Support									0	0	
1.1.3.1.1.1	Strip TBS UCI	U. of California, Irvine	0	0	0	0	0	0	0	0	0	Engineering judge
1.1.3.1.1.2	Strip TBS UW	U. of Wisconsin, Madison	0	0	0	0	0	0	0	0	0	Engineering judge
1.1.3.1.2	Pixel Test Beam Support									0	0	
1.1.3.1.2.1	Pixel TBS UCI	U. of California, Irvine	0	0	0	0	0	0	0	0	0	Engineering judge
1.1.3.1.2.2	Pixel TBS UW	U. of Wisconsin, Madison	0	0	0	0	0	0	0	0	0	Engineering judge
1.1.3.2	ROD System Design									0	3	
1.1.3.2.1	ROD Requirements									0	3	
1.1.3.2.1.1	Requirements UCI	U. of California, Irvine	0	0	0	0	0	0	0	0	3	Engineering judge
1.1.3.2.1.2	Requirements UW	U. of Wisconsin, Madison	0	0	0	0	0	0	0	0	0	Engineering judge
1.1.3.2.2	ROD Essential Model									0	0	
1.1.3.2.2.1	Essential Model UCI	U. of California, Irvine	0	0	0	0	0	0	0	0	0	Engineering judge

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ROD Cost and Schedule Contingency

WBS Number	Description	Institution	Risk Tech	Risk Cost	Risk Sched	Risk Design	Weight Tech	Weight Cost	Weight Sched	Cont %	Base Cost (k$)	Basis of Estimate
1.1.3.6.1	SCT prototype testing	U. of Wisconsin, Madison	4	4	8	8	2	1	1	28	35	
1.1.3.6.2	Pixel proto type testing	U. of Wisconsin, Madison	4	4	8	8	2	1	1	28	20	
1.1.3.6.3	User evaluation of ROD	U. of Wisconsin, Madison	4	4	8	8	2	1	1	28	27	
1.1.3.7	**ROD Production Model**									22	134	
1.1.3.7.1	Updating of ROD to Producti	U. of Wisconsin, Madison	4	3	4	8	2	1	1	23	44	
1.1.3.7.2	Fabrication of production Mo	U. of Wisconsin, Madison	4	3	4	4	2	1	1	19	51	
1.1.3.7.3	User evaluion of production	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	39	
1.1.3.8	**ROD Fabrication**									24	1419	
1.1.3.8.1	ROD 5 % Production									24	104	
1.1.3.8.1.1	ROD 5% Production Fabric	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	79	Engineering judge
1.1.3.8.1.2	ROD 5% Production Debug	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	26	Engineering judge
1.1.3.8.2	ROD 45 % Production									24	450	
1.1.3.8.2.1	ROD 45% Production Fabri	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	407	Engineering judge
1.1.3.8.2.2	ROD 45% Production Debu	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	43	Engineering judge
1.1.3.8.3	ROD 50% Production									24	673	
1.1.3.8.3.1	ROD 50% Production Farbi	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	583	Engineering judge
1.1.3.8.3.2	ROD 50% Production Debu	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	89	Engineering judge
1.1.3.8.4	Purchase ROD Crates		4	4	4	8	2	1	1	24	192	
1.1.3.9	**ROD Installation, Repair and S**	**U. of Wisconsin, Madison**								24	197	
1.1.3.9.1	ROD Installation and Repair	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	181	
1.1.3.9.2	ROD shipping	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	16	

ROD Cost and Schedule

Selected Cost Book Items

WBS Number	Description	Institution	Risk: Tech	Risk: Cost	Risk: Sched	Risk: Design	Weight: Tech	Weight: Cost	Weight: Sched	Cont %	Base Cost (k$)	Basis of Estimate
1.1.3.6.1	SCT prototype testing	U. of Wisconsin, Madison	4	4	8	8	2	1	1	28	35	
1.1.3.6.2	Pixel proto type testing	U. of Wisconsin, Madison	4	4	8	8	2	1	1	28	20	
1.1.3.6.3	User evaluation of ROD	U. of Wisconsin, Madison	4	4	8	8	2	1	1	28	27	
1.1.3.7	ROD Production Model									22	134	
1.1.3.7.1	Updating of ROD to Producti	U. of Wisconsin, Madison	4	3	4	8	2	1	1	23	44	
1.1.3.7.2	Fabrication of production Mo	U. of Wisconsin, Madison	4	3	4	4	2	1	1	19	51	
1.1.3.7.3	User evaluion of production	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	39	
1.1.3.8	ROD Fabrication									24	1419	
1.1.3.8.1	ROD 5 % Production									24	104	
1.1.3.8.1.1	ROD 5% Production Fabric	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	79	Engineering judge
1.1.3.8.1.2	ROD 5% Production Debug	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	26	Engineering judge
1.1.3.8.2	ROD 45 % Production									24	450	
1.1.3.8.2.1	ROD 45% Production Fabri	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	407	Engineering judge
1.1.3.8.2.2	ROD 45% Production Debu	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	43	Engineering judge
1.1.3.8.3	ROD 50% Production									24	673	
1.1.3.8.3.1	ROD 50% Production Farbi	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	583	Engineering judge
1.1.3.8.3.2	ROD 50% Production Debu	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	89	Engineering judge
1.1.3.8.4	Purchase ROD Crates		4	4	4	8	2	1	1	24	192	
1.1.3.9	ROD Installation, Repair and S	U. of Wisconsin, Madison								24	197	
1.1.3.9.1	ROD Installation and Repair	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	181	
1.1.3.9.2	ROD shipping	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	16	

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ROD Cost and Schedule

Selected Cost Book Items

WBS Number	Description	Institution	Risk: Tech	Risk: Cost	Risk: Sched	Risk: Design	Weight: Tech	Weight: Cost	Weight: Sched	Cont %	Base Cost (k$)	Basis of Estimate
1.1.3.10	Project Management	U. of Wisconsin, Madison	4	4	4	8	2	1	1	24	92	

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