Proposal for a DAQ and Online Test Stand for the DIRC

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Abstract

To develop online and DAQ systems for the DIRC, a dedicated DAQ and online test stand is needed. In this note, we propose the construction of a test stand at LBL. The primary goals for the test stand will be to develop a DIRC readout system within the Babar framework, and to develop a DIRC calibration procedure. We list the resources needed, and discuss how we might obtain them. We discuss how this effort would relate to the development of the general Babar online, and to the development of online systems for the other sub-detectors. We also discuss how DIRC colleagues outside of the bay area could participate in this work.

1 Introduction

Functioning DIRC DAQ and online systems must be available in early 1998 both for the 3-sector testbeam at CERN, and to test sectors when they start arriving at SLAC. A good goal is to use realistic DAQ and online systems for these tests, in order to test and debug them as well.

To develop these systems, a realistic test environment is needed. To this end, we propose to setup a DIRC DAQ/online test stand at LBL. LBL is a logical place for this installation, as it already hosts a general Babar DAQ development lab (see section 2). The proposed DIRC test stand would share the lab space with the general DAQ setup, allowing a sharing of tools. Most importantly, the LBL test stand would provide us with access to the BaBar DAQ experts (Gerry Abrams, Steve Lewis, Joe White, and Chris Day), and their workers. In a reciprocal role, the DIRC test-bench will provide the general DAQ group with an example sub-system on which to experiment.

The main goals of the test stand will be development of DAQ and calibration software. These will require intimate knowledge of the performance and behavior of the DIRC and DAQ electronics, which can only be obtained through direct testing and experimentation. We foresee a long program where specific goals co-evolve with the DIRC electronics and the general BaBar DAQ system. Details of our proposed program are given in sections 4.1 and 4.2.

There are also important secondary goals of the DIRC test bench. One will be to provide an environment for testing the DIRC/SVT/IFR personality module. Another will be to help define the fast control system requirements. Successful DIRC readout software would also provide a model for other sub-systems.

The Babar DAQ group have shown enthusiasm and support for the idea of a DIRC test bench, and have offered to share human and other resources. In particular, it is hoped that some hardware necessary (most importantly a prototype ROM) might be provided by them. Other materials might be financed from the Babar R+D fund, or through DIRC discretionary funds.

Our plan is to start setting up the test stand early 1996. The initial task will be to learn about the readout controller, and to begin customizing the Babar online interface for our purposes. After the prototype DIRC front-end electronics boards, the prototype ROM, and the prototype personality modules first appear, we will begin DIRC specific tests. As described in section 3, we would upgrade the system piece at a time, as new electronics and general software appear.

2 Existing LBL DAQ Test Setup

A sophisticated DAQ test setup is already in operation at LBL. This setup was constructed by Chris Day and Bob Jacobsen, mainly to study dataflow and event building. The setup has also been used by Steve Lewis and Joe White to develop prototype online control software. A similar system has been setup at SLAC by the drift chamber group.

The existing setup has many aspects of the final BaBar DAQ. It consists of VME crate electronics with remote micro-processors connected to UNIX workstations. There are currently 3 SUN stations and 3 DEC ALPHA stations connected in various ways to Motorola processor VME controllers. As these are currently all in use for various projects, the DIRC group would have to provide its own UNIX station.

There are a total of three VME crates. Two of them are currently devoted to high-speed network development and benchmarking. Each of these has a Motorola M-VME167 CPU board (68040) as primary processor and a Motorola M-VME1600 CPU board (PPC603) as secondary processor. Also, each has an Interface 5211 FDDI/CDDI network adapter card and an Interface 5215 ATM network adapter card. All of the CPUs are running VxWorks 5.2 as their operating systems.

The remaining VME crate has two Motorola M-VME167 CPUs in it as well as a large memory module (MM6390), a multipurpose I/O register (CAEN V262) with NIM and ECL channels, and an interrupt generator board (RCB 8047 CORBO). The CPUs run VxWorks 5.2 as well as EPICS. Initialy, the DIRC test bench electronics could be housed in this crate. Ultimately, we need a DIRC front end crate.

In addition to the VME hardware, there is a CAMAC crate and a NIM bin, with assorted modules. These would be used to simulate the trigger and timing control in the initial phase of the test bench. Usual ancillary tools such as oscilloscopes and logic analyzers are also available.

Software licenses exist at LBL for AVS (a data visualization package) and Object-Store (an object-oriented database). These might be used as prototypes for the online event display and database.

3 DIRC Test Stand Setup

Our proposed test stand will reuse some of the components used at the CERN testbeam. To control the electronics, we propose to use the SUN workstation which ran the DAQ at the CERN testbeam. A replacement SUN station could be configured to run the same software, providing continuity for the 1996 beam tests.

Our initial readout system will be based in the SUN processor, and will use EPICS to connect to the VME crate. We will use the standard run-control environment that is being developed for Babar, which is based at least in part on the run-control used at the DIRC testbeam. The user interface for DIRC specific access will be mostly written in c and Tcl/Tk, as at the testbeam. for our initial tests, the time performance of the system will not be critical. As timing becomes more critical, we will have to push the readout software out of the unix processor and into the remote micro-processors (ROC cpu). Monitoring and data evaluation will continue to be performed in the UNIX station. To get realistic performance estimates, the SUN will eventually need to be replaced by a faster UNIX station (whatever is chosen by the online group for general DAQ).

Initialy, the electronics and software will be tested using both on-board and external pulsing. External pulsing will be done with a programmable signal generator. Having both internal and external pulsing will give us flexibility in the kinds of test we can perform, as well as allowing us to verify the performance of the internal pulsing.

Later phases of the readout tests will require a more realistic single photon signal. Realistic signals will also be required to develop and test the calibration software. To provide such signals, we propose to use a dark box with a bundle of 24 Hamamatsu tubes from the testbeam. To induce signals in the PMTs, we will use a fast (<1 nSec) blue LED. The LED would Initialy be pulsed through a fast pulsing circuit developed for the AMANDA experiment for calibrating their phototubes with LEDs. The LED will be triggered through the readout system, allowing full control over the pulse timing, rate, and amplitude. This setup will allow us to model both calibration readout (with a synchronous light flashing) and beam readout (with asynchronous light flashing and triggering).

The initial hardware needs are thus;

- SUN station (from CERN test)
- VME crate and readout (from LBL online lab)
- DAQ card prototype with personality module (ROM) (purchased from Babar R+D funds?)
- Prototype DIRC front-end board (DFB) (from Orsay)
- Pulser, signal generator, and 'NIM' logic (from LBL)
- basic ADC and TDC.

Intermediate tests will require in addition

$\geq$ 1 DIRC front-end crate (purchased from Babar R+D funds?)

$\geq$ 1 PDB card (from Ecole Polytechnique)

$\geq$ 1 DIRC crate controller (DCC) (from Ecole Polytechnique)

dark box (from LBL)

PMTs (from testbeam)

LED and pulsing circuit (from LBL)

2nd generation DFB prototype cards (From Orsay)

Fast control modules (FCDM, FCS) (??)

4 Tests

A series of tests must be carefully planned to develop the on-line software and test it with the DIRC electronics hardware. These elements are blended together to operate and obtain results from the detector.

We will start from very basic tests designed to familiarize us with the system's basic components and back-bone software developed in conjunction with the BaBar data-acquisition group. This software will be portable to other subddetectors.

4.1 Electronics Tests

The DIRC DAQ has a wide range of components which need to be integrated to make up the complete final system. It will be important to start early testing of the prototypes as well as the final components with a system perspective. A description of the electronics system components and their function is given in appendix A.

1. Basic Tests:
   The basic tests are shown in figure 1. The highlighted objects are the ones most under scrutiny.

   The first group of tests will start with a minimum of BaBar specific modules in order to concentrate on VxWorks and EPICS work environment. We will use a prototype ROM; DAQ board without Power PC, and Personality Module; and the prototype DIRC Front-end Board (DFB) which has a VME interface. This will allow us to "peek and poke" these modules' registers via the VME interface and verify their functionality. In next step we will connect the Personality Module individual clock control and data I/O to the standard DFB I/O (this bypasses the GLINKs, fiber-optics and DIRC Crate Controller (DCC)). With this set-up we will check out the protocol transmission and decoding in the DFB, and exercise the DFB electronics calibration.

   Then, we will connect our logic which simulates the trigger electronics and the fast logic, and with a signal generator we will inject digital impulses to the input of the TDC and verify the functionality of the DFB readout section.

2. GLINKs and DCC Tests:
   The proposed DCC tests are shown in figure 2. Once we are satisfied with the above mentioned tests we will introduce the fiber-optic CLINK and DLINK, the DCC, and the DIRC front-end crate with the Point-to-point Distribution Board (PDB). With this configuration we can run the same tests as we did in the preceding step to verify the functionality of the DCC. One of the most critical test with this set-up is to look at the stability of the 59.5MHz clock being sent to the DFB. This clock is extracted in the DCC from the data received over the CLINK from the Personality Module. The stability of this clock is crucial because the timing of the TDC is dependent upon it, there should not be any shift in frequency or in phase. At this point one may consider introducing analog measurements to verify the operation of the discriminator, ADC, TDC, and selective readout chain. The signal injected to the input will be coming from a signal generator so the calibration can be exercised. To complete tests with this set-up we may plug in the Power PC on the ROM and run the calibration locally.

3. DIRC Functional Tests:
   The proposed functional tests are shown in figure 3. The installation of a second DFB in the Front-end crate will test thoroughly the DCC and PDB. The 59.5MHz clocks for the DFBs within one crate must be reasonably lined up in phase, there should not be any interaction between DFBs, and the Personality Module addressing of the VRAMs on the DAQ board will need to be verified. By that time a Fast Control Distribution Module should become available simplifying our custom logic which will need only to simulate the trigger. More realistic functional tests and calibration runs can be imagined and at last real signals from PMTs can be measured, We will use the Dark Box and LED pulser triggered from either the DCC, for calibration runs, or the pulse controller via VME to simulate physics events.

4. Architectural Tests:
   The architectural tests are shown in figure 4. These tests call for several Front-end crates populated with several DFBs each, and as many ROMs as crates. A more sophisticated trigger and Fast Control System (FCS) may be tested using this configuration. It will require many

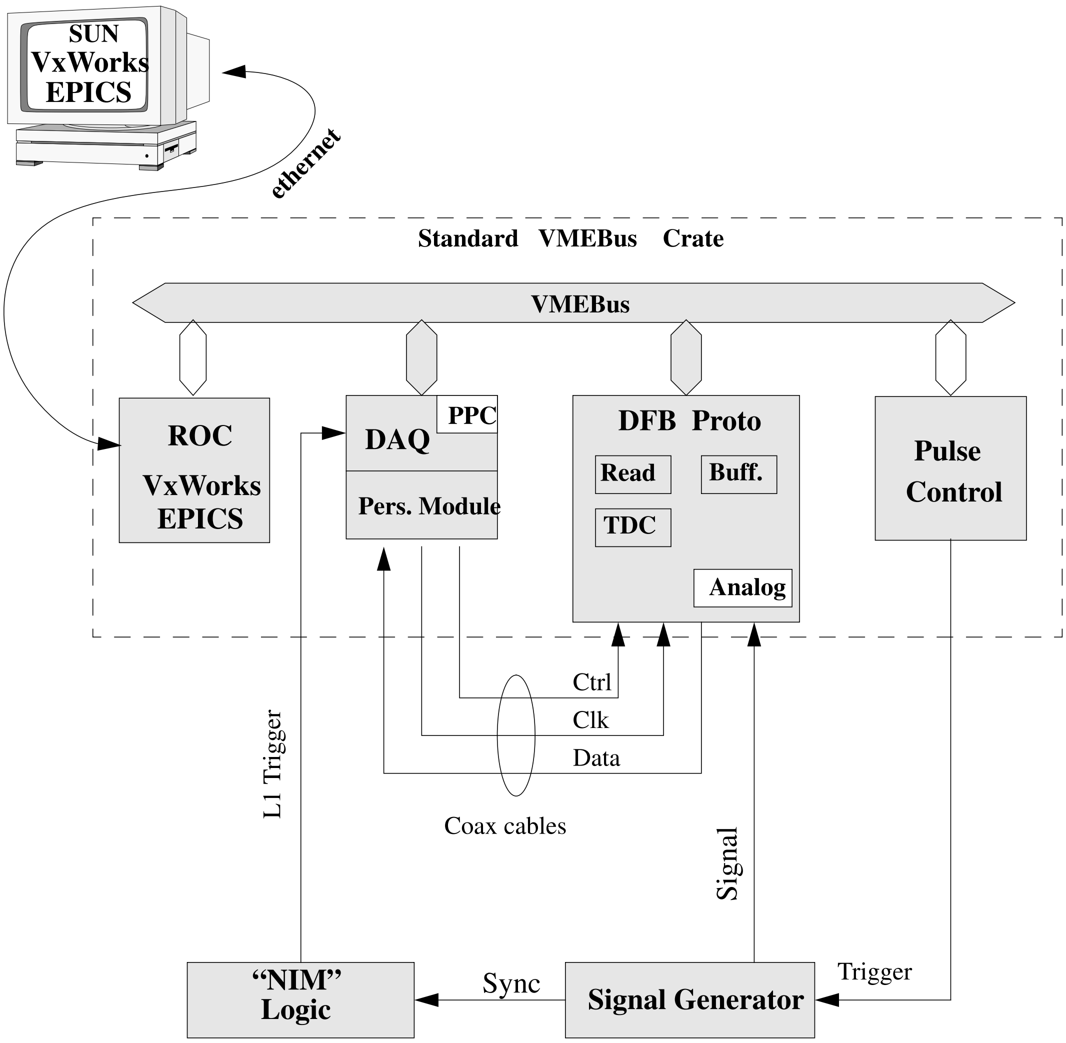


Fig. 1 DIRC Basic Tests

Figure 1:

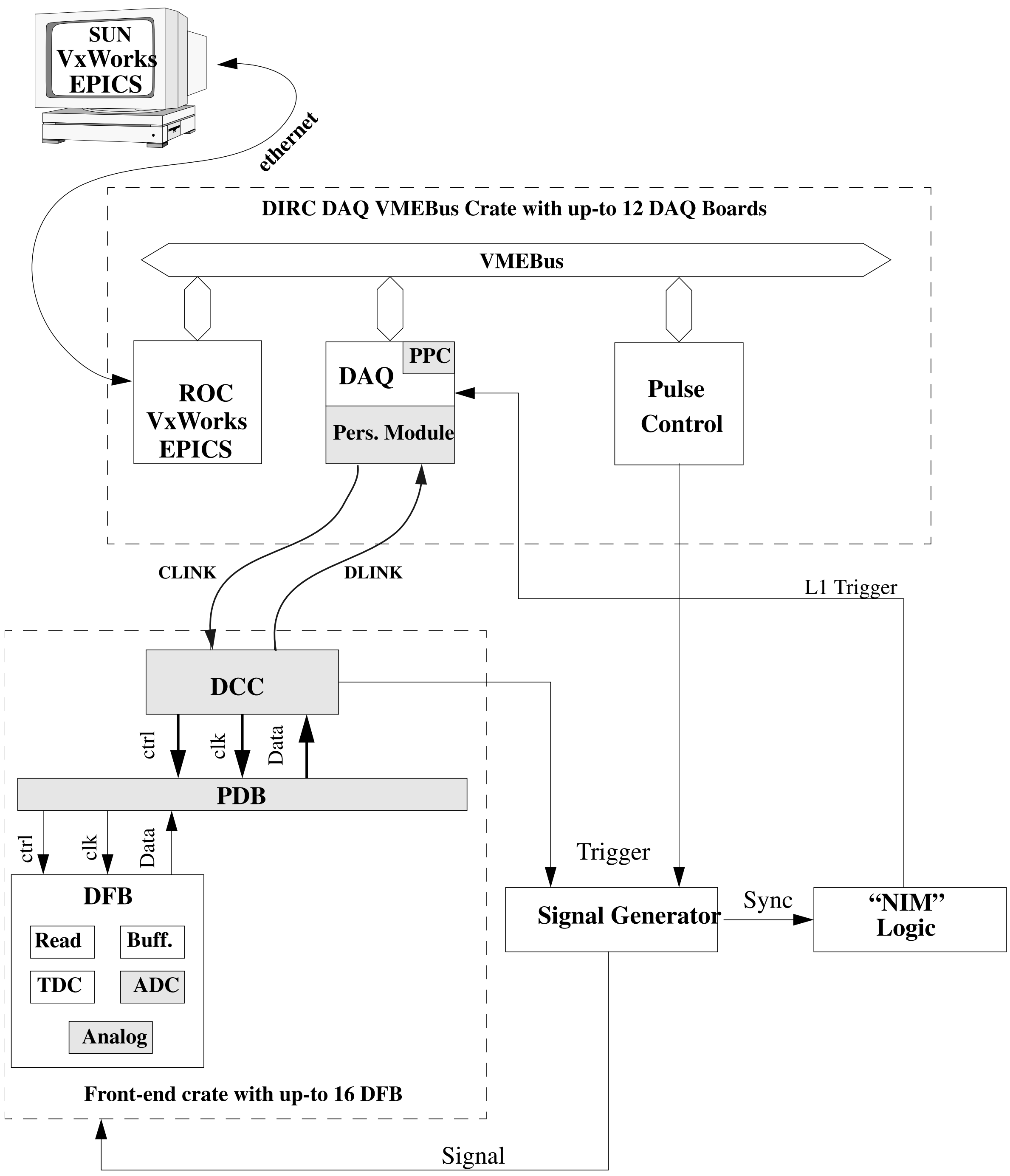


Fig. 2 DIRC GLINKs & DCC Tests

Figure 2:

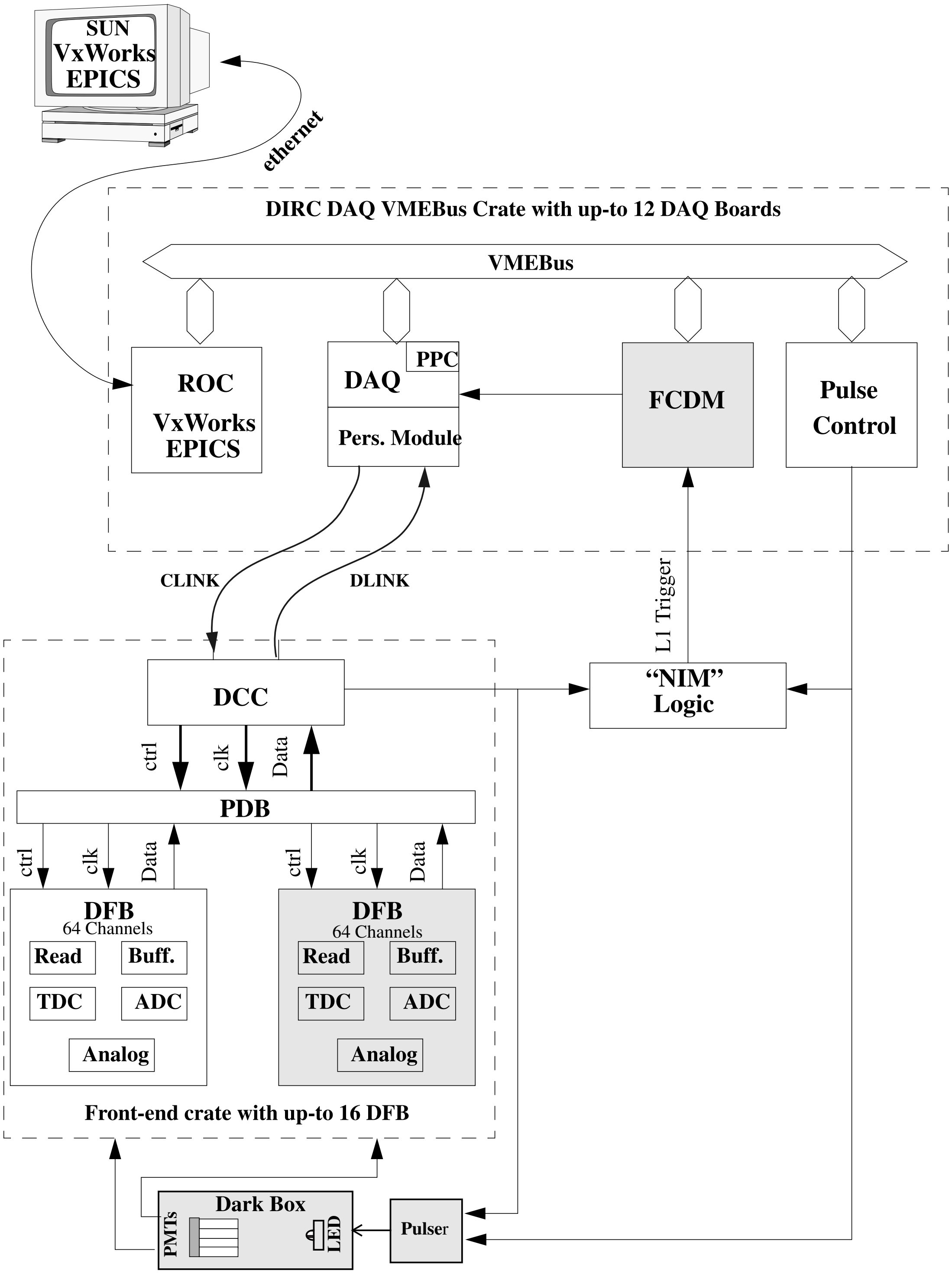


Fig. 3 DIRC Functional Test

Figure 3:

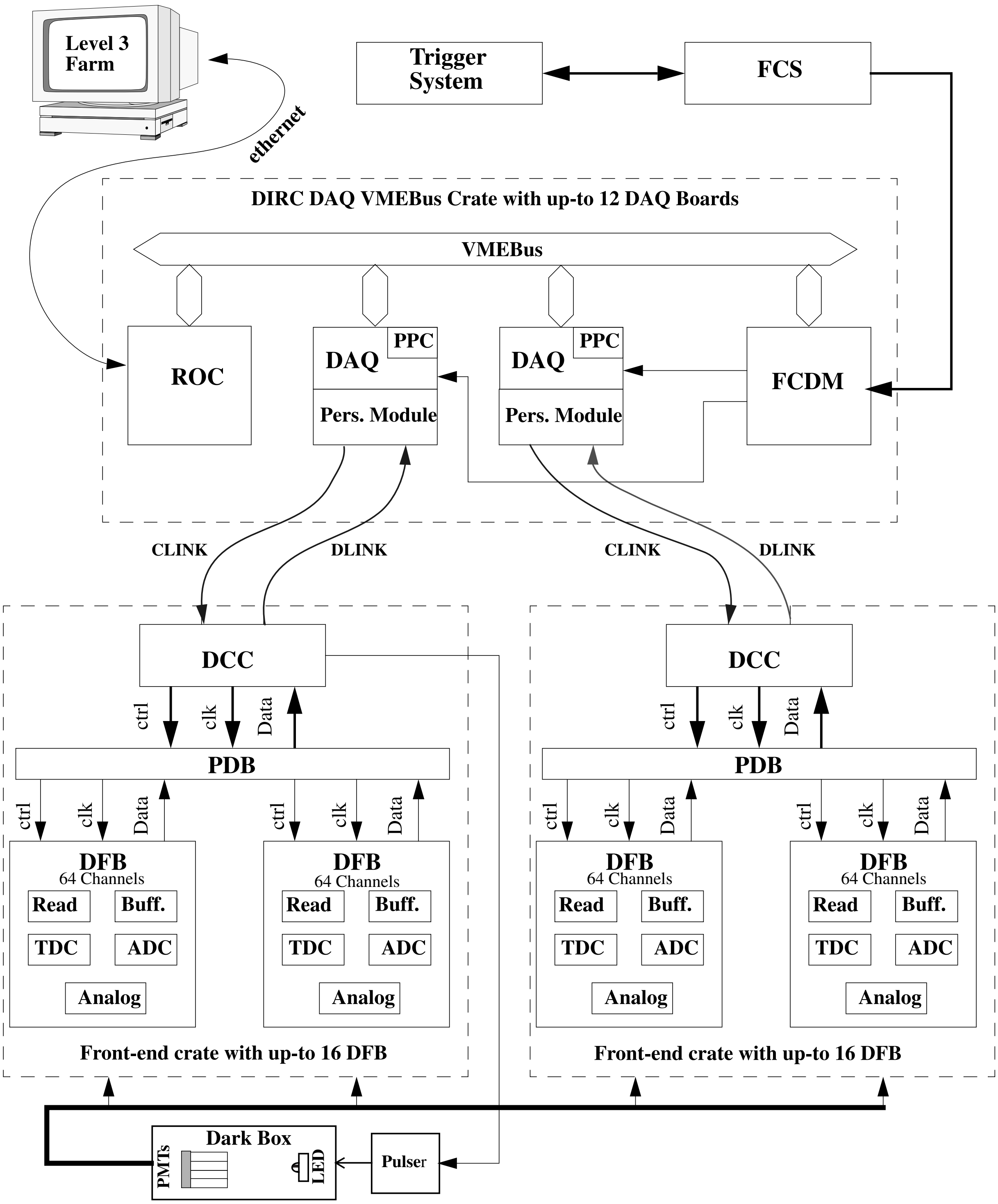


Fig. 4 DIRC Electronics Architecture

Figure 4:

experts from different groups at this stage to generate triggers and organize the data flow, this architecture will be implemented with the final production software and hardware.

4.2 Online Software Development

The DIRC online must integrate control and readout of the detector. Additionally, functions such as communication with the main Babar run control tasks, calibration, monitoring, and event display must all be supported. A schematic of how the online will be setup is given in figure 5. In this scheme, there are two main paths for data flow, *detector control* and *run control* (including calibration and monitoring). The goal of the LBL test stand will be to develop the run control path, as described below. Detector control for the DIRC is being developed elsewhere, and will be integrated with run control only at the highest, user-interface level.

Many aspects of the Babar online software environment have not yet been defined. The online test bench will therefore need to evolve with the common Babar online elements. Our approach will be to choose a likely candidate for crucial elements (such as a graphics packages for GUI, histogramming, and event display), and work with them until a Babar-wide decision is made.

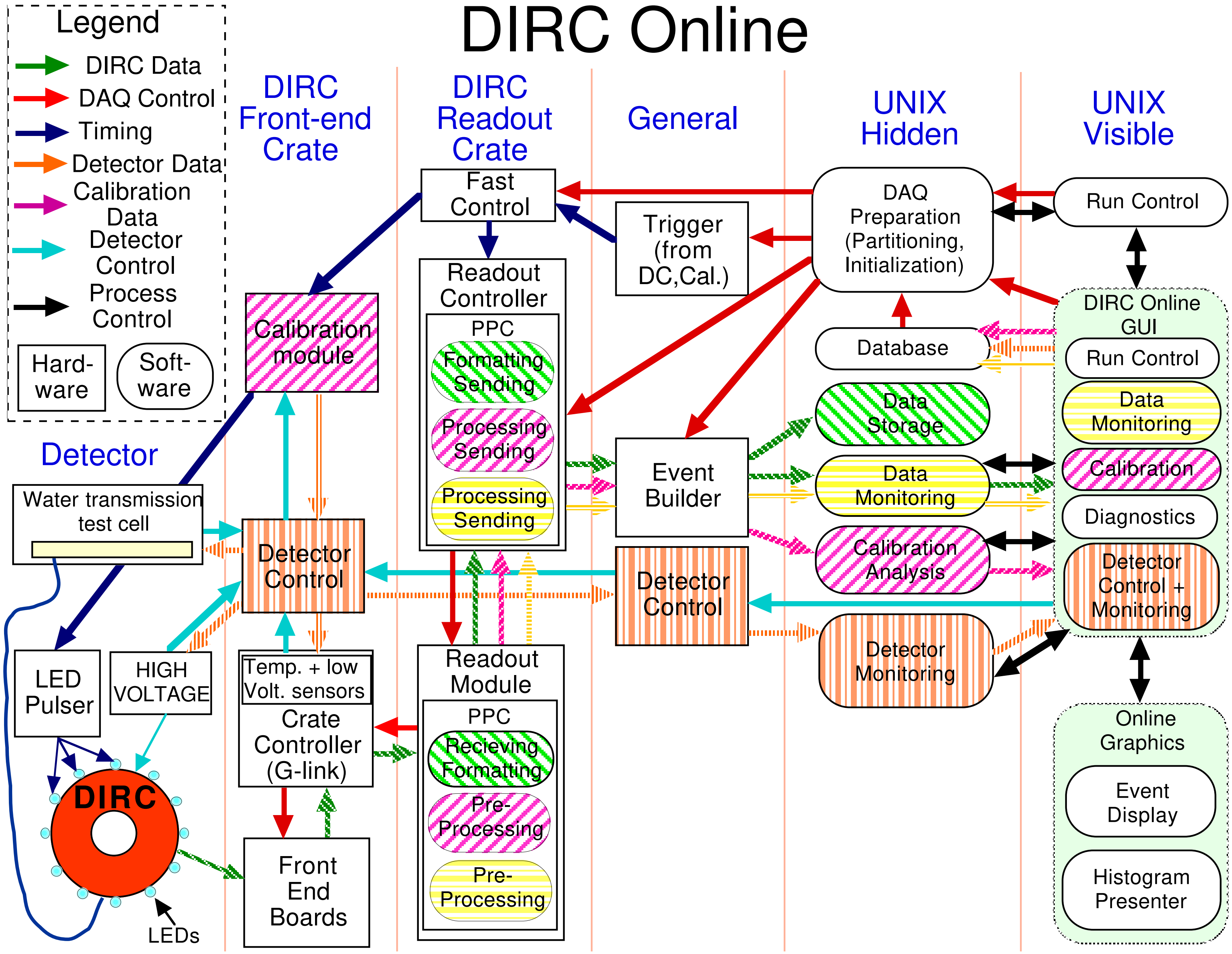
We perceive the online software development proceeding by stages. The stages are listed in rough chronological order below.

1. Diagnostic Access:
   The first need in the test bench will be to access individual elements of the hardware one channel at a time 'by hand'. This will most effectively be done inside the VxWorks environment, using the remote shell feature. Once the basic electronics problems have been solved, we will put together the simple tests which proved useful into a 'menu' of standard diagnostics, accessed through a graphical user interface (GUI) making use of the EPICS connections available in the etWish shell. This diagnostic menu will be perpetuated and added to throughout the life of the online, so as to provide experts with access to basic tests in case of hardware problems.

2. Electronics Calibration:
   Once we understand how to make the hardware function, we will proceed to develop algorithms for standard electronics calibrations. These will involve loops over channels, and loops over multiple calibration triggers. Software to provide higher-level user control of these will be introduced. Algorithms for extracting calibration information (T0, thresholds, etc.) will be developed. A choice will be made for a prototype histogram presenter, and that will be included to provide graphical evaluation of the calibration data. Once on-board electronics calibration is functioning in this way, we will develop an analogous system using external pulsing through a function generator.

3. Detector Signal Faking:
   To design more realistic signals for readout modeling and more complete calibration procedures, we will introduce a fake detector. The fake detector will consist of a few phototubes in a dark box, illuminated by an LED, as described above. In providing the DAQ with realistic signals, we will be able to refine the calibration procedures, and introduce new algorithms such as efficiency measurements and threshold setting on noisy tubes. By interpreting the calibration pulse as a L1 trigger, we will also be able to start developing readout algorithms. Additional user controls for the extra calibration and readout software will be developed. Prototypes of the online monitoring and event displays will be developed, operating the test stand in fake L1 trigger mode.

4. Microprocessor Utilization:
   Many DAQ tasks will need to be run in the front-end CPUs for reasons of efficiency. Calibration,



DIRC Online
Legend
DIRC Data
DAQ Control
Timing
Detector Data
Calibration Data
Detector Control
Process Control
Hard-ware
Soft-ware
DIRC Front-end Crate
DIRC Readout Crate
General
UNIX Hidden
UNIX Visible
Fast Control
Trigger (from DC,Cal.)
DAQ Preparation (Partitioning, Initialization)
Run Control
Calibration module
Readout Controller
PPC
Formatting Sending
Processing Sending
Processing Sending
Database
DIRC Online GUI
Run Control
Data Storage
Data Monitoring
Data Monitoring
Calibration
Event Builder
Diagnostics
Calibration Analysis
Detector Control + Monitoring
Detector
Water transmission test cell
Detector Control
Detector Control
Detector Monitoring
LED Pulser
HIGH VOLTAGE
Temp. + low Volt. sensors
Crate Controller (G-link)
Readout Module
PPC
Recieving Formatting
Pre-Processing
Pre-Processing
Online Graphics
Event Display
Histogram Presenter
DIRC
Front End Boards
LEDs

Figure 5:

which must run at $/sim$ 10KHz to minimize loss of luminosity, must pre-process data in the front-end CPUs in order to match the 2KHz online farm output rate. There is therefore a need to push code developed in the unix environment back into the micro-processors.

Testing code in the micros will be a main task of the online test stand. By having unix and micro-processor versions of the same code, we'll be able to verify the code and determine it's performance. All algorithms will be developed in standard C/C++, and so will be transportable to the micros without major re-writing. Additional controls to coordinate different micros performing different tasks will be developed in conjunction with the Babar online core. Tests and comparisons of different compilers will be possible in a 'real-world' environment, and we will begin addressing the issue of how to store and download binary executable files and data files to the micros.

5 Calibration Software

The calibration system structure for Babar is only vaguely defined. Furthermore, the DIRC group hasn't yet clearly defined the requirements of the calibration system. As the time available for a calibration run is very short ($\sim$ 1 minute), extensive code development and testing are necessary. The online test stand will allow us to test possible solutions, and to answer some of the open questions questions about calibration, namely;

1. Goals. What are realistic goals for dedicated calibration runs? Which of the necessary measurements must be done online in a dedicated calibration run, and which are best done by offline monitoring of collision data? Possible goals might be:
   - Detector 'live' tests:
     We need to know if the detector is still working after a shutdown or access. This must be done online.
   - Discriminator threshold setting:
     This must be done online.
   - Cross-talk determination:
     This must be done online.
   - TDC linearity and slope:
     This can best be measured online.
   - ADC pulse height/gain measurement:
     This needs to be done online, and repeated offline.
   - TDC/ADC slewing:
     This needs to be done online, and repeated offline.
   - Search for hot/dead channels:
     This needs to be done online, but might get refined offline.
   - Channel efficiency map:
     This can be measured crudely online, but will need to be refined offline.
   - T0:
     This can be measured crudely online, but will need to be refined offline.
   - Time resolution:
     This can be measured crudely online, but will need to be refined offline.
   - Bar attenuation:
     This is best measured offline.

- Alignment:
  This is best measured offline.
- Water transmission:
  This must be measured online, but should be done through the detector control system, not a dedicated calibration run.

2. Control:
   What users controls are needed for dedicated calibration runs that aren't already available through the general run control? What hardware path should be used for sending calibration control signals, run control or detector control?
3. Database:
   What data do we need to store for the DIRC, and in what format? This issue must be settled in conjunction with the DIRC offline.
4. Hardware:
   What physical apparatus is necessary for calibration? Do we need anything besides electronics pulsing and a uniform illumination the image plane with LEDs? Are the white plastic spheres adequate for image plane illumination? What would be the purpose of laser pulsing, and is the laser necessary?
5. Electronics:
   What control electronics is needed specifically for calibration? For LED pulsing, what are the requirements in terms of pulse height, pulse width, and pulse time adjustment? The calibration system of Prot2 suggests that a pulse width $\leq$ 5nSec is necessary to calibrate the TDCs, and adjustment of pulse height over 2 orders of magnitude is necessary to correctly adjust the light intensity. Adjustable pulse delays between 0 and 100nSec is necessary to measure TDC linearity and slope.

6 Collaboration outside the bay area

People outside the bay area may participate in the test stand in several ways. First, satellite installations could be prepared at remote sites with a subset of the hardware used at LBL. These sites would allow independent development work, or exploitation of the software developed at LBL for detector/electronics tests. Remote access to the LBL test bench will be possible for special tests. DIRC personnel interested in DAQ could arrange to visit LBL and work with the test stand after the spring of 1996. DAQ/online progress would be reported regularly through DIRC notes and presentations.

7 Conclusion

We have presented our proposal for constructing a DIRC DAQ/online test bench at LBL. This test bench would provide the environment necessary for the testing and development of the DIRC DAQ and calibration systems. The goal will be to have a working system in time for the 1998 CERN 3-sector tests. If funds are approved, the test bench construction would begin early in 1996. The test bench must be furnished with prototype DIRC and Babar DAQ electronics.

A DIRC DAQ Hardware Summary

The DIRC electronics must perform a number of tasks. All the tasks are controlled by the on-line software and the fast control system, and the final product, the raw data, is in turn delivered to the on-line software before being sent to the level three trigger for further analysis.

Starting with the PMT and going towards the physics analysis the following tasks are performed:

1. Detection of a single photoelectrons performed by the PMT.
2. Detection of the PMT signal and noise rejection by the analog electronics, which consists of a zero crossing discriminator and a sampling ADC.
3. Upon detection of a PMT signal a time stamp corresponding to the signal arrival time is generated by a TDC. The amplitude of the 1/64 of the signals will be digitized by an ADC.
4. Since the BaBar event decision takes up to 11.5 microseconds and the PEP II beam crossing frequency is 4.2 nanoseconds, the time stamp and the amplitude value need to be stored in FIFOs. The present system has a digital FIFO to store the time stamp and an analog FIFO to store the analog value
5. The electronics continuously examine the content of the TDC FIFO to determine if the data stored lies within the maximum trigger latency (11.5us). When the data stored within the FIFOs was captured prior to the possible trigger it is discarded.
6. Upon reception of a Level 1 Accept trigger signal the zero suppressed data associated with this particular trigger is stored in an event buffer. The Level 1 accept trigger signal has, as mentioned above, up to 11.5us latency over the event itself. 11.5us is the maximum time taken to make the decision that there was indeed a possible physics event. The minimum time to make that decision is (so far) 10.5us. Therefore, the electronics stores in the event buffer a time slice of data worth 1us spanning from 10.5us to 11.5us. Since another Level 1 accept trigger may be received before the event buffer is read out,there are several event buffers.
7. The data is read out serially from the event buffer and sent to a multiplexer which accepts data from all channels within a sector and send them to the DAQ over a single fiber optic.
8. The serial data from all channels within a sector is received by the DAQ electronics, it is demultiplexed so that the data from each channel or group of channels can be written into a specific memory location of the ROM.
9. Once the data is stored in memory within the DAQ subsystem it can be formatted and sent to the level 3 trigger via a network.
10. To control the data acceptance and the data flow the software and hardware are very tightly coupled. Based on calibration runs thresholds need to be adjusted, channels disabled and so forth. The entire BaBar detector must be synchronized and time critical signals need to be distributed. The system needs to be monitored as well. All those functions are originated by the software and distributed via the ROM down to the front end electronics.

The Electronics Hardware for the DIRC is designed to be modular at the DIRC sector level. There are so-called on-detector electronics and off-detector electronics for each of the 12 sectors. The on-detector electronics performs tasks 2-8 described above and tasks 9 and 10 are performed by the off-detector electronics.

The on-detector electronics is housed in a chassis containing a maximum of 16 front-end cards and a "crate controller", the channel multiplexer. Each front- end card performs tasks 2-6 for 64 PMT channels. Therefore, as far as the data path is concerned, the front-end includes the analog electronics, TDC, FIFOs; analog and digital, digitizer, selective readout logic, and event buffers. The crate controller accepts the serialized data from 16 front-end cards and multiplexes them into one line going to the off-detector electronics.

The data arrive at the off-detector electronics on the personality module. There it is demultiplexed and formatted to be written into the ROM's video memory. The data stored in the video memory can then be examined by the local Power PC or directly transferred over the VME bus to a commercial processor.

Of course, all the actions described above are started by software calls and prompt signals originating from the BaBar fast control system. The DAQ has a single path to communicate with the front-end via a control link driven from the personality module. The personality module's hardware interprets signals from the fast control system and commands from the software and distribute a set of op-codes to the front-end cards via the front-end crate controller (multiplexer). The op-codes are decoded by the front-end cards to perform specific functions (see list of proposed protocol).

B DIRC Electronics Test Components

1. Analog chip.
   The prototype analog chip, a single channel zero crossing discriminator will be tested at LAL Orsay in October, 1995. The final chips with four channels will likely be tested at the factory and also at LAL for acceptance before being mounted on the front-end board. The analog section, discriminator and possibly amplifier, will be integrated in a four channel chip designed in Orsay.

2. TDC chip.
   The prototype TDC, without selective readout, is integrated in a 16 channel chip. It will be tested at Paris IV in the next few month using LabView for controls and measurements. The final version of the TDC will include the selective readout and will, most likely, be tested at the factory for functionality and then at Paris VI for acceptance.

3. Front-end card.
   The prototype front-end card is designed by LAL engineers and the debugging will be done by LAL in collaboration with Paris VI. It should incorporate the prototype analog chip, the prototype TDC and a readout logic implemented with discrete ICs. Also this prototype will include a VME interface for test purposes. The planned completion of testing this board is January, 1996. The final version of the front-end card will have the eight channel analog chip. It will be tested in France and probably will be used with a DIRC prototype at CERN.

4. DIRC Crate controller (Multiplexer).
   A prototype design should be completed in December, and testing completed in February, 1996. This will be tested at Ecole Polytechnique where it is designed. The final version should not be very different from the prototype and since there are only few (12 plus spares) of these boards. Ecole Polytechnique is expected to handle all the testing.

5. Personality module.
   A prototype is being designed by LBNL and SLAC. A board should be tested in December. One feature of this prototype is that it can be used for testing with up to four front-end boards without using the multiplexing and demultiplexing functions and the fiber optic links. Therefore without the DIRC crate controller. However, this will require some intermediate connection to a front-end crate. The final version of the personality module will be mass produced and tested since the same design will be used for the SVT, DIRC and IFR.

6. DAQ Board.
   A prototype exists at LBNL with planned completion of testing, with the personality module, in January, 1996. The final ROM will be mass produced and tested. However the final design cannot be completed before stringent testing of the prototype with software developed for the experiment.