# CCD and IR array controllers

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## ABSTRACT

A family of controllers has been developed that is powerful and flexible enough to operate a wide range of CCD and infrared focal plane arrays in a variety of ground-based applications. These include fast readout of small CCD and IR arrays for adaptive optics applications, slow readout of large CCD and IR mosaics, and single CCD and IR array operation at low background/low noise regimes as well as high background/high speed regimes. The CCD and IR controllers have a common digital core based on user-programmable digital signal processors (DSPs) that are used to generate the array clocking and signal processing signals customized for each application. A fiber optic link passes image data and commands to VME or PCI interface boards resident in a host computer to the controller. CCD signal processing is done with a dual slope integrator operating at speeds of up to one Megapixel per second per channel. Signal processing of IR arrays is done either with a dual channel video processor or a four channel video processor that has built-in image memory and a coadder to 32-bit precision for operating high background arrays. Recent developments underway include the implementation of a fast fiber optic data link operating at a speed of 12.5 Megapixels per second for fast image transfer from the controller to the host computer, and supporting image acquisition software and device drivers for the PCI interface board for the Sun Solaris, Linux and Windows 2000 operating systems .

Keywords: CCDs, IR focal plane arrays, optical astronomy, infrared astronomy

## 1. INTRODUCTION

The control and readout requirements for CCD and IR arrays in many astronomical applications are quite similar, motivating us to design controllers for both types of arrays that have many components in common. Aggregate data rates up to several Megapixels per second characterize visible light applications with CCDs and infrared arrays operating below the thermal infrared regime in ground-based applications. Typical clocking rates for both CCDs and IR arrays are in the range of one to ten microseconds per pixel with several clock transitions required per pixel. The number of clocks and DC bias supplies required to operate CCD and IR arrays varies quite a bit from one device to another, but is generally in the range of about a dozen for CCD and near IR arrays, and considerably more for IR arrays operating in the thermal IR regime. Similarly, clocking voltages are in the range of +10 to -10 volts for the arrays. Signal processing requirements for CCDs and IR arrays are somewhat different, as the pixel sampling circuitry of CCDs is reset before each pixel's charge is sampled, whereas IR arrays reset the entire array before the image is acquired. This allows a correlated double sampling circuit for CCDs to be implemented with analog circuitry that operates on one pixel at a time, whereas the correlated double sampler for IR arrays is implemented

digitally with the reset image being stored as an array of digital numbers that is subtracted from the exposed image after the entire image readout is complete. Readout noise figures for low noise, high amplifier gain, thinned CCDs at these readout times iof a few microsec per pixel is typically 4 to 7 electrons rms, with full wells of somewhat greater than 100,000 electrons. The readout requirements of IR arrays in the wavelength regime of one to 2.5 microns are similar, with four channels per array typically being read out in a few microsec, but at a bit higher readout noise and similar full well. The readout requirements of thermal IR arrays operated from the ground in the thermal IR regime are quite different since the background is so much higher, requiring that they be read out much more quickly from a larger number of channels to avoid saturation.

Control, data handling and array clocking requirements of CCD and near IR array controllers are similar enough that they can use many of the same components. The video processing requirements are quite different and require different designs and components. For the remainder of this paper we describe a controller design that has been used extensively for several years to operate both CCD and IR arrays of a great variety in a large number of applications worldwide, stress the commonality that has been achieved in the two controllers applications, and then discuss the different approach that is taken for thermal IR arrays.

## 2. CONTROLLER OVERVIEW

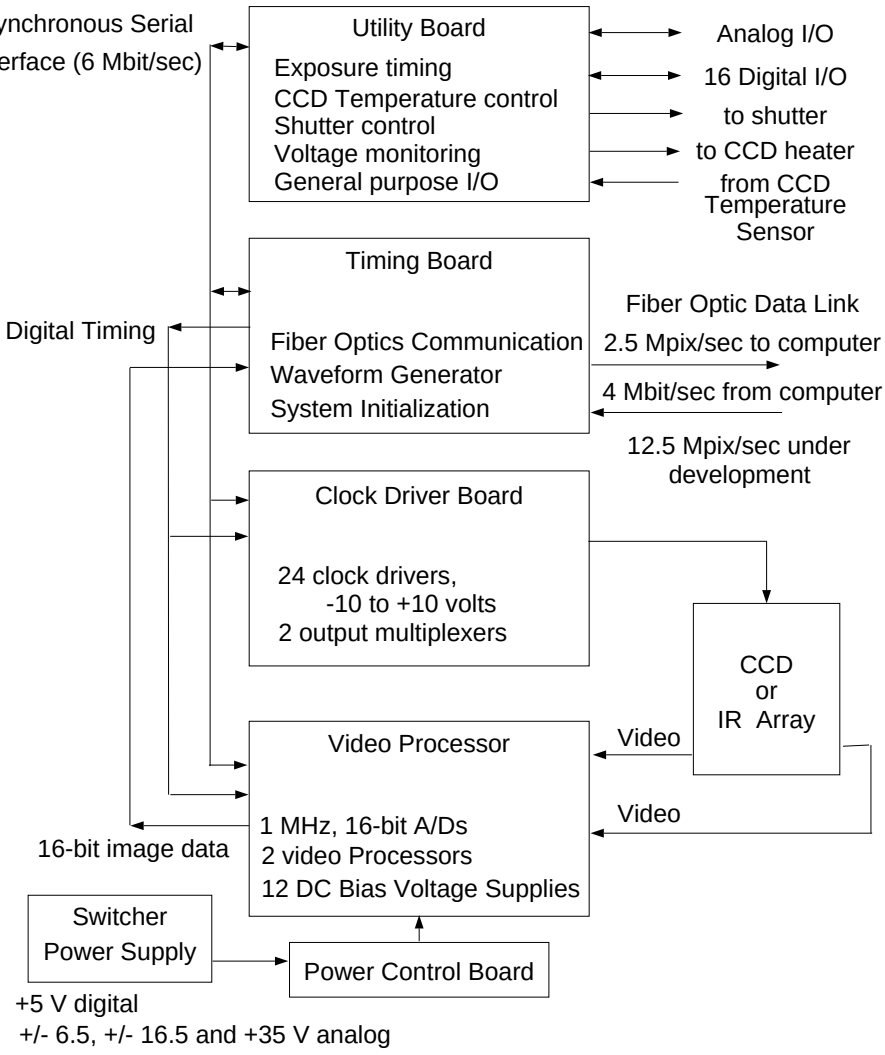


Fig. 1 - Block diagram of a dual readout CCD or IR array controller

Fig. 1 shows a block diagram of the controller design. Five different types of circuit boards reside in a controller housing. A utility board at the top of the figure that performs CCD temperature control and shutter operation is included in CCD controllers but not usually in IR controllers. The clock driver board supplies clocking signals to the CCD or IR array from digital timing waveforms generated by the timing board, while the video processor supplies DC biases to the array, and filters and digitizes the incoming video signals. A power supply consisting of commercially available switcher supplies resides in a separate box that can be located several tens of meters from the controller housing. A small power control board turns on the analog voltages to the controller boards in a programmable, gentle fashion to minimize transients that might endanger the array or the electronics, and turns off the analog power if certain voltage and thermal conditions are not met. More than one clock driver and/or video processor board may be installed in a system, as the clocking and video processing of multiple arrays occurs simultaneously.

Communication between the host computer and the controller is over a fiber optic link to the timing board, transmitting at an aggregate rate of 2.5 million 16-bit pixels per second Mbits/sec from the timing board to the host interface board. A faster

fiber optic data link is under development and has been demonstrated in a prototype PCI board that operates at 250 Mbits per second in both directions, and transmits 12.5 Megabytes of 16-bit pixels to the host computer. The host computer can be configured with a PCI interface board that operates in a 33 MHz, 32-bit wide bus and has device driver software support for the Sun Solaris operating system. Device drivers for Linux and Windows 2000 are under development. Alternatively, a host interface board for the VMEbus is also available.

In this architecture the video signals from each array readout circuit are processed in parallel from the same timing signals using separate video processors and A/D converters. At the end of the A/D conversion the timing board collects the 16-bit image data numbers from each A/D converter one by one and transmits them down the fiber optic link to the computer where they are stored. The maximum readout speed of the controller is determined either by the conversion rate of the A/D converters, which is one microsecond, or by the speed of the data transmission from the controller to the host computer.

There is a small difference in the clock driver circuits wherein slower rise time drivers with minimal overshoot and undershoot are used for IR arrays, and much faster circuits with about a volt of undershoot are used for CCDs. Differences between the CCD and IR array operation arise almost entirely in the processing of their video outputs. Most, but not all, CCD applications place the CCD controller within a meter or less of the CCD, allowing direct connection between the video output pin of the CCD and the controller. For such near IR arrays as the PICNIC and HAWAII, a small fanout board that contains the array socket and connections for the array signals also contains a JFET transistor for each video output to reduce amplifier glow compared to using the transistor that is located on the array. Additionally, a preamplifier for each video output is located immediately outside the cryogenic dewar to boost their voltage level and reduce their impedance, allowing the controller to be located a considerable distance away from the cryogenic dewar if required.

## 3. COMPONENTS IN COMMON BETWEEN CCD AND IR CONTROLLERS

A Motorola DSP56002 monolithic digital signal processor is used as the basic timing generator of the controller. The DSP functions as a timing generator by writing 24-bit data words to its data bus every instruction cycle, which are decoded by external circuitry to control various functions. Memory internal to the DSP is used for all array timing functions and performs with a timing resolution of 40 nanosec, but is sometimes limite by the memory size of 1024 locations total. Memory external to the DSP has been implemented with a bank of 32k x 24-bit SRAMs and is used for operations that do not require the speed that the internal memory provides.

To facilitate transmission of image data from multiple readouts a PAL is used to read image data from the analog-to-digital (A/D) converters on the video processor boards over the backplane, as it controls six address lines to read up to 32 A/Ds. Each A/D value is read by the timing board and sent over the fiber optic link, at the end of which the PAL reads the next A/D value until all of them are read. This sequence of A/D reads and transmissions is initiated with a single DSP command. This feature is implemented to allow array clocking to overlap with the image data transmission.

The DSP56002 implements an emulator function called the On Chip Emulator (OnCE) via four pins on the DSP. These are brought out to a fourteen pin connector with a pinout that matches a companion board that Motorola markets for operating from a Sun, Mac or PC. The emulator can be used for a variety of debugging tasks since it allows the DSP to execute code in real time, which can be interrupted by installing breakpoints so the user can examine the contents of all internal registers and memory locations.

An alternative timing board is available for IR systems that connects the controller to a PCI interface board via parallel copper wires using RS-422 differential drivers and receivers. The PCI interface board is manufactured by Spectral Instruments, Inc., and has Windows NT drivers and an associated image acquisition and analysis program tailored for IR array operation. It has a higher throughput than the 2.5 Megapixel fiber optic link, transferring data at 6.25 Megapixels per second. It is especially suitable for short and medium distances between the computer and the controller in environments that are not electromagnetically hostile.

During CCD readout the DSP writes 24-bit timing words to the backplane. The most significant eight bits make up a delay word that postpones the execution of the next word in the waveform table by a programmable number of 20 nanosec clock cycles. The most significant bit D23 selects either a coarse or fine delay mode, wherein coarse delay sets the number D16-D22 of 160 nanosec

delay steps, for delays over the range of 0.2 to 20 microsec. The fine delay selects the number D16-D22 of 20 nanosec delays, for delays over the range of 80 to 2500 nanosec. The remaining 16 bits are written to the backplane as digital timing signals for decoding by the clock driver and video processor boards.

These utility board provides controller functions not directly involved in the array readout, such as exposure timing, shutter control, focal plane array temperature control, power monitoring, and power turn onand off. It also has many non-dedicated analog and digital inputs and outputs that the user can customize, and is particularly useful for controlling peripherals such as shutters, filter wheels and stepper motors and monitoring temperatures. It operates from an interrupt service routine that executes every 800 nanosec, and uses an older style DSP56001 with extensive electrically erasable programmable read only memory (EEPROM) on board. For systems that do not require temperature control or additional I/O the utility board is not needed since the timing board can perform the power on, exposure timing and shutter control functions.

The power control board contains five switches to turn on the analog power supplies +6.5, -6.5, +16.5,-16.5 and +36 volts from the incoming power supply cable onto the backplane where it is distributed to the video processor and clock driver boards. A jumper can be installed on the board to prevent the +36 volt supply from being connected to the backplane in IR systems. The powr control board turns on the power with a linear ramp lasting a few milliseconds on command from the utility or timing board in order to avoid power glitches from passing to the fCCD or IR array that might occur with an sudden or uncontrolled power surge. It also has voltage comparators monitoring the power supply voltages to turn off the supplies if the voltages fall outside allowable limits. The digital logic on the board is powered any one of the +5, +6.5 and +36 volt supplies so that if all but one of them fail the board can still shut the power down gracefully. The power control board is four slots in width and clamps on to the back of the backplane. It has a large, heavy duty circular connector to the power supply.

The clock driver board generates 24 clocked signals over the range of -10 to +10 volts for driving CCD or IR array clock registers directly. Several clock driver boards may be installed in a single controller system for driving multiple arrays. The clocks are generated by analog switches selecting from one of two voltages determined by DACs, whereby up to twelve switch states on a clock driver can be changed in a single 40 nanosec instruction cycle. The clock drivers for the array operate with a fast op amp circuit connected to the analog switch that produces 60 mA of sustained output current, and slews over a ten volt range in 20 nanosec with no load. The clock drivers for IR arrays are much gentler, switching in 200 nanosec for a four volt range. The DAC voltages are updated over the serial link from the timing board, taking about 2 microsec per voltage. MOSFET switches are placed between the clock drivers and the output of the board to prevent voltage transients from reaching the focal plane array by disconnecting the clock drivers from the array until they are fully configured during power up, or by quickly disconnecting them if there’s a power failure. Finally, there are two multiplexers on the board that can each route any one of the 24 clocks to coaxial SMB connectors mounted on the front of the board for viewing on a scope during system integration.

Power distribution and communication between the boards takes place over a custom built backplane similar to the VMEbus backplanes, and contains 96 signal, power and ground pins utilizing DIN-96 connectors. The boards all communicate with the DSP on the timing board via a serial link running at 6 Mbits/sec. Communication is bidirectional between the timing and utility boards, and unidirectional from the timing to the clock driver and video processor boards, being used solely for configuring the digital-to-analog converters (DACs) and slowly changing switches and multiplexers. Digital timing is provided to the clock driver and video processing boards with a time resolution of 40 nanosec over 16 signal lines over the controller backplane, with 4 bits serving as address lines to select which board is being addressed, and 12 lines being updated in each time slot. This allows many clock driver and video processor boards to be installed in the same system. Finally, 16 image data bits are transferred in parallel from the video processor to the timing board over the controller backplane for transmission over the fiber optic data link to the computer.

The power supply contains commercially available switcher modules. They are encased in a heavy aluminum box that contains large inductance toroids to reduce the noise generated by the switchers. Slightly lower readout noise with a fast readout, low noise CCD has been achieved with the switcher power supply than with the older linear design with a toroidal transformer. Some of the switchers contain remote sense circuits that maintain a constant voltage at the power control board, and necessitate that remote sense wires for each of the supplies be run through the power supply cable. This enables the power supplies to be operated with a range of power supply cable lengths up to several tens of meters without adjusting the power supply voltage for ohmic losses in the cable. Two sizes of power supplies are available - a smaller one with lower current output supplies that does not contain the remote voltage sense capability. The larger one has twice the current output, along with remote voltage sense on all supplies except for the

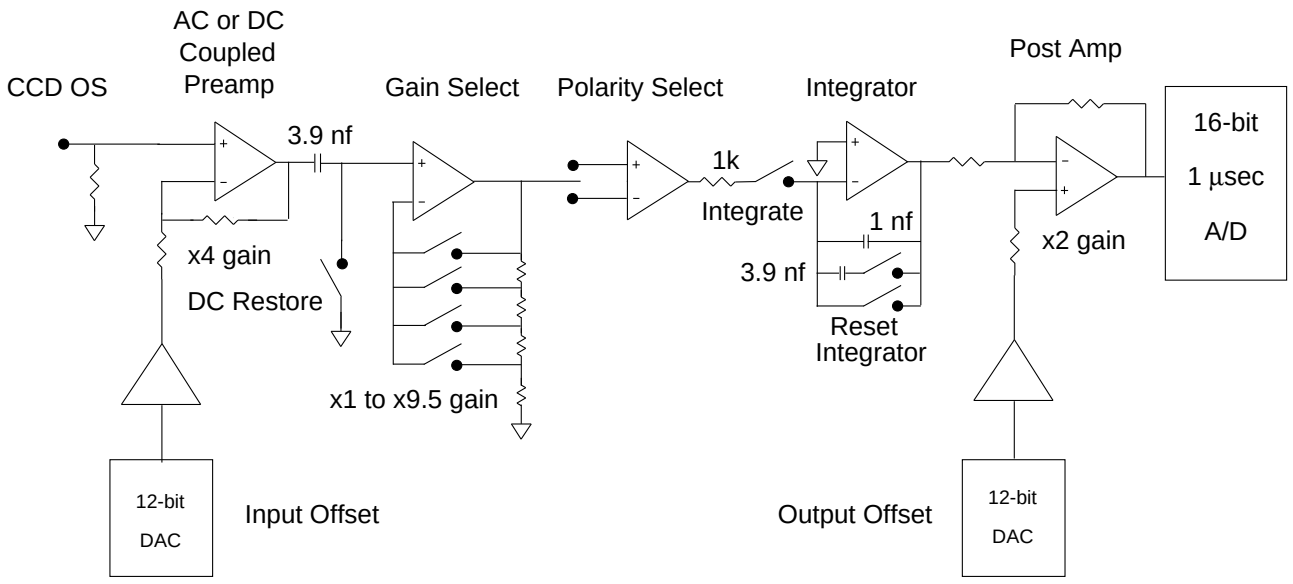


Fig. 2 - Block diagram of the CCD video processor

fan supply. The larger power supply is targeted to controllers with many video processor boards or systems that require a large distance between the controller and power supply where the remote sense capability would be beneficial. A +5 volt supply provides power for the digital logic on the controller; +/- 6.5 volt power is supplied to be down-regulated to +/- 5 volts for the analog power on the A/D converters and some of the video processor op amps, while the +/- 16.5 volt power is similarly down regulated to +/- 15 volts for the A/D converters and the clock driver and video processor op amps. The +35 volt supply drives several op amps that generate up to +30 volts for the drain supplies of CCDs, and for the preamplifier op amp if configured in DC coupled mode.

## 4. VIDEO PROCESSING

The CCD video processor is shown schematically in Fig. 2. It contains a low noise front end preamplifier that is AC or DC coupled to the CCD and contains a DAC controlled input offset adjustment. The preamplifier contains and Analog Devices AD829 voltage feedback, low noise op amp, chosen for its low voltage and current noise. It is a bipolar transistor op amp whose current noise and bias currents are considerably higher than similar FET op amps, but whose voltage noise is much less. Recently developed low noise, high speed CCDs have output impedances of several hundred ohms, making the current noise contribution of the AD829 op amp smaller than its already low voltage noise, especially when operated in a high gain circuit (x4) such as this one. Variations in bias current are relatively unimportant due to the short time between the sampling of the reset and signal levels in a correlated double sample circuit such as this one.

The preamplifier connects to a post amplifier through a DC restore circuit operating every pixel that has a choice of four software controlled gains over a range of x1 to x9.5. It is a low impedance driver feeding a pair of amplifiers to select the polarity of the signal input to the integrator. The output is summed on a classical analog integrator, followed by an A/D driver, offset adjustment and x2 gain stage. The A/D converter has 16 bits accuracy and a one microsec combined sample-hold and conversion time. A/D converson overlaps with all operations of the video processor board, allowing total pixel readout and processing times as short as one microsecond. Two identical video processors are installed on each video processor board for connection to two separate CCD readouts, with a shared PAL on the board for address decoding when reading the A/D digital output values and setting the voltages of the DACs.

Four DAC packages are provided on each video processor board, with each package containing four separate DCA circuits, for a total of sixteen DAC voltage outputs per board. Four of these are used for the offset circuits (input and output offsets on each of two video processing circuits) and the remaining twelve generate low impedance, low noise DC bias supply voltages. Similar to

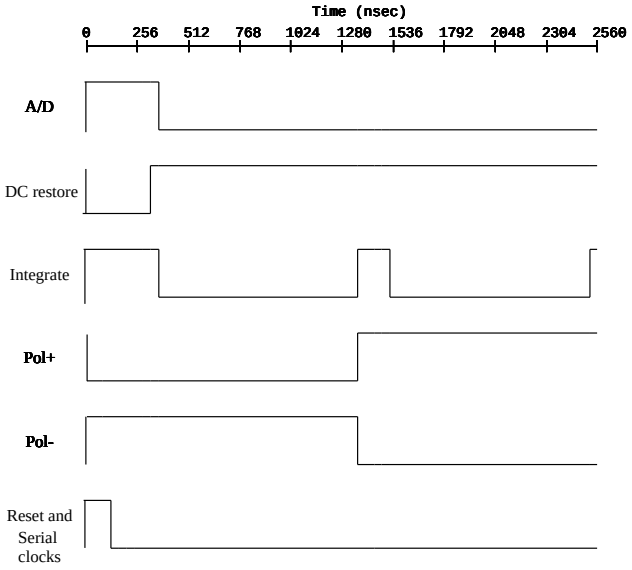


Fig. 3 - PIxel and video processing clocking waveforms generated by waveform visualization software

the clock driver board, MOSFET switches are placed between the DC bias supply drivers and the board output to enhance the safety of the focal plane array.

Waveforms generated by the timing board are shown in Fig. 3 below for the case of a pixel time of 2.56 microsec and a total signal integration time of 2.0 microsec. It is important for achieving good noise performance at fast speeds to maximize the amount of time the video processor spends doing this integration since it directly reduces the bandwidth of the signal chain and reduces the noise. One microsec is spent integrating the video signal immediately after reset of the CCD output node and one microsec is spent integrating the signal after the charge is dumped from the summing well to the output node. The integrate signal is low while the integrator is active, which the POL+ and POL- signals change the polarity of the signal input to the integrator, causing a subtraction of the signal after reset from the signal after charge is dumped. Most of the clocking occurs during the first part of the pixel time, as the serial clocks are cycled through all but the charge dump onto the output node, the CCD and integrator are reset, the video processor is DC restored and the A/D conversion of the previous pixel is initiated. Also during this time the A/D counts from the previous pixels are transferred from the video processor board through the timing board to the host computer.

The video processing for IR arrays is somewhat simpler. JFETs are placed inside the cryogenic dewar right next to the array for buffering the video output from each channel. A preamplifier module with four non-inverting op amp gain stages mounts immediately outside the dewar and is capable of driving modest cable lengths between the dewar and the controller electronics. A standard one stage preamplifier with fixed gain and bandwidth is available, as is a newer two-stage preamplifier with programmable gain and bandwidth to allow selection of widely different readout speeds. The next stage is located in the controller housing, and it uses a simple RC filter for bandwidth liming and noise reduction chosen to be about 5 times the fastest pixel readout rate, while slower readout rates rely on the bandwidth limiting in the programmable preamplifier. It connects to a gain and offset op amp to allow offset matching between the multiple channels of an array. The same 16-bit A/D converter as is used inthe CCD video processor completes each video processor circuit.

## 5. MID INFRARED CONTROLLERS

Thermal IR arrays such as the Rockwell CRC-774 and the Boeing P/N 50078 that are operated in ground-based, high background environments typically detect so much background flux that the array saturates on a time scale of tens of milliseconds. This is faster than the readout time for the controllers operating four or fewer readout channels that have been discussed so far, so clearly a different approach is needed. These arrays provide more readout channels, generally either 16 or 32. Even for arrays operated at 5 microns readout speed is critical and the manufacturers of the Aladdin and HAWAII-II have provided for 32 readout channels, though mercifully the HAWAII-II array can optionally be read out from 4 channels for lower background observations. To handle the larger number of readouts required for these arrays a specialized board is available with our controllers that includes four video processors with four A/D converters. Systems for these 16 or 32 channel arrays will require either four or eight of these boards. Each board also has a DSP and a large, fast access image memory that is 1024 x 1024 x 32 bits in size that is used for coadding images up to 32 bits of precision on the video processor before the image is transferred to the host computer. Up to 65536 images can be coadded. This enables the image transfer to the host computer to be slower than the readout rate, so the fiber optic link does not have to be so fast. It also distributes the coaddition burden over four or eight DSPs that are dedicated and well suited to this task, rather than relying on the host computer. As an example, the Rockwell CRC-774 array readout time with our controllers is 6.5 milliseconds, and the transfer time to the host computer of a coadded 32-bit image of 320 x 240 pixel image size is 76.8 milliseconds.

## 6. SOFTWARE SUPPORT

DSP code that executes in the timing, utility, VME and PCI interface boards is derived from software development tools available from Motorola. An assembler, a linker, a software simulator and several format translation programs are available from Motorola's Web site. DSP code for a particular board consists of two parts. Boot code to initialize the DSP, process commands, read and write from memory and communicate over the serial links is loaded into the DSP from on-board EEPROM memory after the DSP is reset. Any changes in boot code must be done by writing to the EEPROM. Application code consists of the remaining code required to operate a board, and contains such things as clocking and DC bias voltage tables, timing waveforms, temperature control algorithms, and exposure timers. Application code is written to the DSP and possibly to on-board SRAM memory either rom the on-board EEPROM or by downloading from the host computer over the communications link. A typical development cycle consists of editing the application source code file with a text editor, execution of a script to assemble, link and generate a downloadable file, downloading the file from the host computer, and testing it. This cycle can take as little as a few seconds. Once the application code reaches a certain level of stability the user can write it to EEPROM memory and have the DSP read it directly.

To help the user develop timing code for reading out arrays a waveform visualization program named Waveform has been written that reads the tables of waveform numbers from the timing board source code and plots them as a conventional timing diagram that the user can easily understand. Editing of the waveforms is done manually by editing the numbers in the source code. Fig. 3 above was generated from this program.

A user interface, image acquisition and display program named "voodoo" has been written and distributed in source code form to users for use with the fiber optic PCI interface board for either CCD or IR arrays. It is a written in Java for maintainability by users and for portability across several operating systems. It is a windowing program that communicates with the PCI interface board through a device driver to provide point and click specification of controller functions and exposure control. Control over loading the application code into each DSP is provided, along with turning power on, specifying image dimensions, displaying images through standard display programs, recording images on disk in FITS format with a keyword editor, and running sequences of exposures. A device driver for Sun Solaris has been written and device drivers for Linux and Windows 2000 are under development. Complementary to this image acquisition program is more comprehensive acquisition and analysis program available only for Windows NT that provides extensive display, bad pixel removal, array control, and image diagnostic features for use with IR arrays.