A Real-Time Transverse Momentum Discriminator for the BABAR Level 1 Trigger System[1]

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Abstract

The Transverse Momentum Discrimination Module (PTDM) is one of the three main modules used in the Level 1 Charged Particle Trigger System of the BABARDetector at PEP-II. It provides trigger decisions for charged particles with a transverse momentum, $P_{\rm t}$, greater than a configurable threshold. The transverse momentum discrimination algorithm works by evaluating the curvature of the charged tracks in the 1.5 T axial magnetic field. The capabilities of the PTDM are key to a stable and efficient operation of the BABAR experiment even at severe background conditions. A sharp threshold behavior with an efficiency rise from 10% to 90% within 30 MeV/c at 600 MeV/$c$is achieved by using track segment information with very good spatial resolution (0.7 mm). This resolution is obtained by evaluation of the drift time information from the drift chamber [1]. In this paper the design and implementation of the PTDM is described.

I. INTRODUCTION

The Level 1 Drift Chamber Trigger system provides trigger decisions within 6 μs [2, 3]. It consists of three types of printed circuit boards, 24 Track Segment Finder Modules (TSFM), one Binary Link Tracker Module (BLTM) and 8 Transverse Momentum Discriminator Modules (PTDM). The TSFM [4] are used to find groups of up to four hits that are contiguous (in space and time) and to link them to form track segments. Very good spatial resolution (0.7 mm) is achieved using drift time information from the drift chamber. The results of the TSFM algorithm are passed both to the BLTM [5], which links the track segments to form complete tracks, and to the PTDM. The final Level 1 trigger decisions are made by the central trigger logic (GLT). The GLT combines the detailed information from the drift chamber trigger containing charged track multiplicities and spatial information with calorimeter cluster information (track-cluster matching) from the calorimeter trigger and starts the readout of accepted events.

The drift chamber is a small-hex-cell design and contains 40 layers with a total of 7104 drift cells. The 40 layers are grouped four each in 10 radial superlayers. There are four axial superlayers (A1, A4, A7 and A10), with each pair of axial superlayers separated by two stereo superlayers (U2, V3, U5, V6, U8 and V9). Each superlayer is divided into 32 sectors in the azimuthal direction. A magnetic field of 1.5 T, parallel to the beam axis, forces charged particles on a circular trajectory and facilitates the measurement of their transverse momentum. The drift chamber front-end electronics system [6] continuously contributes "real-time" information (hit signals) about particle-related activity to the drift chamber trigger system at a rate of 3.7 MHz.

The drift chamber trigger decisions contain detailed informations about charged track multiplicities as well as spatial information and thus allow the subsequent logic combination of charged tracks with calorimeter clusters at lowest trigger level (track-cluster matching). Excellent detection efficiency for physics processes is required in order to minimize systematic experimental errors and to avoid losses of rare physics events with low track multiplicity. At the same time it offers efficient background suppression allowing it to keep the rate of accepted events smaller than 2 kHz. This rate limit is given by the subsequent Level 3 Software Filter Trigger and the DAQ system.

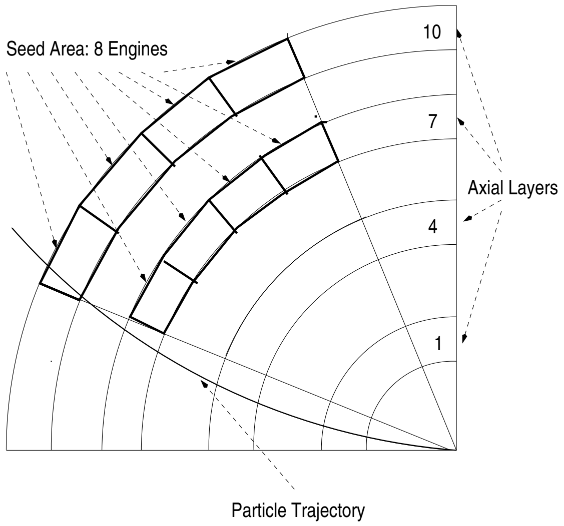

Figure 1: Geometry Implementation

II. PT DISCRIMINATOR

Each of the eight $P_{\rm t}$ discriminator boards receives track segment data from the six track segment finders corresponding to one drift chamber quadrant. It looks for "seeds" in one of the "seed" layers (axial superlayers 7 or 10) within one 1/8 wedge. Using detailed azimuthal position information for the segments of the four axial superlayers each of the eight PTDM evaluates whether a sufficient number of track segments lie inside a pre-defined envelope and thus are consistent with a particle

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track of a transverse momentum P_t greater than a specified minimum. The PTDMs overlap by one 1/16 wedge allowing them to process data from neighboring wedges (see Figure 1). For P_t discrimination only the four axial superlayers are used since their wires have constant positions in the transverse (x-y) plane, independent of the position along the beam axis. The processing on each board is subdivided in eight processing engines, one for each of the 8 seed areas covering a 1/32 wedge of the drift chamber in one of the two superlayers (A10 and A7).

III. HARDWARE IMPLEMENTATION

The PTDM has been implemented as a 9U $\times$ 40 cm 10-layer printed circuit. It comprises six separate functional units, namely the engines, the memories, the post processor, the DAQ memories, the diagnostic memories and the control logic.

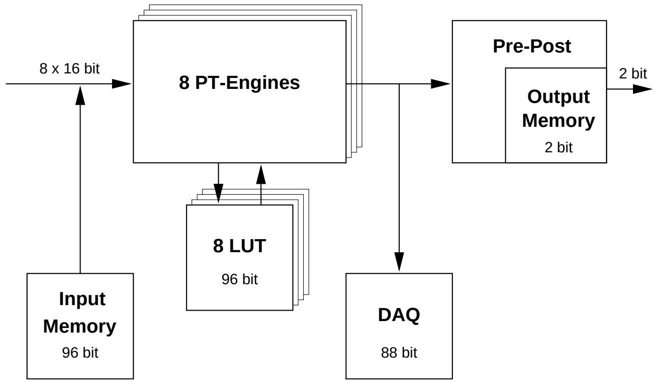

Figure 2: PTDM Board Implementation

The principal components in each channel are an algorithmic processor engine and programmable look-up memories which contain the limits for each individual seed position. The contents of the look-up memories thus specify the envelope of allowed track segment positions for each of the three other axial superlayers and consequently define the effective P_t discrimination threshold. A sketch of the process schematics on one of the eight PTDM boards is shown in Figure 2. The engines, as well as all other control logic, have been implemented using Lucent Technologies OR2C series field programmable gate arrays (FPGAs). All FPGAs were programmed using the VHDL hardware description language in order to shorten development time, while keeping the design flexible and easily upgradable.

A. The PT Engines

The eight P_t engines function as the main data processing unit. They receive 96 bits worth of track segment data from six Track Segment Finders at a rate of 30 MHz. Each engine has a dedicated bank of six look-up table memories. These memories contain information about the envelope positions for each possible track trajectory. A detailed description of the algorithm performed by the engines is given in section IV.

B. Look-up Table Memories

The look-up table memories are organized according to the algorithmic steps. For each seed position the envelope is defined by three 96-bit words. The first word contains the mask used to select the cells which are situated entirely within the boundaries of the track envelope. The fine position testing (second step) is done using the remaining two data words: The second word is the limits mask, specifying the two cells per superlayer that lie partially within the boundaries of the track envelope. The third word describes the fine position of the envelope boundary at the subcell level.

C. Post Processing

The P_t discriminator processes the track segment data at a cycle frequency of 3.7 MHz (clock-4). The results from the eight engines are further processed before being sent off-board. First the A7 and A10 outputs belonging to the same 1/32 wedge are "OR"ed together to produce a 4-bit word. This word is delayed by one clock-4 cycle and stretched in time by two clock-4 cycles in order to facilitate the matching with signals from other trigger boards. Afterwards the bits from adjacent wedges are "OR"ed together. The resulting 16 bits (2 bits from each PTDM) are sent to the Global Trigger Logic to be combined with track positions from the BLTM and calorimeter trigger information from the Level 1 calorimeter trigger to produce trigger decisions.

D. DAQ Memory

A set of DAQ memories providing detailed information about the decision algorithm allows run-time monitoring of the trigger performance. A continuous stream of detailed P_t data is temporarily stored in a 2k-word deep circular latency buffer at a rate of one word per clock-4 cycle. This buffer has sufficient storage to hold the history of local data during the time required for the trigger decision to be made.

Upon receipt of a Level 1 trigger signal issued by the global trigger logic, eight of the DAQ words are transferred into a four event deep DAQ buffer, representing a 2.2 μs time slice. Each word consists of 88 bits, 11 bits per engine. Each engine saves the status of its output, the fine position of its seed and the number of superlayers with a valid track segment corresponding to its seed. During a read-event each PTDM sends this data to the upstream read out module (ROM), totaling of 100 bytes, including the 4-byte header.

E. Play Record Memories

Each board is equipped with play/record memories for board testing and diagnostics to aid in the board debugging, verification and calibration. These memories are implemented both at the input and output of the PTDM and thus allow to operate the boards independent of the trigger electronics environment. The memories can be loaded with data from computer generated events so that event data can be propagated through the system with the aim to monitor the system performance and to calibrate the trigger. Alternatively it is possible to record real data or computer generated data injected further upstream, in order to monitor the performance of a certain board or partial system. This feature has proven particularly useful during the debugging and functionality analysis of the board algorithms.

F. Fast Control Logic

The entire board is controlled by a pair of FPGAs, a Fast-Control unit and a Board-Operation-Controller. The Fast-Control unit implements a high speed serial command and data link with the Read-Out-Module for the remote control/configuration as well as data I/O. It serves as a command and data interpreter and is a generic chip common to all drift chamber trigger modules and the global trigger logic.

G. Board Operation Controller

The Board-Operation-Controller implements the interface and memory control logic specific to the PTDM. It controls the board operation during both run-time and non run-time. This includes the generation of memory addresses and read and write strobes as well as other logic control signals.

H. Interfaces

All cabling is handled by a small (6U) back-of-crate interface board behind each main board. A PT Discriminator Interface Board connects the PTDM to six TSFM boards using differential receivers and 100 mil shrouded-header connectors. It also accommodates the interface to the global trigger logic consisting of one driver.

IV. Implementation of the PT Algorithm Software

A. Design

The design of the trigger architecture and selection algorithms is based on extensive simulation studies of the detailed response of the BABAR detector to physics and background events. A software model of the complete Level 1 Trigger electronics pipeline was developed for this purpose. This model consists of 20,000 lines of Fortran code and describes various potential hardware-implementable trigger algorithms. Over 400 possible parameters of the design were varied and tested using millions of physics benchmark and background data. The final design was chosen from among those variations.

A major fraction of the design effort has been dedicated to the implementation of the trigger algorithms described above in VHDL code to operate within Field Programmable Gate Arrays (FPGAs). One PTD board has 11 FPGAs comprising 400,000 logic gates synthesized from 20,000 lines of VHDL code. Design and prototyping efforts were greatly sped up by state-of-the-art Computer Aided Design tools [7]. These sophisticated tools, which include routing algorithms for logic arrays and gate level simulation, facilitated detailed simulations of the board operation including a multichannel logic analysis that takes into account the placement dependent signal delays inside the FPGAs. The use of these tools greatly helped to streamline the design process.

B. PT Algorithm

The algorithm processing is begun when a seed is found in the data from the TSFM. To qualify as a seed, the estimated resolution of the position as determined by the TSFM must be better than 1/14 of the cell size (0.7 mm). The evaluation of the transverse momentum criterion is then performed in three steps: 1) All track segments in cells which are situated entirely within the boundaries of the track envelope for the given seed are counted for each superlayer; 2) the track segments in the cells at the borders are added to the counter if they satisfy the fine position conditions; 3) all superlayers with an above-zero count of valid track segments are added up. The number of valid superlayers is then compared to a programmable register within the engine to determine overall track acceptance based on a two out of four, three out of four or four out of four requirement.

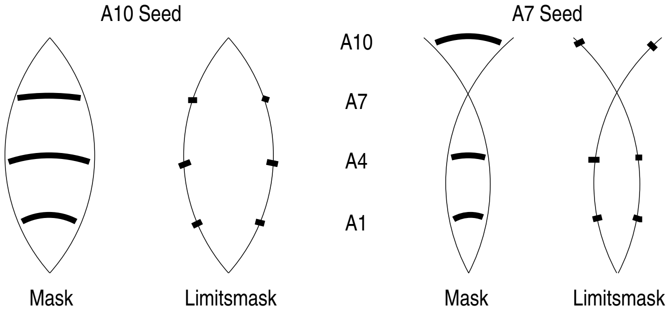

Figure 3: Format of Look-up Table Envelope Information

<table>
<tr><th colspan="8">Cycle</th><th>Action</th></tr>
<tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td></td></tr>
<tr><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Latch TSFM Data</td></tr>
<tr><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td>Test for Seed</td></tr>
<tr><td></td><td></td><td>*</td><td></td><td></td><td></td><td></td><td></td><td>Read Mask-word</td></tr>
<tr><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td>a: Mask && Data</td></tr>
<tr><td></td><td></td><td></td><td>*</td><td></td><td></td><td></td><td></td><td>Read Limitsmask</td></tr>
<tr><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>b: L-mask && Data</td></tr>
<tr><td></td><td></td><td></td><td></td><td>*</td><td></td><td></td><td></td><td>Read Limits-word</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td>c: Data within Limit</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td>a || (b && c) for each SL</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td>Sum SL Results 3/4</td></tr>
</table>

Table 1
Flowchart of the P_t Discriminator Algorithm

One complete algorithmic cycle takes 269 ns and consists of eight synchronous subcycle steps. The realization of the subcycles in time is schematically shown in Table 1. A sketch of the data flow between the processing steps is given in Figure 4. 1) The track segment finder data are latched to the engine. 2) Each engine tests the data for a seed within its assigned area. Layer 10 and Layer 7 contain 4 areas per board. Each area is processed separately by one engine (see Figure 1). 3) In case a seed is found, the 96 bits long mask-word corresponding to the position of the seed is read from the six look-up table memories. As sketched in Figure 3 the mask-word indicates the positions of the cells within the three other axial superlayers that fully lie inside the envelope given by the chosen $P_{\rm t}$ threshold. 4) The data for the three non-seed axial layers of each engine are formatted such that a simple bitwise logical "AND" yields the information whether a track segment lies inside the $P_{\rm t}$ envelope. At the same time the limits-mask word is read from the look-up table memories. This word specifies the cell numbers of the two cells situated at the boundaries of the envelope (see Figure 3). 5, 6) In case the cell numbers of mask and data agree the subcell spatial information of the data is compared with the limits-word that defines the subcell boundary position of the $P_{\rm t}$ envelope. 7) The two results from mask-word test and limits test are "OR"ed for each superlayer independently. 8) At last the results from each superlayers are summed up. The standard setting produces a positive $P_{\rm t}$ decision if in at least 3 out of 4 superlayers including the seed layer valid track segments are found within the envelope.

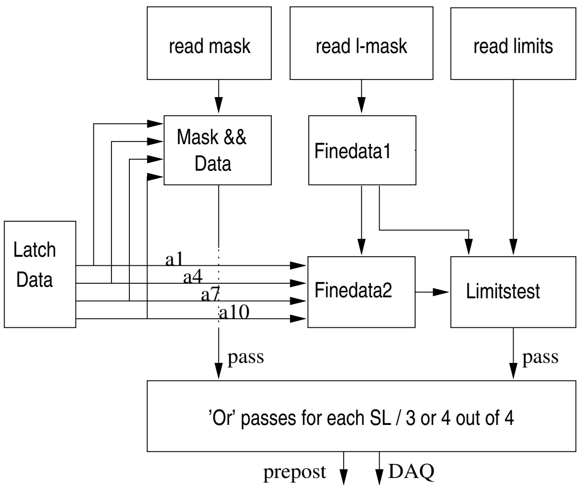

Figure 4: Engine Schematics

V. Design and Test Methodology

The development and test of the board design and production relied on a scheme of triple redundancy: 1) during the design phase a software model of the complete trigger was developed to reproduce the functionality of the hardware components. This software was used to study efficiency and background suppression capabilities of each of the trigger modules and to optimize the trigger algorithms. In the test phase this software was used to generate test patterns from simulated physics events as input to the test procedures and to predict the correct algorithmic behavior; 2) extensive tests of the algorithmic and logic functionality of the board were performed throughout the complete design phase and during board testing using advanced Computer Aided Design Tools; 3) finally, a prototype of a fully loaded $P_{\rm t}$ discriminator board was tested and compared to expectation.

A. Design and Performance Studies

In the design phase the software model of the trigger was used to study the trigger performance for various hardware design options. The package allows to use Geant-Monte Carlo simulated physics events as well as background signals. With the help of this package the charged particle trigger algorithms were optimized by systematically varying each of the algorithmic steps.

The studies show that the $P_{\rm t}$ discrimination of charged particle tracks with low transverse momentum in the range between 400 MeV/$c$and 1 GeV/c helps to efficiently suppress backgrounds and that the $P_{\rm t}$ Discriminator Modules are key to a stable operation of the BABAR experiment in a high background environment. At the same time, in order not to compromise the efficiency for $B\bar{B}$ physics events, the $P_{\rm t}$ discrimination algorithm must provide a sharp turn-on behaviour. The performance of the final $P_{\rm t}$ discriminator described in this paper is illustrated in fig. 5. It shows the efficiency to detect single muons as a function of their transverse momentum. The solid line (A') shows the $P_{\rm t}$ discrimination threshold behaviour for a pre-set nominal value of 600 MeV/c. An excellent efficiency rise from 10% to 90% within 30 MeV/c is achieved. Also shown are the limits in transverse momentum imposed by the drift chamber geometry and the axial magnetic field of 1.5 T for short tracks (B, traversing the inner five drift chamber superlayers) and long tracks (A, reaching the outermost superlayer layer).

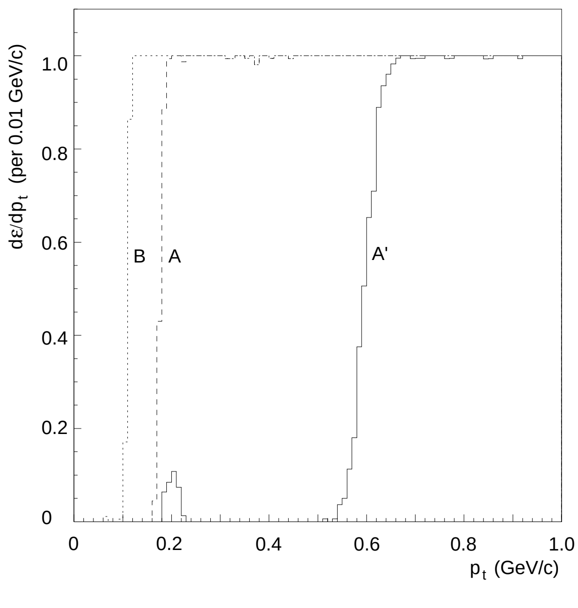

Figure 5: Turn-on curve of the BABAR $P_{\rm t}$ Discriminator Module as obtained from simulations of single muons. The simulated transverse momentum discriminator threshold for a pre-set value of 600 MeV/c is indicated by A'. Also shown are the limits in transverse momentum for short tracks (B) and long tracks (A) imposed by the drift chamber geometry and the magnetic field.

B. Board Test Methodology and Results

The debugging of the algorithm software and look-up table contents proceeded in two steps by making use of the play/record memories:

1) In the first step test data were produced systematically varying the positions of the track segments in steps of one unit in azimuth. This way the turn-on turn-off behavior of the $P_{\rm t}$ discriminator at the boundaries of the envelope was scanned for random seed positions. This procedure was particularly powerful in detecting problems in the encoding of the look-up table mask and limits words. 2) In the second step the bit level hardware simulation of the BABAR Trigger was used to produce physics events for both board input test vectors and output predictions. This way all essential algorithmic features could be tested before the prototype board was fabricated.

Since the algorithm had been tested successfully and thoroughly, the prototype test itself concentrates on the functionality of the hardware. The hardware test included the verification of the PC board schematics, the stability of the play/record memories and look-up tables, the timing constraints of the synthesized FPGA logics necessary to run the synchronous algorithm logics and interface connectivity tests with the Track Segment Finders and the Global Trigger Logic. For the prototype tests a teststand was set up that implements all test procedures as simple push-button operations using the Tcl/Tk language for a graphical user interface in conjunction with standard BABAR online-dataflow software.

On this teststand a mass event board test was performed using 10^5 generated physics events. The test showed bit-by-bit agreement between board simulation, off-line trigger simulation and prototype results.

VI. Summary

The $P_{\rm t}$ discriminator module of the BABAR Level 1 Charged Particle Trigger System has been successfully designed, prototyped and tested at the Lawrence Berkeley Laboratory. Extensive Monte Carlo Simulation studies of the complete trigger system have shown that the $P_{\rm t}$ discrimination of charged particles is key to the stable and efficient operation of the trigger in a potentially high background environment. The discrimination algorithm implemented in the eight PTDM makes heavy use of the FPGA technology in connection with user-configurable look-up tables in which the discriminator threshold is described by envelopes corresponding to the track curvature of particles with minimum allowed transverse momentum. The Prototype and one preproduction board were successfully tested showing that electronics simulation, off-line simulation and board tests agree at the level of 10^5 events. The production assembly of 10 further PTDM has just been completed.

VII. References

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