Front End Electronics for the STAR TPC

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The front end electronics (FEE) for the STAR TPC receives signals from the 136,600 pads on the TPC, amplifies them, shapes them, and digitizes them with a 512 time sample, 6/12 MHz, 10 bit waveform digitization system[1].

The waveform digitization is done in two custom analog chips, the STAR Amplifier/shaper, which contains a low noise preamplifier, shaper and buffer, and the SCA/ADC, which contains a 512 time bucket switched capacitor array and a 12 bit ADC; both chips are 16 channels wide. These chips are contained on 32 channel FEE cards which plug into the TPC sectors.

Up to 36 FEE cards are read out by a single readout board, which multiplexes the data and sends it to the data acquisition system over 1.2 Gbit/sec fiber optic links. A trigger distribution system initiates data acquisition and calibration events, while a slow controls link monitors temperatures, currents and voltages, and can provide an alternate (slow) data readout path.

In 1997, the STAR system test[2], was gradually developed to read out a full TPC supersector, with 181 FEE cards read out by 6 readout boards. In July, the complete system was moved to the just completed TPC, for a cosmic ray test. Over one month, over one hundred thousand cosmic ray events were collected; the data was used to test the TPC field cage. These events also provided a comprehensive test of the FEE, and the data was used to tune up the FEE board design to eliminate crosstalk in the ADC section of the SCA/ADC[3].

With this in hand, full scale FEE board production began, and by the end of 1997, about 800 boards had been completed. The boards are being stuffed and soldered at MPI Munich, with testing and final backer assembly done at LBL. At the same time, power supply chassis and cable production was completed at LBL. Readout board and clock and trigger distribution system design are continuing.

We have also modified the FEE design for the main TPC so that it is suitable for the STAR forward TPCs[4]. This entailed lengthening the SAS shaping time to 400 nsec and reducing power consumption; both of these changes were achieved by changing SAS control voltages. The SCA sampling rate was also reduced, to about 5 MHz. The SAS and SCA chips also required repackaging into smaller packages to fit the very limited space. These custom chips are in hand and packaged, and the design is well advanced.

References

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[2] W. Betts *et al.*, "Results from the STAR TPC System Test," IEEE Transactions on Nuclear Science. **44**, 592 (1997).

[3] Presentations by H. Wieman *et al.*, I. Sakrejda *et al.*, and E. Hjort *et al.*, at the 1997 APS Division of Nuclear Physics Meeting, Oct. 5-8, 1997.

[4] "The Forward Time Projection Chamber for the STAR Detector," F. Bieser *et al.*, MPI-PhE/98-3, Jan. 30, 1998.