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To: Peter Wilson

From: Michael Lindgren, for the Review Panel

Subject: CDF Time of Flight Electronics Review Report

The CDF TOF electronics review panel met 13 July 2000 with the TOF Electronics team for a review of their plans and production status. The review panel members were Bill Foster, Jonathan Lewis, Michael Lindgren, Charlie Nelson, Jim Patrick, Harold Sanders, and Terry Shaw. Presentations from Joseph Kroll and Matthew Jones of the University of Pennsylvania were made which covered the status and readiness of the TOF electronics. The clock system was discussed in their presentations, but no separate presentation was made covering it in detail.

The committee charge included:

1. Evaluate the design for time-of-flight electronics using ADMEM boards to determine that this planned system will meet the performance requirements.
2. Evaluate if the manpower is sufficient.
3. Is there a credible schedule for completion and installation of the readout electronics by 1 March 2001.

Status and Summary

The current status of the project is that the active elements, PMT's, bases, preamps, and readout cables have all been installed in the detector. This is the first review for these components. The ADMEM boards and Café cards have all been produced and tested by the calorimeter electronics personnel. The remaining parts of the system and their status is as follows:

Transition board - The transition board is a 9U board that resides in the rear of the crate, which is used to receive and split the signal from the preamps and send them to the ADMEM through the backplane. The board has DAC's, ADC's, a digital interface to VME, communication with crate clock fanout, and remote monitoring of clock and analog signals. The board is presently in the design and prototyping stage. No design specification document yet exists.

Clock system – There is a 9U double width central distribution module residing in one of the 8 endwall calorimeter crates, and 8 crate transition board distribution modules, one in each endwall calorimeter crate. There exists a schematic for the 9U board, and the transition boards printed circuit boards's have been produced. No design specification or interface document exists. No information was presented about safety, PCB, or grounding reviews for the system.

DeCAF cards – The deCAF cards are daughter boards that are installed on the ADMEM boards. The board is similar in format to a CAFÉ card, but the QIE, current calibration circuits and flash RAM have been replaced with a 12 bit ADC which receives a voltage from a TAC on the transition board. This card is still in the design stage. No design specification document exists.

Low voltage and preamp power – 1 of 2 of these are built, the second and a spare unit will be finished soon.

HV system – 50% of the system is at FNAL, and they are in the process of testing it.

There was one request from the presenters. Mathew Jones will be relocating to FNAL in September 2000, and the request was made that a VME test stand and lab space, preferably close to a magnet, be provided.

Finally, the TOF review committee thanks the CDF TOF team for their presentations and cooperation over the course of the review. We want to commend them on the tremendous amount of work they have done in the 18 months since approval, to get to where they are now.

Comments

Charge 1: Will this design meet its performance goal?

The committee generally felt that from the data supplied it seems like a good possibility, but that there was no real way to know in the absence of a full chain test. Looking at the design of the tube base, pre amp and cable comparator chain we could not say definitely that the statistics of the signal and noise could be controlled to stay under 100 ps jitter. Many believe the 25 ps jitter contribution of the electronics will be hard to achieve, but since a complete prototype system from tube through digitized time has not been assembled, or even completely designed, or in some cases not even prototyped, it is not possible to say for certain whether the specs will or will not be met. A system timing error budget should be produced. The short-term channel-to-channel drift is also a major concern. Limited tests show the parts of the system (tube/preamp/cable) that are built might be OK. Circuits like those that are being proposed for the rest of the chain can meet the specs for the individual components. A high priority should be building a test setup for the full chain - ideally with the magnet on the assembly hall floor. This should be ready so that as electronics prototypes are generated and pass initial bench testing they can be quickly tested in a detector-like environment. For example, the 20mV noise quoted as being observed *in situ* would produce 100ps of timing jitter on a 1V waveform with 5ns rise time. (numbers taken from the status report). The problem of long-term drift correction is not simple but maybe possible. Most felt the hardware that was already in place is first class and carefully thought through.

Charge 2: Manpower

While in general the committee feels the Penn group has the ability to solve the technical issues in designing a suitable system, the committee was divided as to if there is sufficient manpower to address both the transition module and the deCAF card through design, production, and installation in the short time remaining before 1 March 2001. Since we were not presented with a resource-loaded schedule, it is difficult to evaluate whether the personnel levels are adequate. It appears that the basic design, prototyping, and testing is getting done, and Matthew has done a phenomenal amount of work on the preamp, but given the schedule, it is not clear he can do both of these other projects. *In situ* system testing of prototype and production parts should be a full time job for somebody between now and March 1. This system testing will require someone familiar with the DAQ and software, and such a person is not visible in the TOF effort. The transition card is a delicate problem in analog circuitry and the deCAF card requires integrating with the ADMEM. Both of these parts will require extensive testing of both the performance of prototypes and quality of the production boards. Integrating with the ADMEM's also means modifying FPGA code and testing TOF ADMEM's in a crate with standard ADMEM's to see that readout of TOF and WHA are compatible. In short, most felt that adding more manpower there won't help much unless it is expert help which is able to do design work on the transition boards and/or the deCAF cards.

Some members were confused by the status report that shows Penn responsible for the transition board while page 16 of the same report shows Pisa to be working on that project. Others felt that the Penn effort can be adequate if strong (dedicated) help from the Staff personnel of Newcomer and Van Berg is made available. It was felt that Fermilab personnel would be required to help in connecting to the ADMEM cards. It was also recommended that the deCAF design and production might be better assured of meeting the schedule if it was done by adding Fermilab personnel, assuming an engineer of the right qualifications could be found soon.

Also of some concern were that some of the people listed share time with other detector components. Additional effort will definitely be required to get all the boards through production check out, installation, and integration into the data acquisition readout. Significant work will be required on calibration and monitoring software. It is not clear who will do this. The TOF group should have an overall calibration plan and a person (or people) who are primarily responsible for creating and implementing it. There was not enough information about the clock system manpower resources required to make a good judgement about whether it is adequate.

Charge 3: Schedule

As for whether the schedule is plausible, no schedule or list of remaining tasks was presented, although the proponents are working one. So it is difficult to evaluate this. Many technical decisions have to be made correctly, and there is not much time for making and testing prototype versions. The deCAF and transition card designs are not final, and in fact analog circuit prototyping still remains. At least one prototype iteration, if not two, will be required on the deCAF and full transition cards before the production order. Given this, as well as CDF experience with various engineering and vendor delays, many committee members felt that having everything installed and checked out by 1 March 2001 is not likely. It should also be mentioned that some in the committee felt it was possible.

It was also felt that by many that the number of technical details that have not yet been tested poses a serious threat to the schedule. Obviously, when prototypes are available they should be installed on the detector and tested in that environment as soon as practical. Should there turn out to be destructive interference with the endwall or other detector systems, it may be difficult to solve this if it is not discovered until after March 1. Also, if the preamps should require modification this would need to be known early. Prototype orders should be of sufficient quantity to install boards on the detector to properly evaluate performance there. In short, it is unwise to continue system production piece-by-piece, without overall system tests or additional design reviews.

To succeed, some of the tight planning and scheduling that was done for the mechanical installation now must be done for the electronics and software. Even with that, based on the way these things usually go, March 1 will be tough to meet. Given what was (not) presented, the committee felt some kind of follow-up review should be held once a schedule with resources is developed and analog designs with the clock distribution included are completed. We would be better able to answer the questions in the committee charge at that point.

Additional Technical concerns and questions

Transition Modules –

The design uses complicated transition modules that are a problem because of increased power load, ease of access and ease of communication. It would seem prudent, at least in the case of the clock distribution board, to consider just building a full 9U VME module that plugs into the front of the crate. This would, at a minimum, eliminate a special function cable ribbon bus.

Power consumption on the TOF ADMEM transition board should be carefully calculated. The choice of ECL logic, means high power consumption, and there are only 2 pins of +/-5V available, each rated at 1.25 amperes. Access to the transition cards, while better than for the preamps, is still difficult. On the central detector, the only other active components on transition cards are the very robust drivers used for the XFT-COT transition cards. Therefore, some felt that limiting the complexity of the transition cards and having a careful testing and burn-in procedure, one like the ADMEM's, should be considered. A quality assurance plan for the transition modules should be developed.

It is not clear to at least one member of the committee that putting 3 channels on a daughter board for the analog circuitry for the transition modules is the correct design decision. There are significant compromises in making daughter boards. First is that after maximizing signal quality on the nicely impedance-controlled boards, some quality may be lost in the extra board-to-board connection. The ground quality of the signals going from ADMEM to transition to daughter boards can also be degraded. One useful addition to the transition module would be flashRAMs to program the FPGA's. There are other several important issues that must be settled for the transition boards. Can enough current be delivered to each, is the cooling sufficient, and how does it drive the total spec for the new power supply.

The need for an active baseline restoration circuit was not strongly demonstrated. Individual TOF signals are present for perhaps 10ns out of 132, which leaves more than adequate time for complete passive baseline restoration (bipolar shaping with ~50ns recovery time) on every single crossing. This would be simpler and consume less power than active BLR.

ADMEM and deCAF –

Addition of wires to the ADMEM may be necessary for read/write capability through the PO connector. One reviewer noted that there are programmable bits that can be used to fake read and write strobes, and that using those one might avoid customizing the ADMEM's. The ADMEM design group should select optimal placement of wires and pin selection if needed. To minimize, and hopefully eliminate, any major changes of ADMEM programming, data from both the CAFÉ and deCAF should be designed to come off the two types of SIMM modules at the same time. So any fine or course adjustments are best designed into the deCAF module.

There were some doubts about the performance of the single-ended pcb connections between the TAC circuits on the transition cards and the DECAF cards on the ADMEM boards. These lines will receive cross talk from the clocks and from the asynchronous digital traffic from readout. The clocks will be synchronous, so clock transients will not vary from time-bucket to time-bucket, and the overall effect will just be a pedestal shift. The asynchronous digital traffic is a different story.

The deCAF digitizer will be 12 bits, but perhaps only 11 bits of dynamic range are needed. Supposing a full scale signal range of a few volts, one bit out of 11 will correspond to a something like one or two millivolts. High frequency transients at this level may well show up, so the issue may come down to a decision about how much band-width limitation can be tolerated on the DECAF cards. Too little and noise comes in - too much and there is not enough settling time from one bucket to the next.

One member recommended using as large a full-scale voltage range as practical for transmitting signals from the TACs to the deCAF cards. The signals, and the noise they've picked up, would then be attenuated on the deCAF cards before digitization. The ADMEM noise environment CAN be measured on the bench. It is definitely a project, however, since it is just not possible to stick a scope probe on a CAFE card connector on the ADMEM and then look for noise while clocks are running and digital traffic is being transmitted on the backplane because of noise from pickup by the probe cable. This measurement should be done before transition cards and deCAF cards are produced.

It was felt a 'film' of the timing for how the TOF pulse height and time data will be acquired needs to be generated. This should have very high priority. The constraints of already existing boards (ADMEM, etc.) need to be understood well enough to be used as design input by the Penn group, and the design brought back in black and white to FNAL for a discussion with the ADMEM designers to make sure that everything is clear and correct.

Clock System –

The plan to have a single fanout for the TOF clock with returned signals is a good one. However, what is missing is a plan to monitor those return signals. Since one wants tight control over crate-to-crate timing differences, it would seem prudent to monitor the differences. In principle, this could be done with one additional ADMEM with a special transition module. Since the clock fanout cables are dressed locally in the crate, there is not a lot of room. That usually means folding over excess cable. Care should be taken that any bending induced board-to-board timing differences are minimized and as well understood as possible. A detailed clock specification and interface document including timing error budget would do much to allay the committee's concerns.

PMT's, base, preamps, and power supplies –

In looking over the documents on the base and preamp, the only information on testing and burn-in was a 5 min burn-in of the bases. This seems rather minimal. Since the preamps, bases, and connector cards are difficult to reach, they require a high MTBF. There have been many instances in the past where PMT bases have become unreliable over time due the use of small-geometry resistors, metal film resistors, etc. The best defense is a protracted burn in prior to installation. Since this was not possible in this case, it is important to keep the assembled system under HV as soon as possible. Part of the charge was to verify that the system as designed will work reliably. The committee would like more information on the testing of other components. It would be helpful to see what has been done since to validate the system, i.e., has there been a set of PMT's kept at voltage with powered preamps for an extended period of time? Is there a plan to continue such testing for a period of months? Have there been multiple power cycle tests? Since the PMT gain drops by a big factor when the solenoid is turned off, does the system need protection against being turned on at full HV with the beam on and the solenoid off?

There were numerous technical comments about the pmt base and preamp design that are included here, even though those are already built and installed on the detector. A back-terminating resistor (at the cable driving end) might have been very valuable to beat down reflections and system noise. Passive components should have been chosen from manufacturers that had proven records in long-lived PMT bases. The base circuit board layout should be examined in detail to make sure that there were no regions of very high electric field since these can become reliability problems even on coated boards. The PMT sockets and the soldering of pins of the PMT socket should be designed so that it doesn't put excessive forces between pins, since this is another famous way to make phototubes become unreliable over time. Perhaps all of this was done. It is not clear that the PMT output coupling capacitor is large enough—it appears that a significant amount of pulse height might be given away by the value chosen.

The preamplifier seems to have been well designed and executed. There are concerns about noise pickup on the cables between the preamplifiers and the transition boards. It is not known how to calculate this, and it's the one item that can't be tested on the bench. The environmental noise will only be known once everything is installed and the detector is sitting in the collision hall. Preamplifier noise, cable degradation, etc., can be measured on the bench and their effects on the timing performance must already be known. Otherwise, there was nothing in the review about problems with the preamps, and the system as described appears to provide satisfactory noise and rise time performance.

There was a lot of work done on filtering the LV power. E grade supplies were purchased, however, the C and I grade have half the noise output. Why was one of those not chosen? The I grade would run off our clean 400 Hz power, too. Attention should be given to the fusing and safety of the low voltage fanout. The power supplies should be checked to make sure that they don't kick back noise onto the power lines.

Why have the instrumentation amplifiers on the voltage monitor? This means that if the supply fails, the monitor fails but the problem is more difficult to diagnose. The monitor box has high-impedance input, so fuse protection would seem to be sufficient.

One system concern is the introduction of noise into the calorimeter readout boards in the same crate. It would be good to have done tests of as much of the electronics chain as is available in the presence of a noise source like the noise-blaster used for CES readout tests. Alternately, one could inject large optical pulses into a set of TOF PMTs and look for disturbances on the trigger or pedestals of the nearby calorimeters. It would be very unwise to go into production until a full crate interference test has been performed, with all system cables in place on the detector. Another potential place to insert noise is the LV cables, which perhaps should be shielded.

The endwall power supplies must be replaced with higher power units. This could be a non-trivial disruption to activities during the shutdown and sufficient time must be allowed in the schedule for testing to ensure they work as well as the present PEI calorimeter power supplies. Also, given the history of these procurements, sufficient lead-time must be allotted. We do not want to be installing new endwall supplies too close to March 1. The specification and procurement of these should begin immediately.