Chamber electronics Status, Plans, Needs

Sten Hansen and Wu, Jinyuan

Fermilab, PPD/EED

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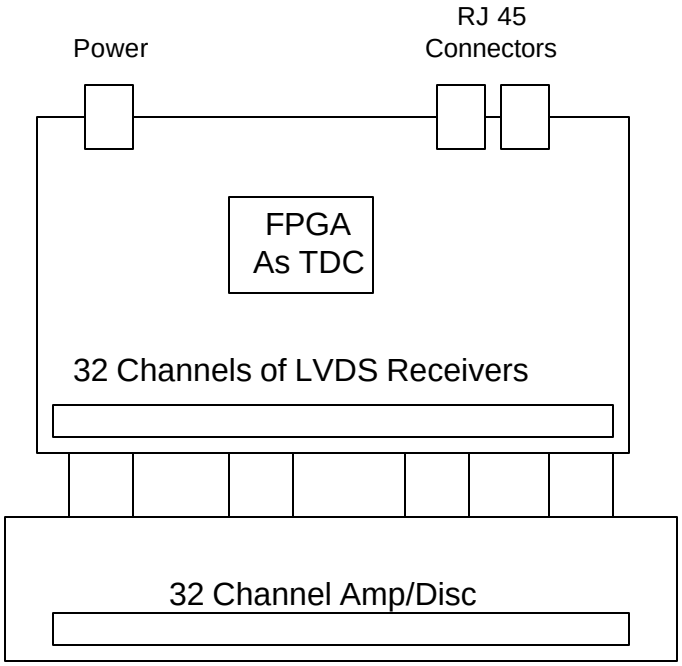
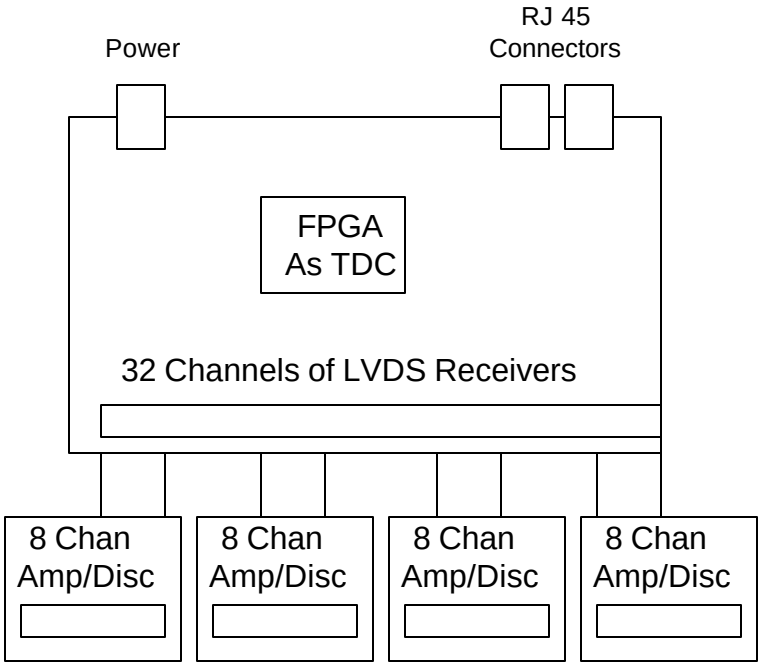
High-Speed Differential Interfaces

"Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic."

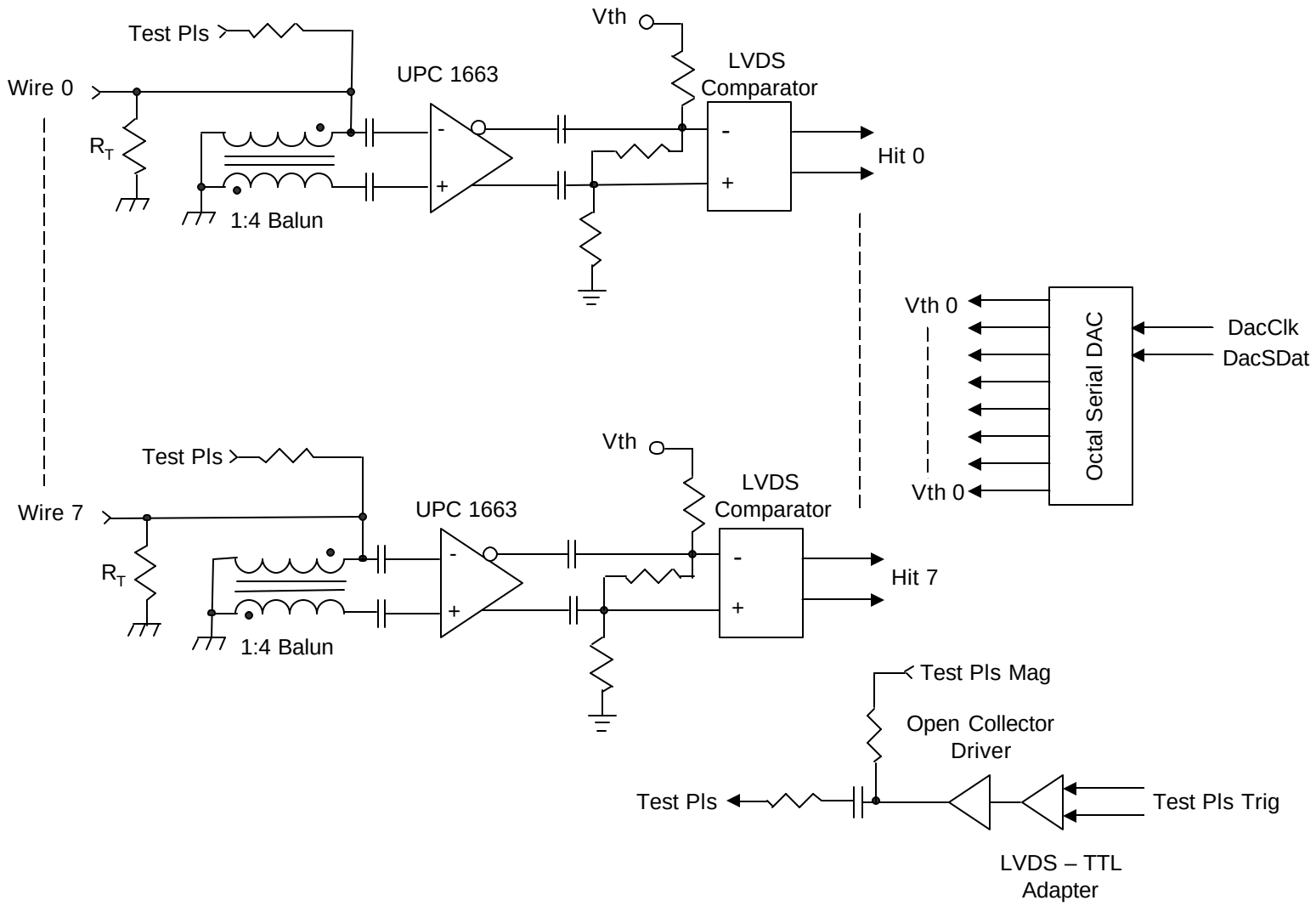
~6000 Channels



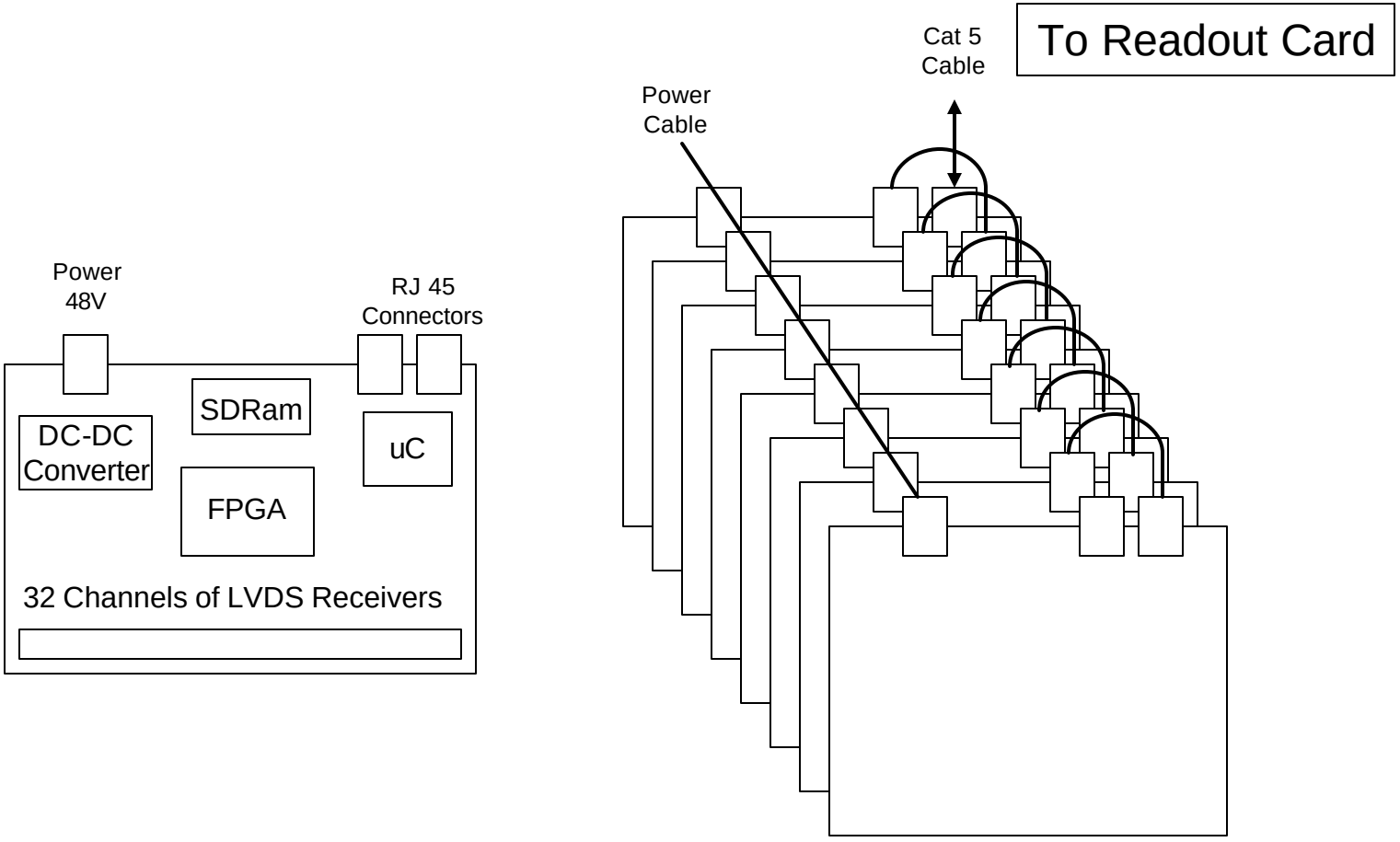
~7000 Channels



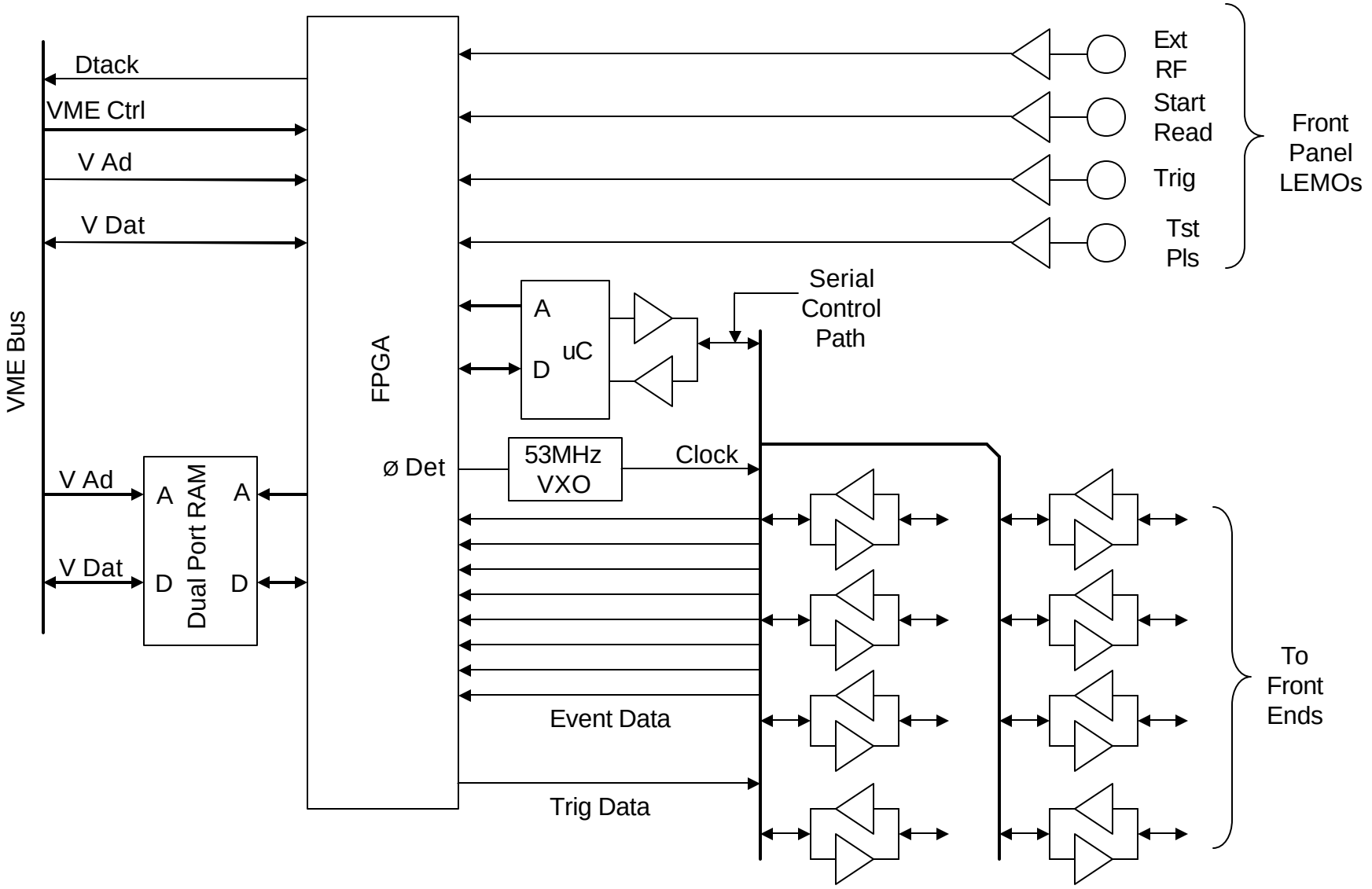
8 Channel Amp/Disc – One per 8 channel Card, Four per 32 channel Card



TDC Card Arrangement

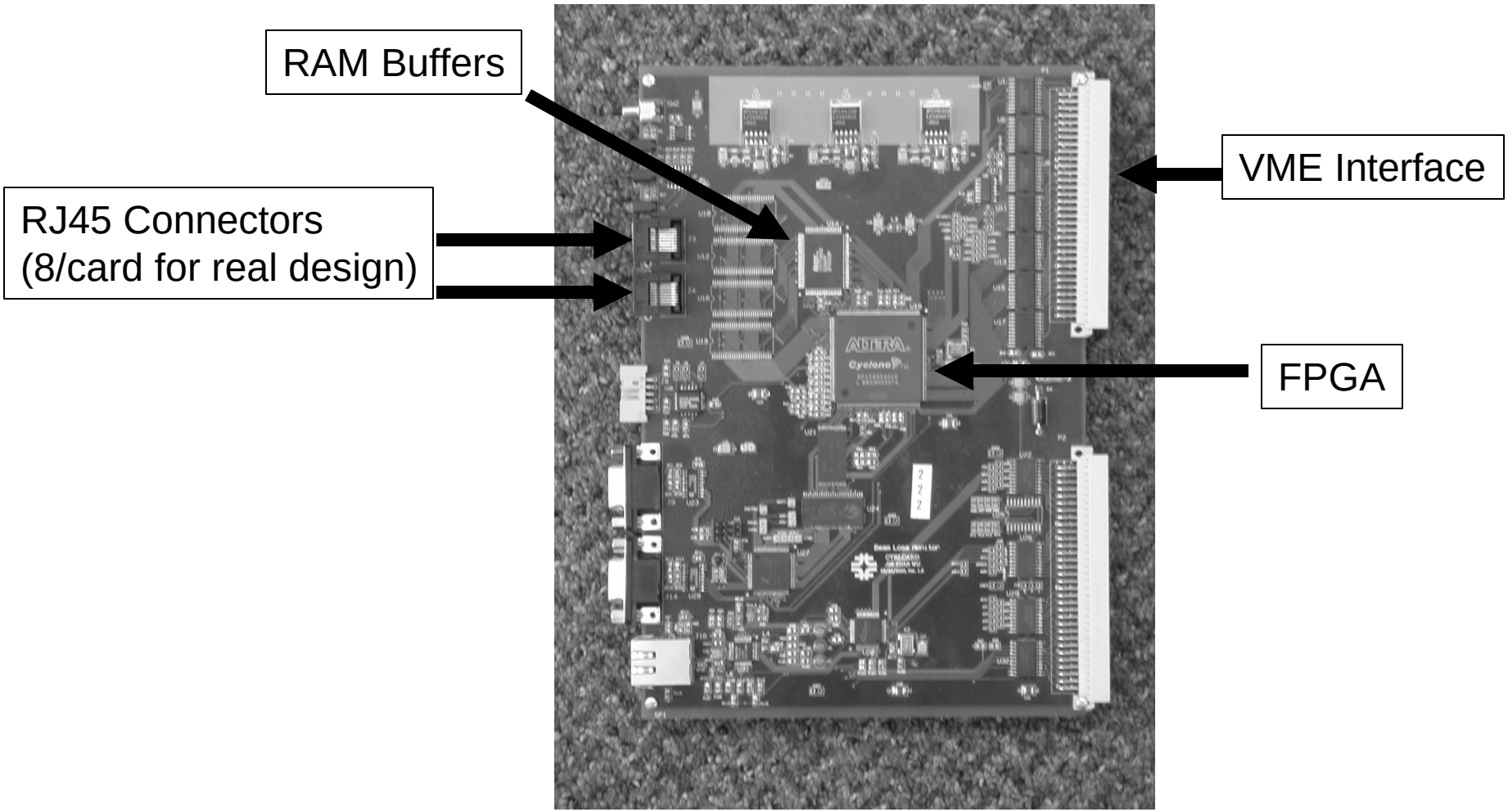


907 TPC/TDC Readout Card Block Diagram

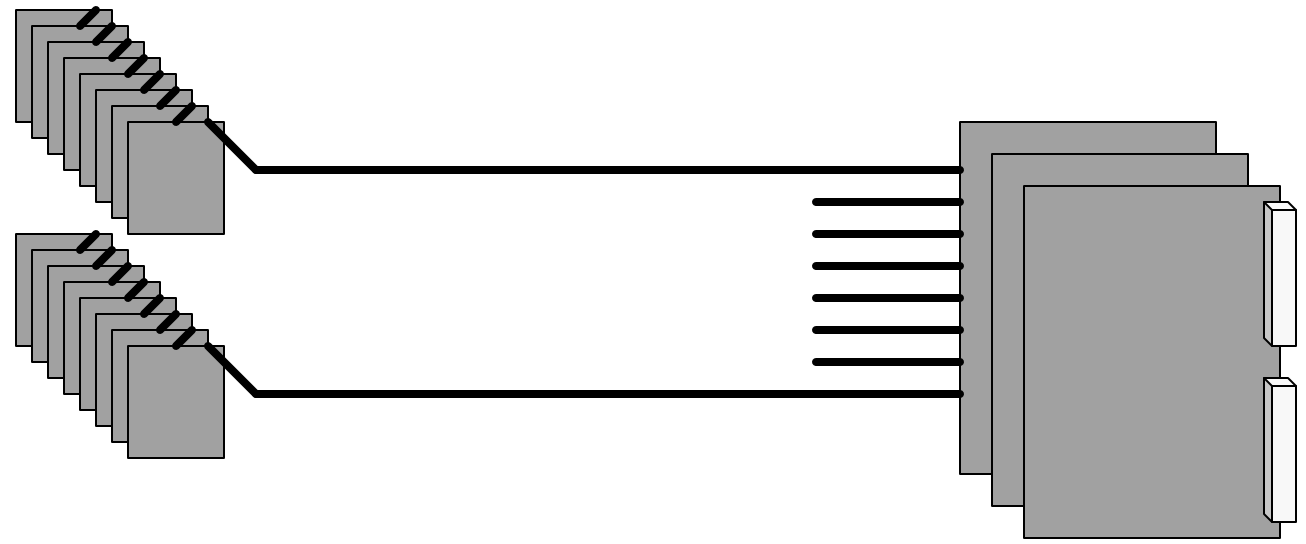


Appearance of Readout Card

Shown here is Fermilab Beam Loss Monitor (BLM) Control Card



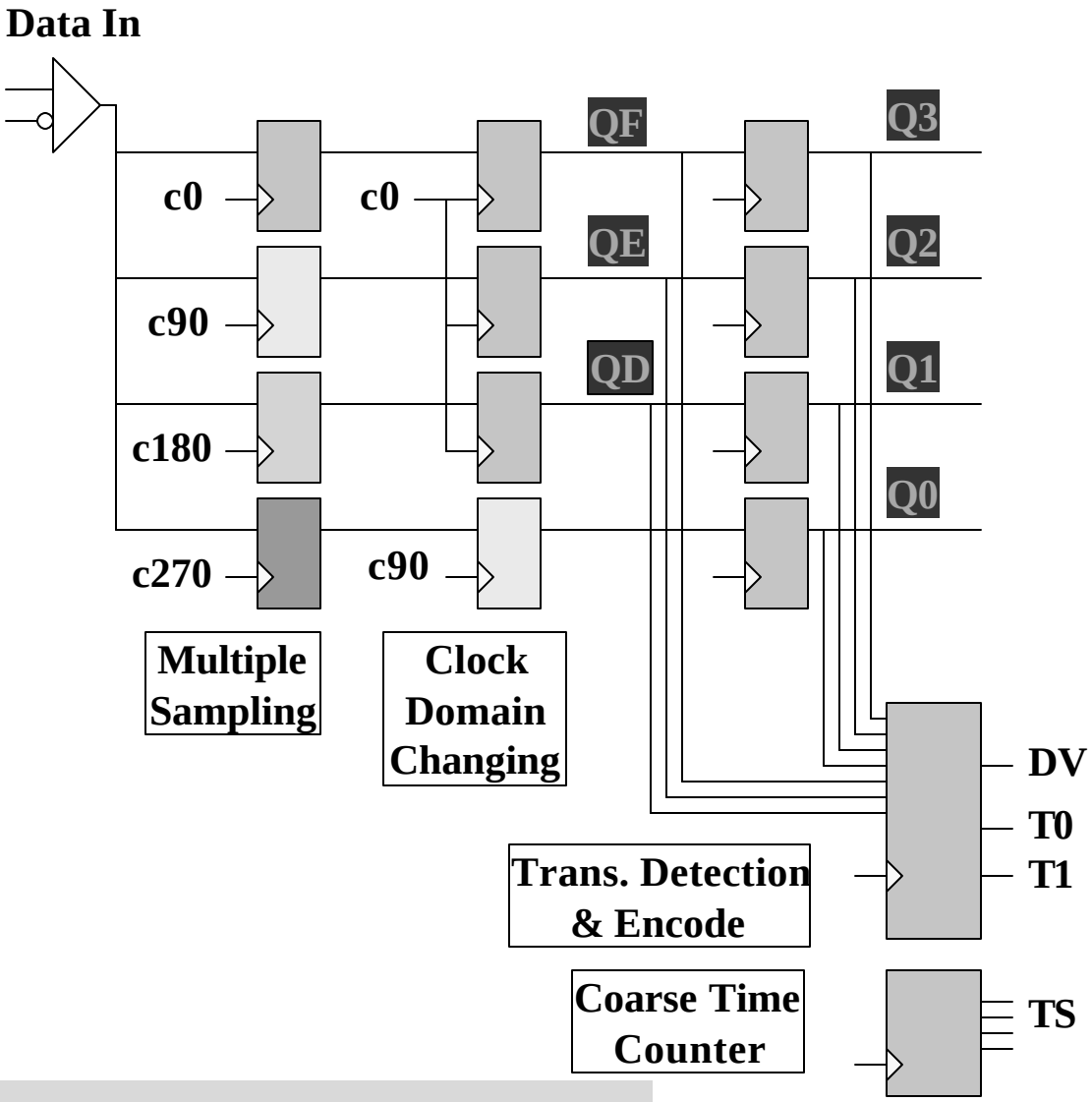
TDC-Readout System

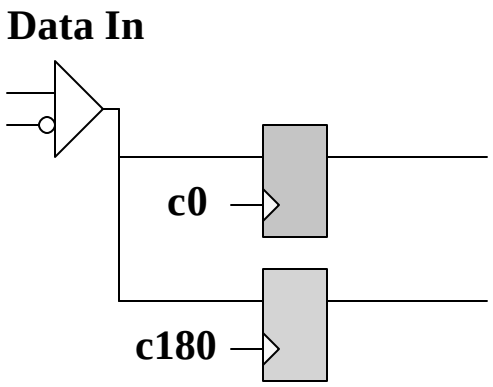


TDC Cards

Readout Cards

TDC Using FPGA (LSB 1ns+-)

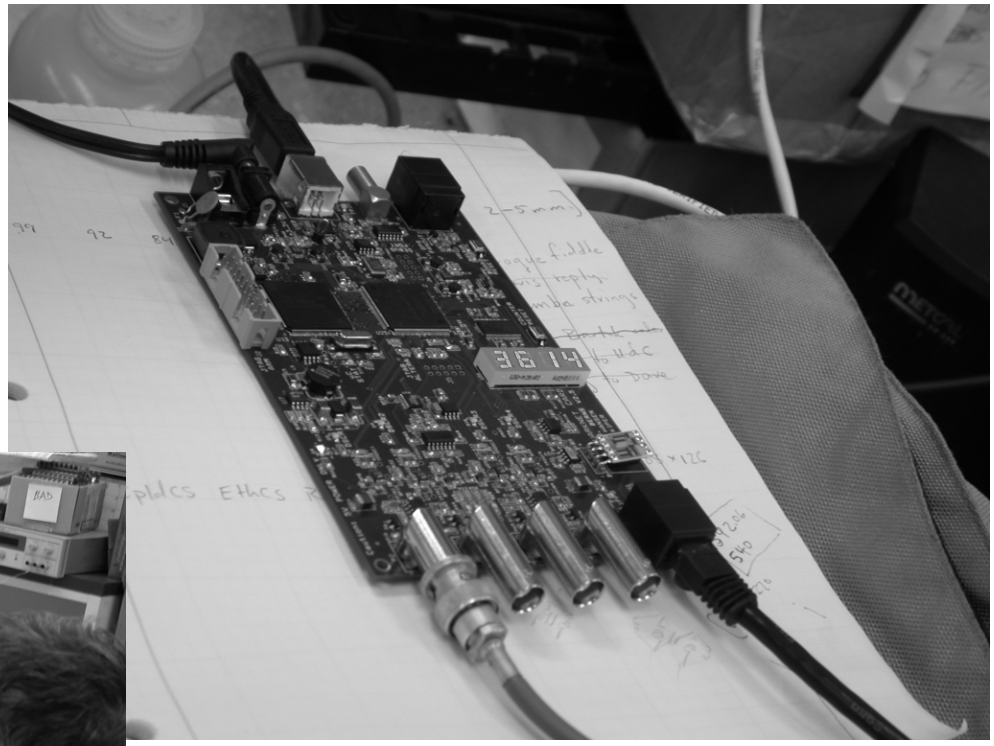




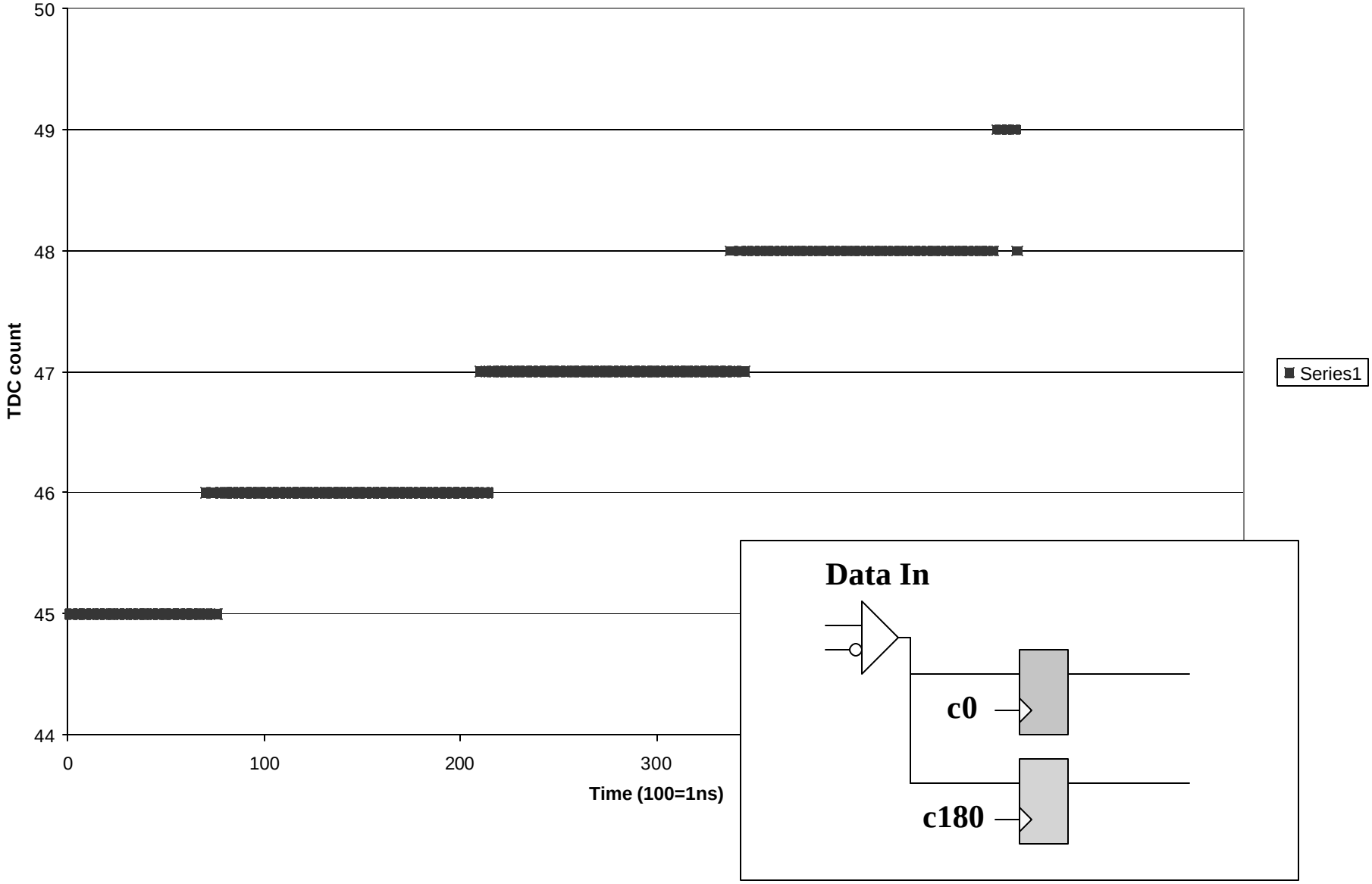
4x Sampling:
250 MHz: 1ns(LSB), 288ps(RMS)
400 MHz: 625ps(LSB), 180ps(RMS)

2x Sampling:
250 MHz: 2ns(LSB), 577ps(RMS)
400 MHz: 1.25ns(LSB), 361ps(RMS)

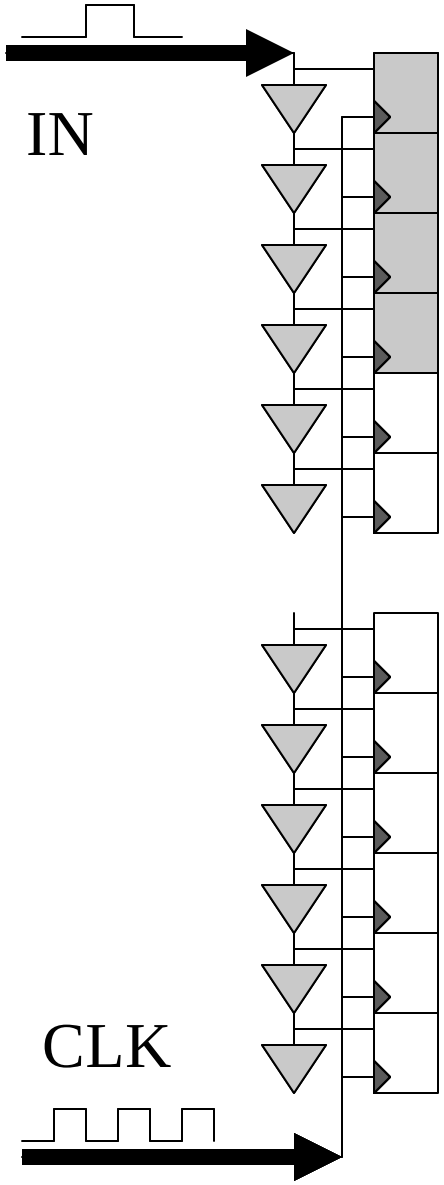
DDR TDC Test Stand



DDR TDC (1.2ns/bin)



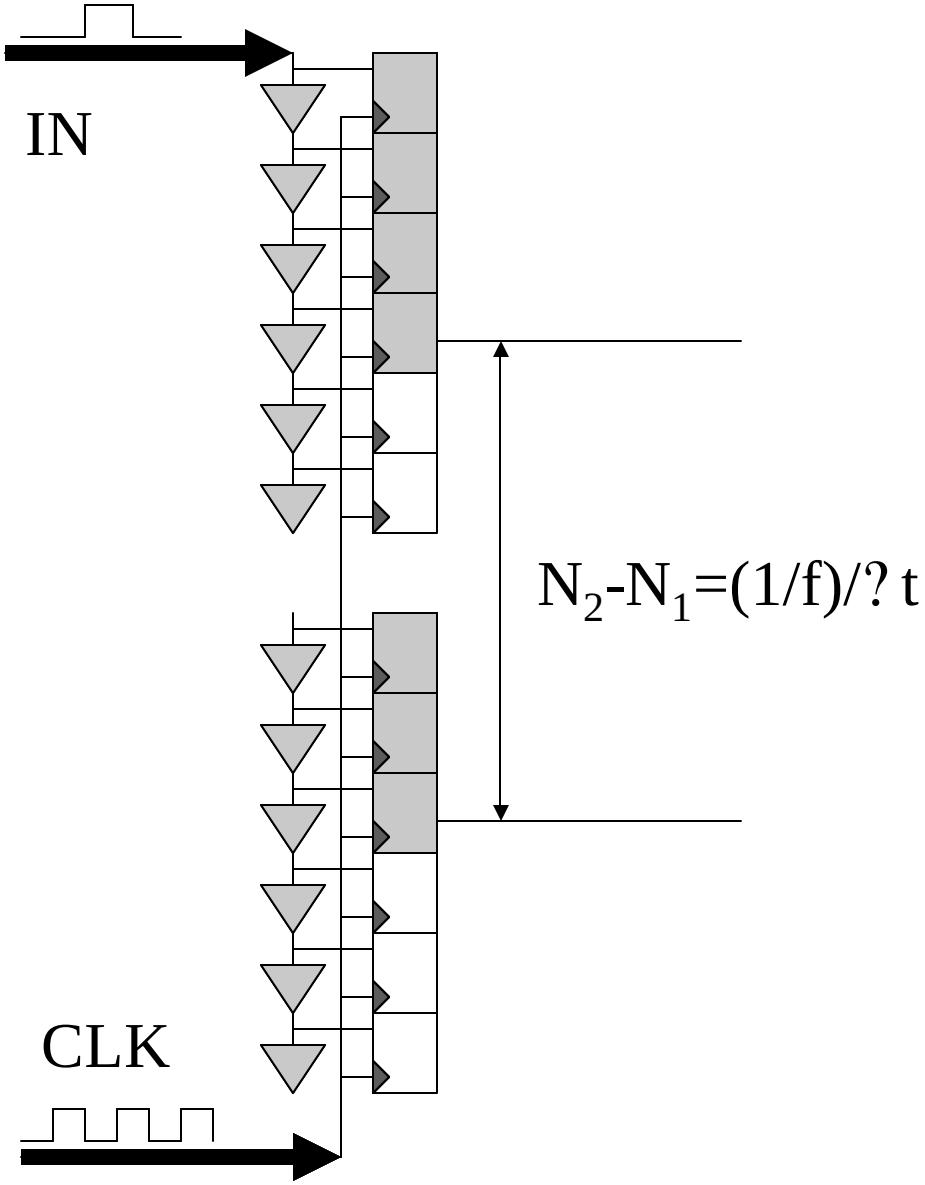
FPGA TDC With LSB < 0.5ns



- This scheme uses current FPGA technology
- Low cost chip family can be used. (e.g. EP1K10QC208-2 $15.25)
- Fine TDC precision can be implemented in slow devices (e.g., 0.4 ns (120ps RMS) in a 200 MHz chip).

This is a 2002 work. To be studied for 2006 devices.

Delay Chain Digital Compensation



- Use longer delay line.
- Some signals may be registered twice at two consecutive clock edges.

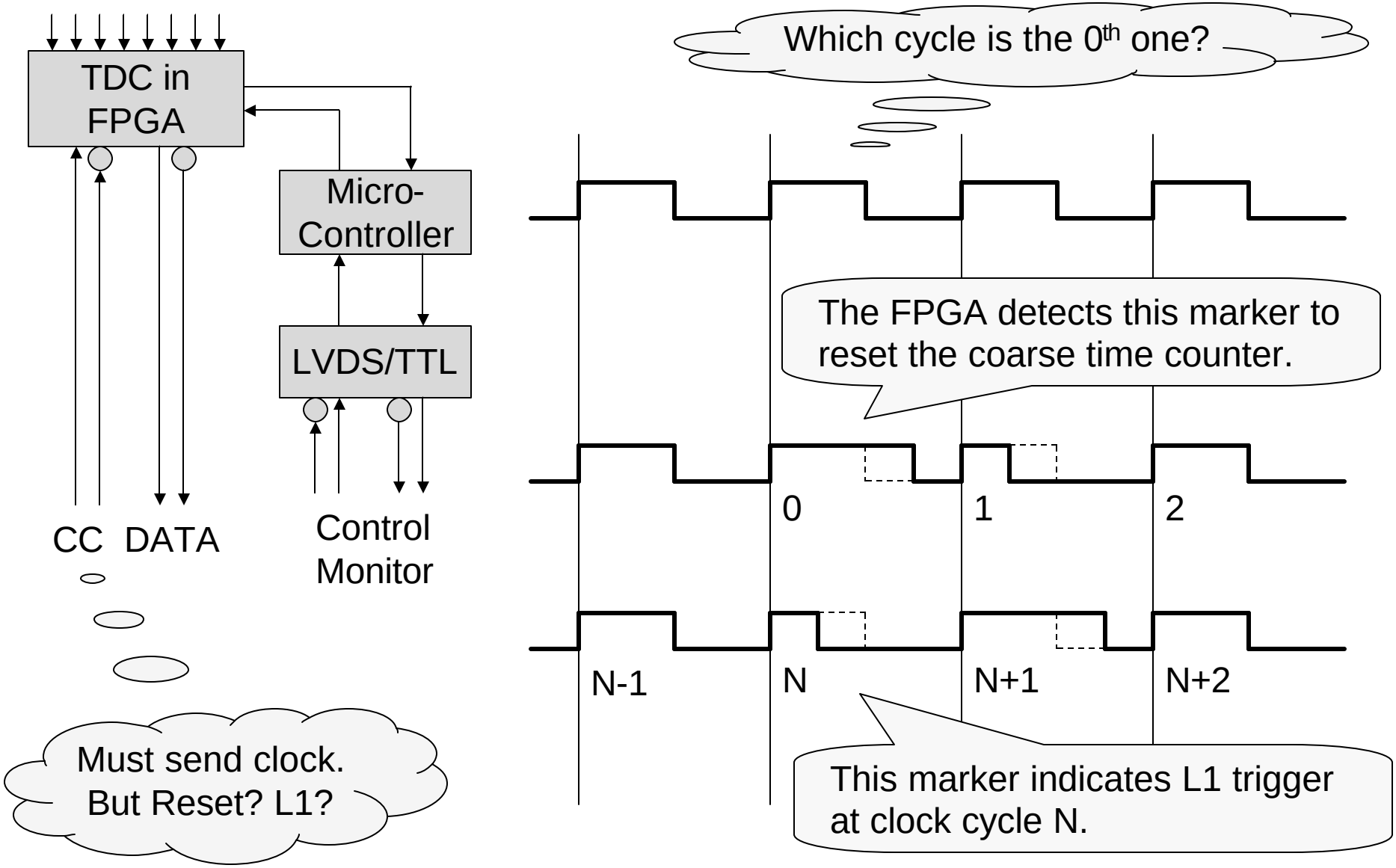
The two measurements can be used:

- to calibrate the delay.
- to reduce digitization errors.

Some Words About FPGA TDC

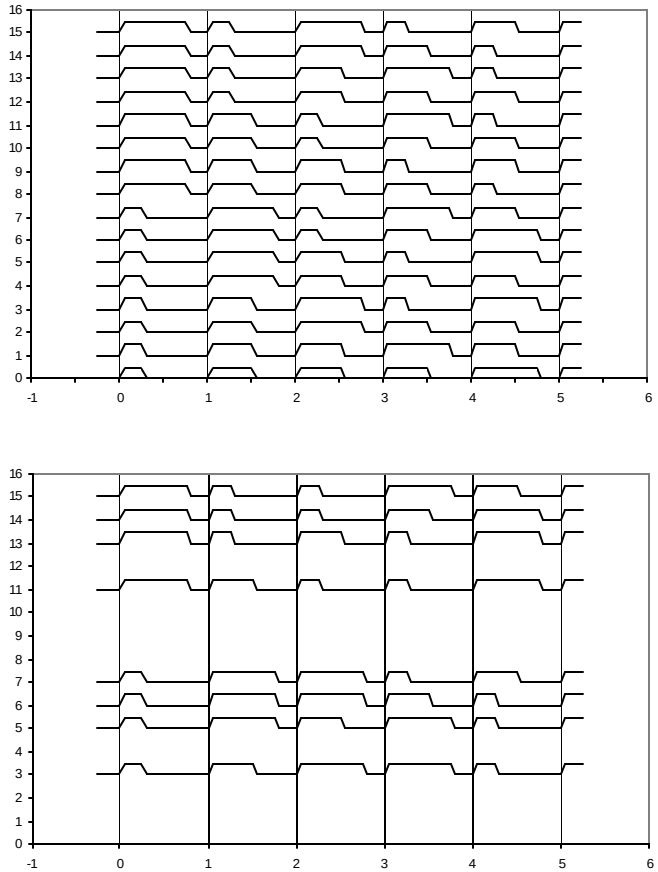
- Many TDC jobs can be done with FPGA purely based on digital process.
- FPGA TDC can be built near the amplifier & discriminator. Timing signals need not to travel in long cable.
- Absolute time is digitized continuously. The timing resolution is factor of sqrt(2) better than in “start-stop” scheme.
- Higher precision (LSB<0.5ns) TDC is possible.

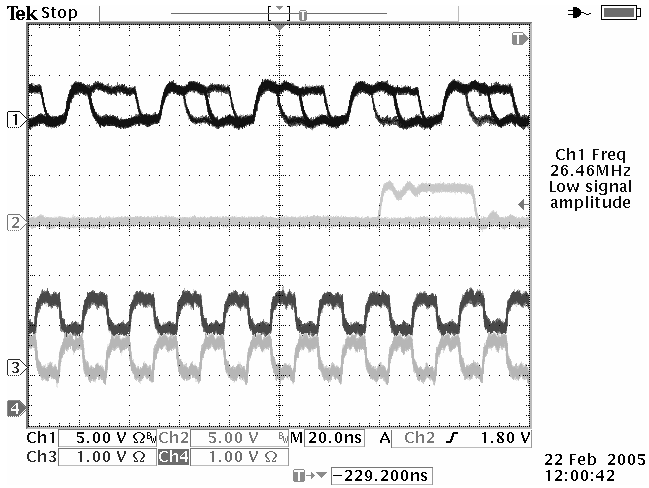
Clock, Reset and L1 Trigger



C5: Clock-Command Combined Carrier Coding

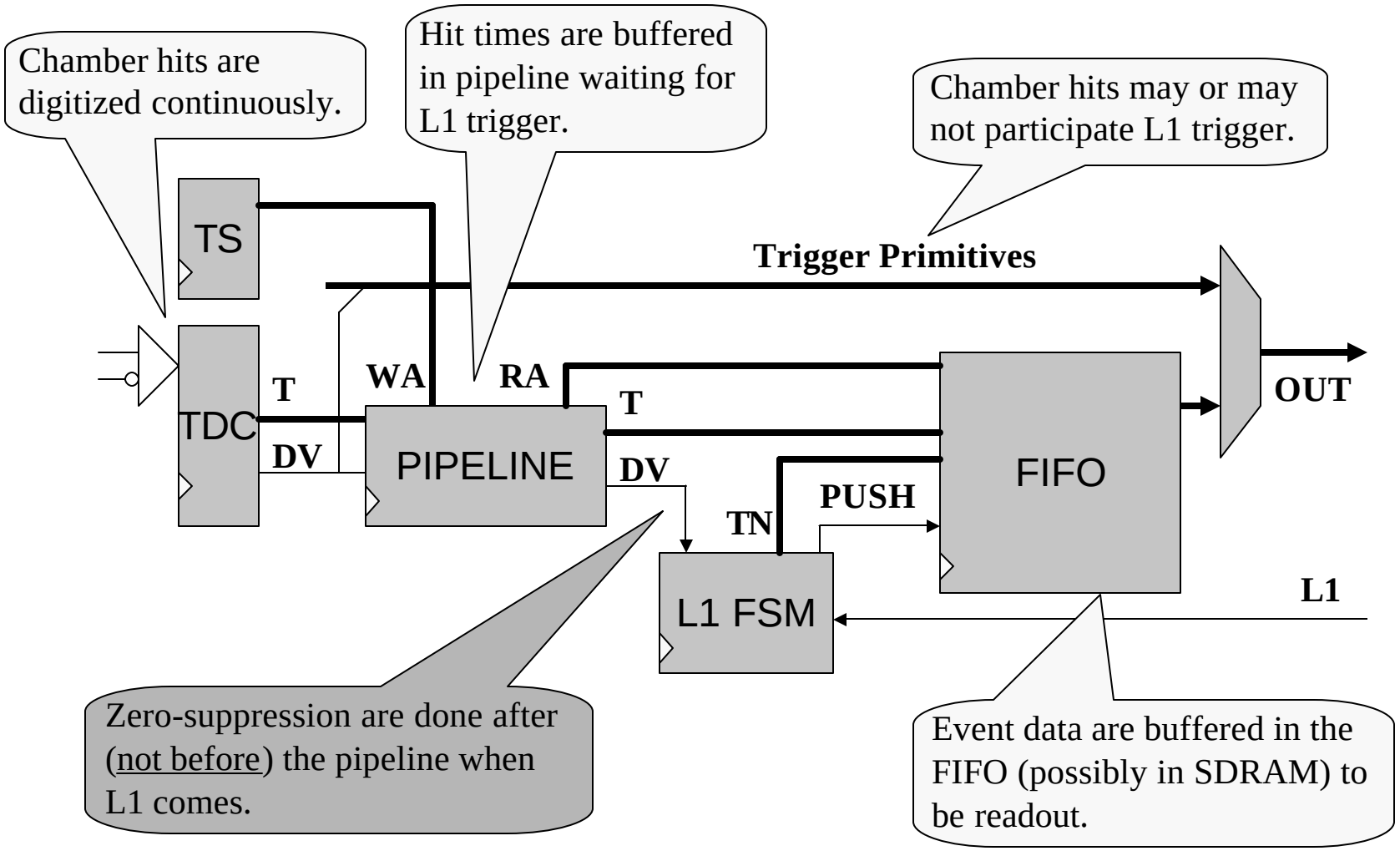
Message can be sent along with clock





Message carried in clock signal doesn't destroy PLL stability

TDC, Pipeline, Zero-Suppression etc.



Summary

- TDC near front-end using FPGA is chosen as basic scheme.
- Appearances of front-end, TDC and readout cards are conceptually known.
- Clock, reset and L1 distribution, zero-suppression scheme and other details are to be determined. But there are sets of standard approaches to choose from.

Beyond

- The TDC-readout system has excessive capabilities. Don’t hastate to ask more if you need.
- TDC: Arrival time + pulse width.
- Chamber info in trigger.