Mark M. Ito
June 15, 1992

Control and Monitoring of Trigger II

1. Introduction

One of the main reasons for rebuilding the E787 trigger is to allow better computer control and monitoring of trigger functions. The new design is Fastbus based and is naturally accessible to the SSP's used in the data acquisition system. This note describes operations that must be performed by the trigger SSP to run Trigger II. In addition, a list of signals suitable for scaling is given.

2. Board ID's

Table 2.1: Trigger II board ID's.

Name	Abbr.	ID
AND/OR board	AO	7871
Sequencer	SQ	7872
Prescaler	PS	7873
R/Z board	RZ	7874
Trigger transmitter	TT	7875
Delay width and fanout board	DWF	787E

Table 2.1 shows the board ID numbers of the new trigger boards. Board ID's are read in bits 16:31 of CSR 0.

3. Initialization

This section describes the registers and arrays that must be downloaded at initialization time.

3.1. Trigger Transmitter

Table 3.1: Trigger Transmitter MLU's. All are in data space. All words are 4 bits wide. Refined range 1 uses data from layers 11, 12 and 13. Refined range 2 uses data from layer 3.

Address	Name	Length (words)
3	Hextant Cut	64
4	L0 Refined Range 1	16384
5	L0 Refined Range 2	8192

Table 3.1 describes the three MLU's of the trigger transmitter. They are loaded with a block transfer to data space. A read back check can be done.

3.2. Prescalers

Table 3.2: Prescaler Registers. All registers are in CSR space. The four addresses indicated are for channels 0, 1, 2 and 3 respectively

Address	Function	Read/Write
C0000000:03	Prescale factor	R/W
C0000008:0B	Input scaler	R
C0000010:13	Output scaler	R
C0000018:1B	Control register	W

Table 3.2 summarizes the registers of the prescaler. Table 3.3 describes the bits of the control register. Initialization tasks are:

(a) the prescaler factors must be loaded (read back check can be done).

(b) Both input and output scalers should be zeroed. Toggle bits 2 and 3 in the control registers.

(c) Input, output, and prescaler counters should be enabled. Turn on bits 1, 4, and 5 in the control registers.

The assignment of trigger types to prescaler channels will follow the level 0 bit assignments in the AND/OR board, as detailed below. The four channels of the first prescaler will correspond to bits 0:3 of the level 0 word, the four channels of the second prescaler will correspond to bits 4:7, *etc.*

Table 3.3: Prescaler control register

Bit	Function	Description
0	Load	Load prescale value from register to prescaler counter. This action performed automatically during each prescale cycle.
1	Enable prescaler	Allows prescaler counter to increment
2	Reset input scaler	Zeros the input counter
3	Reset output scaler	Zeros the output counter
4	Enable input scaler	Allows input counter to increment
5	Enable output scaler	Allows output counter to increment
6	Enable pulser	Use internal clock to produce input pulses.
7	Reset all input scalers	Zeros all four input scalers (address C0000018 only)
8	Reset all output scalers	Zeros all four output scalers (address C0000018 only)

3.3. AND/OR Board

Table 3.4: AND/OR board L1.n association register. High value means that the L1.n requirement will be applied. Write to C0000000. Read back from C0000003.

Bit	Action
0	Apply requirement S to type 1
1	Apply requirement T to type 1
2	Apply requirement U to type 1
3	Apply requirement V to type 1
4	Apply requirement S to type 2
5	Apply requirement T to type 2
6	Apply requirement U to type 2
7	Apply requirement V to type 2
...	...
28	Apply requirement S to type 8
29	Apply requirement T to type 8
30	Apply requirement U to type 8
31	Apply requirement V to type 8

Table 3.4 shows the structure of the L1.n association register. There can be up to four level 1.n trigger requirements, labeled S, T, U and V. These can be applied in any combination to the first eight group A trigger types.

3.4. Sequencer

At power up, the standard clear signal must be reset by toggling bit 2 of CSR 0. Since the clear requires a leading edge, the sequence must set the bit low (write a 1 to bit 18), then high (write a 1 to bit 2), and back low again. The bit can be read back.

Table 3.5: Sequencer group enable register. Adress is C0000001 of CSR space. Read and write. High ⇒ enable.

Bit	Description
0	Enable group A
1	Enable group B
2	Enable group C
3	Enable group D

Table 3.5 describes the group enable register. For normal running groups A, B and D should be enabled. For cosmic running, group C should be enabled.

3.5. Delay, Width and Fanout Boards

Table 3.6: DWF control register. Six channels per board, addresses C0000000:5 in CSR space. Registers are write only.

Bits	Function	Description
0:7	Delay	Sets fraction of full scale for the delay
8:9	Delay Full Scale	Selects the full scale delay.
16:23	Width	Sets fraction of full scale for the width
24:25	Width Full Scale	Selects the full scale width.
30	Inhibit	High ⇒ suppress all output pulses. Also resets output levels.
31	Bypass	High ⇒ operate channel as simple fanout, no delay or width added to pulse.

Table 3.6 outlines the DWF control word. Initialization operations are:

(a) Reset output levels. Toggle bit 30 of all channels.

(b) Load delays and widths.

3.6. IO Board

We would like to reserve 4 bits of the IO board's output port to be devoted to miscellaneous trigger control. These should be operated as levels. The first of these will be used to enable and disable an internal prescaler on the level 0 trigger boards.

4. Read Out: Events

Much of the trigger information that was previously read out through IO boards is now available directly from the trigger boards where it is used. This sections describes trigger data that should be read out every event.

4.1. R/Z Board

Table 4.1: Contents of R/Z board register C0000000, CSR space. Signals are hit range stack layers. CT refers to the charged track gate. Signals are ungated unless otherwise indicated.

Bits	Signals
0	T+2+...+8
1:3	9, 10, 11
4	12+13+14
5	15+16+17+18
6:8	19, 20, 21
9:27	$3{\cdot}$CT,..., $21{\cdot}$CT

Table 4.2: Contents of R/Z board register C0000001, CSR space. FTDC results consist of 6 bits. From LSB to MSB they are: 4 bits of z information, 1 sign bit and an OK bit. There are FTDC's on layers 3, 11, 12 and 13.

Bits	Signals
0:5	FTDC layer 11
6:11	FTDC layer 12
12:17	FTDC layer 13
18	sign bit only, averaged L0Z(1)
19	sign bit only, FTDC layer 3
21	OK bit only, FTDC layer 3

The R/Z Board latches information in two registers for read out every event. Table 4.1 and Table 4.2 show the contents of these two registers. Most of the signals read out are also put on the trigger bus. Layer-by-layer hit information, both gated and ungated by a charged track, and FTDC outputs are recorded in these registers.

4.2. Trigger Transmitter

Table 4.3: Contents of trigger transmitter register C0000000, CSR space.

Bits	Description
0:5	Input hextant bits
6:9	Number of target elements
10:14	Stopping layer bits
15:19	Averaged L0Z(1) bits
20:23	z information only, FTDC layer 3

Table 4.4: Contents of trigger transmitter register C0000001, CSR space.

Bits	Description
0	Hextant cut decision
1:3	Stopping hextant
4:7	L0 refined range 1 decisions
8:11	L0 refined range 2 decisions

Table 4.5: Contents of trigger transmitter register C0000002, CSR space.

Bits	Description
0:25	External conditions

There are three registers on the trigger transmitter that should be read every event. They are described in Table 4.3, Table 4.4 and Table 4.5. They contain information about the inputs and outputs of the MLU's and the value of external conditions. Many of these signals also appear on the trigger bus.

4.3. AND/OR Board

Table 4.6: Contents of AND/OR Board Level 0/Level 1 register, address C0000001, CSR space. All entries refer to group A triggers. Level 1 decisions refer to level 1 decisions alone, not in coincidence with level 0.

Bits	Description
0:15	Level 1 decisions
16:31	Level 0 decisions

Table 4.7: Contents of Contents of AND/OR Board Level 1.n return code register, address C0000002, CSR space.

Bits	Description
0:3	Return code from L1.n requirements S, T, U and V

The AND/OR board gives the results of all group A trigger types for level 0 and level 1, and the return codes from the level 1.n requirements. The information is contained in the two registers described in Table 4.6 and Table 4.7.

4.4. Sequencer

Table 4.8: Contents of Sequencer trigger status register. Address is C0000000, CSR space.

Bits	Description
0:3	Level 0 passes, groups A, B, C, D
4:8	Level 1 passes, groups A, B, C, D
16	Level 1 fail
17	Level 1 pass
20	Level 1.n done
21	Level 1.n fail
22	Level 1.n pass pulse
23	Level 1.n pass level

The sequencer status register tells which groups passed level 0, which passed level 1, and also reports the status of various internal signals of the sequencer. It is described in detail in Table 4.8. The internal signals should be checked against a standard pattern since they will be the same for every event if the trigger is working properly.

4.5. IO Board

Table 4.9: Assignment of bits in the trigger IO board.

Word	Bits	Description
0	0:15	B group trigger types
0	16:31	C group trigger types
1	0:15	D group trigger types

The IO board will contain the results of groups B, C and D triggers. The bit assignments are shown in Table 4.9

5. Read Out: End of Spill

Upon recognizing an end-of-spill trigger, the trigger SSP should read all input and output scalers from the prescalers.

6. Scaler Channels

Table 6.1 shows signals which should be input to scalers.

Table 6.1: List of trigger signals for scalers.

Signal	Board	Connector, Pair
T·2's	RZ	J6, 16
Level 1.n fail	AO	J3, 14
Level 1.n done	AO	J3, 16
Level 1 pass, indiv. grp. A, types 1-16	AO	J4, 1-16
Level 1.n fail, indiv. grp. A, types 1-8	AO	J5, 1-8
Level 0 pass, total grp. A	AO	J5, 10
Level 1 pass, grp. A, total of types 1-8	AO	J5, 12
Level 1 pass, grp. A, total of types 9-16	AO	J5, 14
Level 0 pass, all groups	SQ	J3, 4
Level 1 pass, all groups	SQ	J3, 8
Standard clear	SQ	J3 14
Beam strobe	SQ	J4, 6
Detector strobe	SQ	J4, 12
SSP start	SQ	J4, 16
Level 1.n clear	SQ	J5, 4
Gate fault	SQ	J5, 12
SSP start fault	SQ	J5, 16