TITLE: Reliability of Cu-Based Microelectronic Metallization Systems, #18

PROPOSING CENTER: JPL

PARTICIPATING CENTER: GSFC

PROJECT: Electronic Parts

POINTS OF CONTACT:

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OBJECTIVES:

Assess failure mechanisms of Cu-based metallization and low-permittivity dielectric interconnect systems through collaboration with industry and experimentation. Provide recommendations for use and application of these new metallization systems in high reliability systems.

BACKGROUND:

Ever larger and faster microelectronic circuits ("ULSI") require the development of on-chip interconnect systems with high electrical conductance and low inter-level capacitance. According to the "National Technology Roadmap For Semiconductors 1997" of the Semiconductor Industry Association (SIA), high-profile copper line/plug metallization compatible with a low-permittivity dielectric ($\kappa = 3.2 – 2.5$) will be in the preproduction phase 1999-2001. The interest in Cu results not only from its higher electrical conductance in comparison to aluminum, but also from its higher resistance to electromigration and from its low cost in comparison to gold. Dielectrics with a lower permittivity than silicon dioxide include, in the indicated range, fluorinated silicon dioxide and polyimide. However, these new material systems pose a variety of new problems including adhesion, interdiffusion, corrosion, electrical leakage, and thermal stability. Nevertheless, beating the SIA plan, IBM introduced in September 1998 copper-based PowerPC microprocessors on the commercial chip market and announced plans to offer its copper metal interconnect process to other companies as part of its silicon foundry services in 1999. Motorola, with its own Cu-process, has teamed up with AMD to produce microprocessors.

APPROACH:

In this effort, we propose to investigate the new Cu-based metallization systems and identify reliability and lifetime limitations critical to application of these devices in high reliability systems. The investigation will include collaboration with industry personnel, whenever feasible, and test and characterization of devices and available test structures for stability, diffusivity effects, electro and electrochemical migration, thermal characterization, electrical leakage, and other characteristics to establish reliability and determine common failure mechanisms for this metallization system. Together with CISM, we have contacted representatives of Intel, Applied Materials, IDT, Motorola, IBM, and Novellus to form a Cu-Metallization Reliability Consortium to investigate reliability and stability issues relating to this technology and its applications in high reliability systems. CISM will also contribute in-house copper samples with superior properties.

All data, test reports, and publications will be disseminated to the NASA and industrial community via suitable technical publications, NASA technology reports, and made available on the NEPP homepage.

BENEFITS:

The results of this work will benefit device users, designers, and manufacturers by providing data useful for process and design improvement. It will also provide stability and lifetime expectancy data critical for long-term application users. Infusion of this new technology will reduce dynamic electrical losses in integrated circuits compared to equally sized Al-metallization or will allow to reduce size. The deposition techniques for copper are very efficient and will, together with the low cost of the material in comparison to gold, lower costs for fast integrated circuits. This joint proposal with GSFC will benefit the NASA community in the areas of Codes S, Y and M.

DELIVERABLES:

1. Report of expected failure modes and mechanisms for Cu/ low-κ interconnect systems
2. Experimental results and data.
3. Thermomechanical simulation [GSFC]
4. Final report including recommendations for application of these materials in high reliability systems.

PARTNERSHIPS:

We will form the following partnerships:

Center for Integrated Space Microsystems…………..…Cu deposition, diffusion barriers
GSFC……………………………………………………thermomechanical simulation
Lloyd Technology Inc………………………………… electromigration consultation
NIST/University of Maryland at College Park (UMCP)……….electromigration testing
California Institute of Technology………………thermomechanical parameter extraction
Applied Materials, IDT, Intel, IBM, Motorola, Novellus………..…test samples and data

Substantial leverage is obtained through these partnerships in sharing fabrication, test equipment, and simulation software.

ENDORSEMENTS:

Mars Exploration Program (Code S & M)………….…….see letter by Frank Jordan/JPL
New Millennium (Code S)……………………………....see letter by Chuck Minning/JPL
Center for Integrated Space Microsystems (Code S)...see letter by Elizabeth Kolawa/JPL

SCHEDULE:

1FY00	Process information, sample, and data collection from vendors
2FY00	Report of expected failure mechanisms Test and experiment setup
3FY00	Adhesion, leakage, corrosion experimentation
4FY00	Thermal stress analysis [GSFC] Evaluate data and write intermediate report
1FY01	Electromigration experiments
2FY01	Long-term reliability test
3FY01	Data analysis
4FY01	Final report and recommendations