QIE7

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The QIE7 chip for MINOS is a modification of the QIE5B6 chip which was produced in 1995 and used in the KTEV experiment. For information on QIE5B6 operation, see "A Second Generation Charge Integrator and Encoder ASIC" in the 1995 IEEE NSS Conference Record pp. 280-284, and " A High Speed, Wide Dynamic Range Digitizer Circuit for Photomultiplier Tubes" in NIM A 360 (1995) 150-152.

Unfortunately, detailed documentation and schematics for QIE5B6 are not available. A QIE5B6 pinout description does exist which identifies the functions of all the pins and the external connections which are required to operate the chip. Documentation for QIE7 will therefore consist of a list of changes implemented, and an updated pinout description. Actually, two prototype versions of QIE7 are being produced, which will be referred to as QIE7A and QIE7B. QIE7A has a "minimum" set of changes which were requested by MINOS, and QIE7B has a " maximum" set of changes which consists of the QIE7A changes plus a completely redesigned input amplifier.

Minimum set of changes implemented (QIE7A):

1. Adapt the design for operation with positive supplies only. QIE5B65 nominal supplies are –6.5V, GND, and +5.5V. Nominal QIE7 supplies are GND, VSS (6.5V), and VDD (12V). VDD should be formed from a 5.5V supply which is referenced to VSS. **Note**: it may be possible to run VSS at a somewhat lower level depending on the maximum input current which must be accepted. This will have to be tested on the prototype chips. In any case, VDD should always be 5.5V above VSS.

2. Convert the clock and reset inputs to LVDS. This involves implementing a differential receiver and also performing an internal level shift since the digital rails on the chip are nominally 6.5V and 12V.

3. Modify the digital output circuits (exponent and cap ID). This involves an internal level shift, again because of the digital levels. The digital outputs are differential "open collector" and switch a constant current from one side to the other (the value of the current is set externally), as with the QIE5B6. However, since QIE7's most negative supply is ground, the output common mode must be above ground. Typically the external termination resistors should be tied to 2V. This sets the common mode level at somewhat higher than nominal LVDS, but still within the acceptable range of LVDS operation.

4. Convert the analog output to a simple differential output (2 pads). Each side has approximately 350 ohm output impedance, and therefore must be immediately

buffered externally. (In contrast, QIE5B6 has 4 analog output pads for immediate connection to an external opamp, so that the opamp gain setting feedback network can be internal to the QIE chip).

5. Add diode protection to input. QIE5B6 has no internal diode protection for negative input signals since it is designed to accept up to 50 mA peak current, which puts the input voltage at more than a diode drop below the lowest supply. Since MINOS specifies 20 mA peak input current, internal protection is used. Assuming 50 ohm input impedance, the protection diode will not begin conducting until the input current is greater than about 30 mA.

6. Remove 4 of the 7 NPNs in each current limit circuit in the splitter outputs, since peak input current is only 20 mA.

7. Modify the RFSEL circuit, which scales the DC input bias current for operation at a different crossing frequency. On QIE5B6, the RFSEL pin accepts a digital level between VSS and VDD, and selects for operation at RF (53 MHz) or RF/4 (13 MHz). The QIE7 RFSEL digital input level is 0-5V (not VSS-VDD), and it selects between RF and RF/2 (26 MHz).

Additional changes implemented for QIE7B:

8. Replace the input amplifier with a new design which has a more constant resistive input impedance. This design requires an external resistor in the input signal path which sets the input impedance for large input currents. The impedance at low input currents is determined by the amplifier bias current (NOT the input bias current). The QIE7B pinout and bias requirements are different than QIE7A.

9. Remove the range select feature (fixed/auto range). Fixed range operation is not a desired feature of QIE7, and removing this feature frees up 4 pads which are needed for the new input amplifier. QIE7 will automatically autorange.

QIE7A PINOUT DESCRIPTION

Note: Pin 1 is labeled on the chip in metal2, and numbering proceeds counterclockwise.

1. VBCAS: Cascode bias voltage, generated internally. Bypass required, however, trace length is not critical. Voltage level is typically VSS-0.8V.

2. VCADJ: Charge compensation vernier. Internally biased to VSS-1V, input impedance ~ 20K. Can be varied between VSS-1V and VDD to adjust charge compensation to required value. (For minimum compensation, VCADJ=VDD). If compensation adjustment is desired, provide selectable external resistance to VDD. No bypass required.

3. VCS1: Charge compensation select #1. Internally biased to VSS-1V, input impedance ~ 20K. Leave unconnected for nominal compensation range; connect to VDD for a discrete reduction in compensation level (~35%).

4. VCS2: Charge compensation select #2. Internally biased to VSS-1.5V, input impedance ~30K. Leave unconnected for nominal compensation range; connect to VDD for a discrete increase in compensation level (~50%).

5. INREF: Reference input. Can be left unconnected. However, for maximum noise rejection, the reference input should look as identical as possible to the signal input (INSIG). Nominal voltage level = 1V.

6. IBFE: Front end feedback amplifier bias current set, nominally –300 uA. The IBFE voltage level will be approximately VSS-4.5V (at -300 uA). Use a resistor to GND to set the current. Bypass not required.

7. GND1: Ground supply for front end amplifier/splitter section.

8. VSS1: Supply voltage for front end amplifier/splitter section. Nominally 6.5V, but hopefully can be as low as 5.0V since peak input current is only 20 mA. Bypass required??

9. INSIG: Signal input. Nominal voltage level = 1V.

10. IBIN: Input splitter DC bias current set. For a 53 MHz clock, the bias current should be +100 uA. Set with an external resistor (IBIN voltage is approx. 2.6V).

11-14. RS3-0: Digital range select bits (RS0 = LSB). Digital input levels are VSS and VDD. Each bit is internally weakly pulled high to VDD. If all bits are high, the QIE will autorange. To force the QIE to read out on only one range, set the desired range with RS0-2 (000 – range I/2, 111 = range I/256). RS3 has no function in QIE7 and should be left unconnected.

15. RFSEL: RF/2 clock frequency select. Internally pulled weakly low. Setting RFSEL high (5V) divides the input splitter DC bias current set by IBIN by two, allowing the clock frequency to be a factor of two slower without physically having to change the IBIN set current. This allows operation to be switched between RF and RF/2 with only one external bias set current.

16. ASUBS: Analog substrate connection. Connect directly to ground.

17. VREFN: Reference voltage used in conjunction with VREFP. This sets the range switch points. The value of (VREFP – VREFN)/2 determines the analog output voltage span. For example, if VREFP – VREFN = 2V, then this forces the QIE to switch ranges whenever SIGOUT becomes 1V more negative than REFOUT. In other words, (REFOUT – SIGOUT) is always between 0 and (VREFP – VREFN)/2. VREFN should be generated with respect to VSS and should be no more than 2V below VSS. VREFN should be driven by a low impedance voltage, since it draws approximately 2 mA.

18. VREFP: Reference voltage used in conjunction with VREFN to set the range switch points. Connect directly to VSS.

19. IBDIG: Digital output current set. Sets the current magnitude which is switched between output and output complement at the differential current mode digital outputs. The set current into IBDIG is approximately one third of the current which will be sunk at the digital outputs. For example, to sink an output current of 2 mA, +0.67 mA should flow into the IBDIG pin. The voltage at IBDIG for an applied current of +0.67 mA is approximately 1.3V.

20. VBLAD: Internally generated bias voltage used for the capacitor reset voltage ladder. Bypass required; place capacitor as close as is practical. Voltage level is typically (VDD – 1.5V).

21. AVDD1: Analog supply voltage, +5.5V with respect to VSS. Bypassing not critical – run to closest AVDD bypass.

22. EXP0*: Digital exponent output bit 0 complement.

23. EXP0: Digital exponent output bit 0 (LSB).

24. EXP1*: Digital exponent output bit 1 complement.

25. EXP1: Digital exponent output bit 1.

26. EXP2*: Digital exponent output bit 2 complement.

27. EXP2: Digital exponent output bit 2 (MSB).

28. CAPID0*: Cap ID bit 0 complement.

29. CAPID0: Cap ID bit 0.

30. CAPID1*: Cap ID bit 1 complement.

31. CAPID1: Cap ID bit 1.

32. GND2: Ground for digital output buffers.

33. AVDD2: Analog voltage supply for analog output buffers, 5.5V with respect to VSS. Bypassing is critical – connect to high frequency bypass capacitor (.1uf) with as short a trace as possible.

34. GND3: Ground for the analog output buffers.

35. N/C

36. N/C

37. SIGOUT: Analog signal output. As input signal magnitude increases, SIGOUT goes more negative. Output impedance = 350 ohms. The signal span is from Vrefout to [Vrefout – (VREFP – VREFN)/2] for each of the 8 ranges. The voltage output level is approximately centered around VSS.

38. N/C (Diepad): This chip pad can be connected to the package die pad if desired. However, the corresponding package pin will not be connected.

39. REFOUT: Reference signal output. Output impedance = 350 ohms.

40. IBOUT: Analog output amp output bias current set, nominally +650 uA (voltage is approximately 1.8V).

41. IBOA: Analog output amp bias current set, nominally –200uA (voltage is approximately VDD – 1.5V).

42. IBPED: Analog output amp pedestal adjust, 0 to –400 uA as required. Increasing IBPED causes the analog output pedestal (SIGOUT – REFOUT for zero input signal) to go more negative. The voltage is (VDD – 1.5V) for IBPED = -200 uA.

43. VBCSD1: Internally generated bias voltage for current switch drive circuit. Bypass is required – place capacitor as close as is practical. Voltage is VSS – 0.7V.

44. VBCSD2: Reference for current switch drive circuit. Must be connected directly to VSS.

45. DVSS1: Digital VSS. As explained earlier, VSS may be as low as 5.0V, or may need to be as high as 6.5V. Bypassing???

46. DVDD1: Digital VDD. As explained before, VDD is +5.5V referenced to VSS. Must be well bypassed to DVSS (keep traces as short as possible).

47. DVSS2: Parallel digital VSS connection.

48. DVDD2: Parallel digital VDD connection.

49. CKB: Digital clock input complement (LVDS).

50. CK: Digital clock input (LVDS). Maximum frequency = 53 MHz.

51. RESETB: Digital reset complement (LVDS).

52. RESET: Digital reset (LVDS). Should be applied when CK is low. Minimum width = 10 ns.

53. DSUBS: Digital substrate. Connect directly to ground.

54. GND4: Ground supply for the comparators.

55. GND5: Ground supply for the integrator section.

56. AVDD3: VDD supply for integrator section. Must be well bypassed.

57. IBF1: Bias current set for analog mux followers. With a 53 MHz clock, the optimum is 250 uA (voltage is about 3V). IBF1 can be reduced if the clock frequency is slower. Bypass required, trace length not critical.

58. IBF2: Bias current set for integration capacitor followers. With a 53 MHz clock, the optimum is 150 uA (voltage is about 3.1V). IBF2 can be reduced if the clock frequency is slower. Bypass is not critical; can be omitted if necessary.

59. GND6: Ground for the charge compensation amplifiers.

60. VSS2: Supply for the charge compensation amplifiers. Bypass?

61. VSS3: Supply for the follower clamp and bus precharge. Bypass??

62. IBCCA: Bias current set for the charge compensation amplifiers. Nominally +150 uA (voltage is about 2.9V). Bypass not required. If charge compensation is not desired, connect IBCCA to ground.

63. VBCL: Front end clamp bias voltage, generated internally. No connection necessary unless clamp voltage adjustment is required. Typically 0.2V.

64. AVDD4: Voltage supply for current limiters. Bypassing is critical – connect to high frequency bypass capacitor (.1 uF) with as short a trace as possible).

QIE7B PINOUT DESCRIPTION

Note: Pin 1 is labeled on the chip in metal2, and numbering proceeds counterclockwise.

1. VCADJ: Charge compensation vernier. Internally biased to VSS-1V, input impedance ~ 20K. Can be varied between VSS-1V and VDD to adjust charge compensation to required value. (For minimum compensation, VCADJ=VDD). If compensation adjustment is desired, provide selectable external resistance to VDD. No bypass required.

2. VCS1: Charge compensation select #1. Internally biased to VSS-1V, input impedance ~ 20K. Leave unconnected for nominal compensation range; connect to VDD for a discrete reduction in compensation level (~35%).

3. VCS2: Charge compensation select #2. Internally biased to VSS-1.5V, input impedance ~30K. Leave inconnected for nominal compensation range; connect to VDD for a discrete increase in compensation level (~50%).

4. INREF1: Reference connection to external (47 ohm?) resistor. Connect external resistor between INREF1 and INREF2. It may be possible to use a 0 ohm resistor on the reference input, in which case INREF1 and INREF2 can just be directly connected together.

5. INREF2: Reference input. As stated above, external resistor must go between INREF2 and INREF1. Aside from that, the reference input can be left unconnected. However, for maximum noise rejection, the reference input should look as identical as possible to the signal input (INSIG). Nominal voltage level = 1V.

6. GND1REF: Ground supply for front end reference amplifier/splitter section.

7. VSS1: Supply voltage for front end amplifier/splitter section. Nominally 6.5V, but hopefully can be as low as 5.0V since peak input current is only 20 mA. Bypass required??

8. VCLAMP: Internally generated clamp voltage for amplifier feedback. This pin **MUST** be well bypassed with a high frequency capacitance of 0.1 uF (or greater). Keep trace as short as possible!!

9. INSIG1: Signal connection to external (47 ohm?) resistor. Connect external resistor between INSIG1 and INSIG2. The value of this resistance determines the magnitude of the input impedance for large signals. Keep the traces from the chip to the resistor SHORT and keep the insig1-resistor-insig2 loop area as small as possible!!

10. INSIG2: Signal input. Nominal voltage level = 1V.

11. GND1SIG: Ground supply for front end signal amplifier/splitter section.

12. GUARD: Substrate guard ring around signal input FET. Connect directly to ground if needed.

13. IBFE: Front end feedback amplifier bias current set. The value of this current determines the magnitude of the input impedance for low level signals. For 50 ohms input impedance, IBFE should be approximately -400 uA. The IBFE voltage level will be approximately VSS-1.8V (at -400 uA). Use a resistor to GND to set the current. Bypass???

14. IBIN: Input splitter DC bias current set. For a 53 MHz clock, the bias current should be +100 uA. Set with an external resistor (IBIN voltage is approx. 2.6V).

15. RFSEL: RF/2 clock frequency select. Internally pulled weakly low. Setting RFSEL high (5V) divides the input splitter DC bias current set by IBIN by two, allowing the clock frequency to be a factor of two slower without physically having to change the IBIN set current. This allows operation to be switched between RF and RF/2 with only one external bias set current.

16. ASUBS: Analog substrate connection. Connect directly to ground.

17. VREFN: Reference voltage used in conjunction with VREFP. This sets the range switch points. The value of (VREFP – VREFN)/2 determines the analog output voltage span. For example, if VREFP – VREFN = 2V, then this forces the QIE to switch ranges whenever SIGOUT becomes 1V more negative than REFOUT. In other words, (REFOUT – SIGOUT) is always between 0 and (VREFP – VREFN)/2. VREFN should be generated with respect to VSS and should be no more than 2V below VSS. VREFN should be driven by a low impedance voltage, since it draws approximately 2 mA.

18. VREFP: Reference voltage used in conjunction with VREFN to set the range switch points. Connect directly to VSS.

19. IBDIG: Digital output current set. Sets the current magnitude which is switched between output and output complement at the differential current mode digital outputs. The set current into IBDIG is approximately one third of the current which will be sunk at the digital outputs. For example, to sink an output current of 2 mA, +0.67 mA should flow into the IBDIG pin. The voltage at IBDIG for an applied current of +0.67 mA is approximately 1.3V.

20. VBLAD: Internally generated bias voltage used for the capacitor reset voltage ladder. Bypass required; place capacitor as close as is practical. Voltage level is typically (VDD – 1.5V).

21. AVDD1: Analog supply voltage, +5.5V with respect to VSS. Bypassing not critical – run to closest AVDD bypass.

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26. EXP2*: Digital exponent output bit 2 complement.

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29. CAPID0: Cap ID bit 0.

30. CAPID1*: Cap ID bit 1 complement.

31. CAPID1: Cap ID bit 1.

32. GND2: Ground for digital output buffers.

33. AVDD2: Analog voltage supply for analog output buffers, 5.5V with respect to VSS. Bypassing is critical – connect to high frequency bypass capacitor (.1uf) with as short a trace as possible.

34. GND3: Ground for the analog output buffers.

35. N/C

36. N/C

37. SIGOUT: Analog signal output. As input signal magnitude increases, SIGOUT goes more negative. Output impedance = 350 ohms. The signal span is from Vrefout to [Vrefout – (VREFP – VREFN)/2] for each of the 8 ranges. The voltage output level is approximately centered around VSS.

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43. VBCSD1: Internally generated bias voltage for current switch drive circuit. Bypass is required – place capacitor as close as is practical. Voltage is VSS – 0.7V.

44. VBCSD2: Reference for current switch drive circuit. Must be connected directly to VSS.

45. DVSS1: Digital VSS. As explained earlier, VSS may be as low as 5.0V, or may need to be as high as 6.5V. Bypassing???

46. DVDD1: Digital VDD. As explained before, VDD is +5.5V referenced to VSS. Must be well bypassed to DVSS (keep traces as short as possible).

47. DVSS2: Parallel digital VSS connection.

48. DVDD2: Parallel digital VDD connection.

49. CKB: Digital clock input complement (LVDS).

50. CK: Digital clock input (LVDS). Maximum frequency = 53 MHz.

51. RESETB: Digital reset complement (LVDS).

52. RESET: Digital reset (LVDS). Should be applied when CK is low. Minimum width = 10 ns.

53. DSUBS: Digital substrate. Connect directly to ground.

54. GND4: Ground supply for the comparators.

55. GND5: Ground supply for the integrator section.

56. AVDD3: VDD supply for integrator section. Must be well bypassed.

57. IBF1: Bias current set for analog mux followers. With a 53 MHz clock, the optimum is 250 uA (voltage is about 3V). IBF1 can be reduced if the clock frequency is slower. Bypass required, trace length not critical.

58. IBF2: Bias current set for integration capacitor followers. With a 53 MHz clock, the optimum is 150 uA (voltage is about 3.1V). IBF2 can be reduced if the clock frequency is slower. Bypass is not critical; can be omitted if necessary.

59. GND6: Ground for the charge compensation amplifiers.

60. VSS2: Supply for the charge compensation amplifiers. Bypass?

61. VSS3: Supply for the follower clamp and bus precharge. Bypass??

62. IBCCA: Bias current set for the charge compensation amplifiers. Nominally +150 uA (voltage is about 2.9V). Bypass not required. If charge compensation is not desired, connect IBCCA to ground.

63. AVDD4: Voltage supply for current limiters. Bypassing is critical – connect to high frequency bypass capacitor (.1 uF) with as short a trace as possible).

64. VBCAS: Cascode bias voltage, generated internally. Bypass required, however, trace length is not critical. Voltage level is typically VSS-0.8V.