QIE8 Pad Assignments

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The QIE8 is the latest addition to the "family" of QIE devices. It is the first of a new generation of parts which contain major design changes and improvements over the older versions of QIE. QIE8 is produced in the AMS 0.8u BiCMOS process, a "true" BiCMOS process (previous QIE's were produced in the pseudo-BiCMOS 2u ORBIT process).

QIE8 integrates input charge in 25 nS buckets over a large dynamic range and digitizes the result with nearly constant resolution over the entire range. It accomplishes this by integrating the charge on four ranges with different sensitivities, and selecting one range based on the signal magnitude. The integrator output is fed to a custom on-chip pseudo-logarithmic FADC which digitizes the result. The bit size of the ADC changes in piecewise linear fashion over its range to tend to keep the (bit size)/(signal magnitude) ratio constant. The QIE8 outputs are then purely digital, a 2-bit range number and a 5-bit FADC output.

QIE8 has two independent input amplifiers, one inverting and one non-inverting so that it can accept either polarity input signal. The non-inverting input is meant to accept a fast negative current PMT signal driven down a cable of significant length. It therefore has an impedance which is nearly constant over the entire range, in order to properly terminate a cable. The input impedance is selectable between two values, 50 and 93 ohms. The amplifier gain is approximately one, resulting in a low end sensitivity of 2.6 fC/ bit. The maximum charge accepted per bucket is approximately 26 pC, yielding a 10,000:1 dynamic range, or at least 13 bits. The non-inverting amplifier has a fast response to allow complete integration of a fast PMT pulse in one 25 nS bucket.
The inverting amplifier is meant to accept positive current input pulses from HPD's. Since HPD signal levels are low, the amplifier has a current gain of –2.6, resulting in a low end sensitivity of 1 fC/bit. The maximum input charge per bucket is then approximately 10 pC. Since HPD pulses are slower (stretched over several buckets), the inverting amplifier response is slower than the non-inverting amplifier, in order to limit noise. Also, its input impedance is low (30 ohms or less) but not constant over the full range, since this input is intended to be driven with a relatively short cable.
The user must select which input amplifier will be used by powering only the one desired, and grounding the VDD pin of the amplifier which will not be used.

Following is a list of QIE8 chip pads (<u>not</u> package pins). Many of the ground pins on the chip are intended to be bonded directly down to the die pad, which will serve as analog ground, and not to package pins. The user of a packaged part should refer to a pin list for pin definitions.

The chip pads are numbered from 1 to 84, starting in the upper left corner and proceeding counterclockwise.

1. **CAPID1**. Cap ID output MSB. (Cap ID is a 2 bit number representing which of the four pipelined integrating capacitors is being read out). The Cap ID outputs are read out as a low level differential voltage signal with LVDS-like levels, but with internal terminations (approx. 400 ohms). These outputs are only intended to drive a short distance (approx. 10 pF load) and are not intended to be terminated externally.

2. **CAPID1B**. Cap ID output MSB complement.

3. **OUTISET**. This pad gives external access to the bias circuit for the low level differential voltage output drivers (CAPIDs, EXPONENTs, and MANTISSAs). It is included mostly for test purposes and nominally should be left unconnected. A resistor can be connected from VDD to this pad to increase the output drive level. The nominal resistance which exists internally is 3.4K.

4. **SHIELD1**. Substrate guard between the ADC and the ADC output logic. Connect directly to die pad, which serves as analog ground.

5. **VDDA1**. VDD for ADC comparators. All analog VDDs (VDDA) should be externally bypassed and connected to a 5 - 5.5V supply.

6. **GNDA1**. GND for ADC comparators. All analog GNDs (GNDA) should be connected directly to analog ground.

7. **VDDA2**. VDD for ADC bandgap reference.

8. **GNDA2.** GND for ADC bandgap reference.

9. **VDDA3**. VDD for ADC preamps.

10. **GNDA3.** GND for ADC preamps.

11. **SHIELD2.** Substrate guard between ADC and analog front end. Connect directly to analog ground.

12. **VSUBS1.** Range circuit substrate connection. Connect directly to analog ground.

13. **VDDA4**. Range comparator VDD.

14. **GNDA4**. Range comparator GND.

15. **INTISET**. Integrator bias current set. This is driven by an internal resistor to VDD of nominally 36K. This pad is mainly for test purposes and can be left unconnected.

16. **GNDA5**. Integrator GND.

17. **VDDA5**. Integrator VDD.

18. **VDDA6**. Integrator current dump VDD.

19. **VREF234**. Integrator reference voltage for ranges 2, 3, and 4. This is generated internally and serves only as a test monitor.

20. **GNDA6**. Regulated cascode GND.

21. **VDDA7**. Input amplifier protection VDD.

22. **CLAMP**. Non-inverting input amplifier bias voltage, which must be held at AC ground with an external capacitor of at least 0.1 uF.

23. **VDDA8**. Non-inverting input amplifier VDD. If the inverting amplifier is being used, the non-inverting amplifier should be disabled by grounding this pad.

24. **NI_INBIAS**. Non-inverting amplifier DC input bias current set. Set by connecting a resistor from this pad to VDD. The internal bias current will actually be 4 times smaller than the set value. Nominal set current is 26 uA (6.5 uA amplifier bias). However, this current can perhaps be reduced by a factor of 2 and still retain adequate frequency response. For nominal bias, use approx. 140K.

25. **NI_IN1R**. Non-inverting amplifier reference input #1. This reference input ideally will have a cable or interconnect attached to it which looks identical to the signal input (although the reference input should actually have no signal applied to it).

26. **NI_IN2R**. Non-inverting amplifier reference input #2. An external resistor must be connected between reference input #1 and reference input #2. The value of this resistor depends on the desired input impedance. For 50 ohm input impedance, the R value should be approx. 70 ohms, and for 93 ohm input impedance it should be approx. 125 ohms.

27. **GNDA7**. Non-inverting reference input amplifier ground.

28. **NI_IN1S**. Non-inverting amplifier signal input #1. The signal input cable or interconnect should be connected directly to this input (and the cable shield directly to the analog ground, or die pad).

29. **NI_IN2S**. Non-inverting amplifier signal input #2. An external resistor must be connected between signal input #1 and signal input #2. The value of this resistor depends on the desired input impedance. For 50 ohm input impedance, the R value should be approx. 70 ohms, and for 93 ohm input impedance it should be approx. 125 ohms.

30. **GNDA8**. Non-inverting signal input amplifier ground.

31. **GNDA9**. Inverting amplifier reference input amplifier ground.

32. **I_INREF**. Inverting amplifier reference input. This reference input ideally will have an interconnect attached to it which looks identical to the signal input (although the reference input should actually have no signal applied to it).

33. **VSUBS2**. Inverting amplifier substrate connection. Connect directly to analog ground.

34. **I_INSIG**. Inverting amplifier signal input. The signal interconnect should be connected directly to this input (and the interconnect ground wire directly to the analog ground, or die pad).

35. **GNDA10**. Inverting amplifier signal input amplifier ground.

36. **VDDA9**. Inverting input amplifier VDD. If the non-inverting amplifier is being used, the inverting amplifier should be disabled by grounding this pad.

37. **GNDA11**. Input amplifier (inverting and non-inverting) bias ground.

38. **SHIELD3**. Substrate guard around the input amplifiers. Connect directly to analog ground.

39. **I_INBIAS**. Inverting amplifier DC input bias current set. Set by connecting a resistor from this pad to ground. The internal bias current will actually be 4 times smaller than the set value. Nominal set current is 8.4 uA (2.1 uA amplifier bias). However, this current can perhaps be reduced by a factor of 2 and still retain adequate frequency response. For nominal bias, use approx. 350K.

40. **I_SETP**. Inverting amplifier bias. This is set internally with a nominal 7.4K resistor to ground. No external connection is necessary unless a different amplifier bias is desired.

41. **NI_SETP**. Non-inverting amplifier bias. Since the input impedance of the non-inverting amplifier is dependent on this bias value, no internal bias set resistor is

present. A 1% tolerance external resistance should be used to set this bias value. Nominal is a 14K resistor to ground (300 uA).

42. **RINSEL**. Selects the input impedance of the non-inverting input amplifier. If unconnected, this pad defaults high (VDD), which sets the input impedance to 93 ohms. If grounded, the input impedance is 50 ohms.

43-46. **DAC0-3**. Pedestal DAC inputs. Bits 0-2 control the pedestal magnitude (binary code, bit 0 is LSB) and bit 3 controls the polarity. Bit 3 low gives positive pedestals, and high gives negative pedestals. Each DAC bit gives approx. 0.6 ADC bits of pedestal, therefore the pedestal range is from 0 to about 4 ADC bits, in each direction. If unconnected, the DAC pads all default low.

47. **GNDA12**. DAC ground.

48. **SHIELD4**. Substrate guard around digital control block.

49. **VSUBS3**. Digital control substrate connection. Connect directly to analog ground. (Or system ground??)

50. **GNDD1**. Digital ground. Do not bond directly to die pad (analog ground) – connect GNDD1 and GNDD2 together as soon as possible outside the chip package, then connect this net to PC board ground ("system" ground).

51. **VDDD1**. Digital VDD. Intended to be connected to the same supply used for VDDA. Some filtering may be required to avoid pollution of the analog supply. In the worst case, a separate VDDD supply may be required. VDDD1 and VDDD2 should be connected together as soon as possible outside of the chip package and this net bypassed to GNDD1 and GNDD2. Probably the bypass should be connected to the GNDD's at a point just **before** GNDD is connected to system ground.

52. **GNDD2**.

53. **VDDD2**.

54. **GNDD3**. The GNDD3 and VDDD3 pair should be treated like the GNDD1,2 and VDDD1,2 pair with its own bypass capacitor. Possibly the GNDD3 - VDDD3 bypass can be eliminated and these lines just paralleled with 1,2.

55. **VDDD3**.

56. **RESET**. QIE reset signal. The reset signal should be approximately one clock period in duration, and the edges should occur near a negative going edge of the

CLK signal. RESET is designed to accept a 3.3V CMOS level. A 5V CMOS level is also acceptable. After application of the reset, the capID is set to 0.

57. **CLKB**. Clock input complement.

58. **CLK**. Clock input signal. CLK – CLKB accepts a low level differential signal (LVDS levels). QIE8 is designed for 40 MHz operation.

59. **PADGND1**. Ground for clock receivers. Connect to analog ground. (Or system ground??).

60. **RANGE0**. Range 0,1 form a binary code which forces the QIE range when in fixed range mode. When in autorange mode, these bits have no effect. Input levels are 3.3V CMOS. When unconnected, they default low.

61. **RANGE1**.

62. **FIX/AUTO**. Selects between fixed range mode (range determined by range 0,1 bits) and autorange mode. 3.3V CMOS level. Low selects autorange, high selects fixed range. If unconnected, defaults low.

63. **CALMODE**. Selects between normal mode and calibration mode. 3.3V CMOS level. Low selects normal mode, high selects calibration mode. If unconnected, defaults low.

64. **GNDD4**. ADC encoder digital ground. GNDD4-VDDD4 pair should be treated as the other digital supply pairs.

65. **VDDD4**. ADC encoder digital VDD.

66. **VSUBS4**. ADC encoder substrate connection. Connect directly to analog ground. (Or system ground??)

67. **PADGND2**. Ground for output drivers. Connect to analog ground. (Or system ground??).

68. **PADVDD1.** VDD for output drivers. (Treat PADGND2-PADVDD1 as digital supply pair??).

69. **MANTISSA0.** Least significant mantissa (ADC) output bit. All outputs are low level differential voltage, as explained for pin 1.

70. **MANTISSA0B.** Mantissa0 complement.

71. **MANTISSA1.**

72. **MANTISSA1B**.

73. **MANTISSA2**.

74. **MANTISSA2B.**

75. **MANTISSA3**.

76. **MANTISSA3B**.

77. **MANTISSA4**.

78. **MANTISSA4B**.

79. **EXPONENT0**. Least significant exponent (range) output bit.

80. **EXPONENT0B**.

81. **EXPONENT1**.

82. **EXPONENT1B**.

83. **CAPID0**.

84. **CAPID0B**.