Chapter 4

The Pixel Vertex Detector

4.1 Introduction

The vertex detector is critical to the success of the BTeV experiment. The key goals of the vertex detector are excellent spatial resolution, ease of tracking pattern recognition, radiation hardness, material thinness, and readout of data fast enough for use in the lowest-level (L1) BTeV trigger system. To do this, very high precision space points along charged particle trajectories are required and these are provided by the pixel detector.

The pixel vertex detector is located at the center of the BTeV spectrometer, inside a 1.5T dipole magnet surrounding the interaction region. Data from the pixel detector will be used to find charged particle trajectories and reconstruct the vertices from which the tracks come. Pixel detectors are chosen because they can provide high precision space points with very few noise hits, and be quite radiation hard. Radiation hardness enables the detector elements to be placed very close to the beam (in vacuum, separated from the beam only by a few thin strips for RF shielding), minimizing track extrapolation errors.

4.2 Requirements

The measurement of 3-dimensional space points by the pixel detector, with very few additional noise hits, provides the necessary elements for excellent pattern recognition, allowing the reconstruction of tracks and vertices in real time, essential for triggering on events containing reconstructable heavy flavor decays. The pixel detector has to cover completely the angular acceptance of the downstream detector elements. The requirements that are listed below have been set to meet the BTeV physics goals based on detailed simulations and analyses. Furthermore, we have carried out several years of extensive R&D, including bench tests, irradiation studies and beam tests. This has led to a baseline design of the pixel system that will meet the performance required by the experiment to achieve its physics goals while being both affordable and technically achievable.

4.2.1 Resolution

The resolution of each pixel plane is one of the defining characteristics of the system. This resolution is determined by two things: the spatial resolution of the pixel sensors in a plane, and the amount of material in a plane. A fundamental limit on the accuracy with which tracks can be extrapolated out of the pixel detector into the beam region is given by the spatial resolution at the first two measurement planes, and by the error in the reconstructed track direction due to multiple Coulomb scattering in the first pixel plane.

- **Position resolution** The spatial resolution at each pixel plane must be better than 9 microns in the narrow pixel direction for tracks at angles up to 300mr with respect to the beam.

- **Material Budget**: Each pixel plane should have no more than 1.5% of a radiation length in the active area. Ouside the active area but within the angular acceptance of the downstream detector elements, all materials that are required by the pixel system have to be minimized and must, on average, be less than the amount inside the active area.

- **Time Resolution**: Proper time resolution of the Pixel System has to be better than 50 fs.

- **Impact Parameter Resolution** : this is dominated by the closeness, material, and resolution in the first measurement point. It is related to the position resolution and the material budget. It should be good enough to achieve a rejection factor of 100 at the L1 trigger while keeping the efficiency for interesting all-charged B decays at 50% or above.

- **Two-track Resolution**: When two tracks cross a pixel plane too close to one another, the measurements associated with the two tracks can not be separated from one another. The two-track resolution must be better than 450μm.

4.2.2 Efficiency

BTeV was designed to operate at a luminosity of 2×10^{32} cm^{-2}sec^{-1} with a 132 ns beam-crossing interval (BCO). We can therefore operate at longer BCO as currently planned for the Tevatron, specifically at 396 ns, even with a corresponding larger number of interactions per beam crossing. In order to allow the Trigger system to use simple pattern recognition algorithms which can be implemented in hardware, the Pixel System must have very high efficiency and excellent two-track resolution. All hit data must be read out in a zero suppressed format, and spurious hit data must be minimized. The Pixel system must have high enough bandwidth so that the pixel data from every beam crossing can be read out and be provided to the Level 1 Trigger hardware.

- **Efficiency**: At design luminosity, each pixel plane must have a hit efficiency of at least 98.5% during its entire operational lifetime. This includes losses due to dead pixels, noisy pixels whose output is suppressed, and any loss of data by readout electronics or readout deadtime.
- **Noise**: The noise rate of the system must be less than 10^{-5} per pixel.
- **Readout Bandwidth**: The BTeV Level 1 trigger must make a decision on every bunch crossing (396 ns). This requires a data-driven readout of the pixel system. It also means that (on average) all hit pixel data has to be read out and be available to the trigger processor every bunch crossing.

4.2.3 Radiation Tolerance

The anticipated radiation field at the pixel detector is expected to be dominated by high energy charged particles coming from the primary proton-antiproton interactions, and by electrons and positrons from photon conversions. The best estimate of this rate currently comes from BTeV GEANT and MARS calculations. The hottest region will be that nearest the beam for each detector element. At the closest position, planned for 6 mm from the beam line, the integrated number of minimum ionizing charged particles per ten years of running at a luminosity of 2×10^{32} cm^{-2}sec^{-1} is $\sim 10^{15}$/cm^2, corresponding to an ionizing dose of roughly 35 Mrads. (Most of the pixels will see substantially less radiation as the radiation level falls roughly as $1/\mathrm{d}^2$, where d is distance from the colliding beams.) The detector components must continue operating in this environment, with acceptable levels of signal-to-noise, operating voltages, efficiency, and spatial resolution.

- **Radiation Tolerance**: All the components of the pixel system must remain operational up to 10 years of BTeV running at the nominal luminosity.

The detector design has been guided by these high level physics driven requirements, as will be described in the sections below, where more detailed functional requirements will also be presented.

4.3 Overview

The pixel vertex detector provides the high resolution tracking near the interaction which is required to associate tracks with their proper vertices – primary and secondaries. The design of the pixel detector system is driven by the long interaction region at the Tevatron which has a σ_z of 30 cm. This forces one to have a rather long vertex detector. In addition, the detector must be placed very close to the interaction region in order to achieve good impact parameter resolution and acceptance. In practice, this is limited both by the radiation level that can be tolerated by the detector as well as the beam aperture. Furthermore, since the vertex detector information will be used in the Level I trigger, this places special requirements on the detector and its readout. It is especially important for the trigger, which operates within strict time constraints, that the number of spurious noise hits be as low as possible. Also, the system must minimize the production of pattern recognition ambiguities or ghost tracks which would take extra time to sort out at the trigger level. The three-dimensional nature of the pixels is an enormous help in this regard.

With the planned configuration, the point resolution is expected to be between 5μm and 9μm, depending on the angle of the incident track. This has been demonstrated in our beam test at Fermilab in 1999 [1]. The angular resolution (without taking multiple scattering into account) is of the order of 0.1 mr. The pixel detector does quite a respectable job of measuring momentum without any assistance from the downstream spectrometer. For example, for a track which passes through ten stations, the resolution is

$$\frac{\sigma_p}{p} = 2\% \times \frac{p}{10\ \mathrm{GeV/c}} \tag{4.1}$$

where p is the momentum in GeV/c.

The pixel detector system has 23 million pixels, each 50 μm by 400 μm, in order to have acceptable spatial resolution and low occupancy for the high multiplicity interactions anticipated. The BTeV pixel detector, like most pixel systems developed for high energy physics experiments, is based on a design relying on a hybrid approach. With this approach, the pixel sensor array and the readout chips are developed separately and the detector is constructed by flip-chip mating of the two together. Each sensor pixel is read out by a dedicated electronics cell, containing appropriate amplifier, discriminator, and other circuitry in an Application Specific Integrated Circuit (ASIC). A bump bond connects each sensor pixel to its readout cell. The pixel module is the basic building block of the pixel detector. Each module consists of a single sensor which is bump-bonded to a number of readout chips. Underneath the readout chips, a high density interconnect (HDI) flex circuit is glued that carries the I/O signals and power between the chip and the readout electronics. The modules come in four different sizes. In total, there will be 1380 modules and 8100 readout chips. The total active area of the detector is about 0.5 m^2.

The BTeV pixel detector has doublets of planes distributed along the IR separated by 4.25 cm. The individual planes are composed of two half-planes, each about 5 cm $\times$ 10 cm. There are altogether, 60 planes arranged in 30 doublets (stations). They are mounted left and right of the beam and are arranged so that a small square hole of $\pm$6mm $\times$ $\pm$6mm is left for the beams to pass through (see Fig. 4.1). The two halves of the detector are displaced along the beamline by up to half-spacing between the stations to allow overlap between the two halves. A schematic of the detector is shown in Fig. 4.1.

Each half plane will have detector modules mounted on two sides of a graphite substrate with excellent thermal conductivity. On one substrate, the modules will have the narrow pixel dimension lined up in the y-direction (vertical) and the active area measures about 5 cm by 10 cm. On the other substrate, the modules will have the narrow pixel dimensions lined up in the x-direction (horizontal) with a total active area of 3.8 cm by 7.3 cm. A reasonable momentum measurement can be made using information from three or four stations. Pulse height is read out and made available to the trigger, hence charge sharing can be used to improve the spatial and momentum resolution. The momentum information can be used to reject very soft tracks that would adversely affect the trigger algorithm because of multiple scattering.

Each half of the pixel detector will be sitting in vacuum and will be separated from the beams by a thin rf shield. To take the signal out of the vacuum vessel, we will use large feed-through boards (FTBs) made out of multilayer printed circuit boards. The vacuum system will consist of two integrated cryopumps plus additional surfaces at liquid nitrogen temperature (cryopanels) inside the pixel vacuum vessel. Nominally, the pixel detector will be placed at 6mm from the beams. During beam refill, the two halves of the detector will be moved away to about $\pm$ 2 cm from the beams. When the beam is stable, the detectors will then be moved close to the beam for data taking. A system of actuators and motion sensors will be used. To bring high voltage (HV) bias to each module, a power cable will be used. Our baseline assumes that each module will have its own HV power supply channel and that it will have separate analog and digital low voltage (LV) for the readout chips. On average, the power dissipated is about 0.5W/cm^2 of the active area, giving a total of 2.5 kW for the whole pixel detector system. The operating temperature of the detector is about -5°C, and a cooling system is needed.

Fig. 4.2 shows a conceptual design for the stainless steel vacuum vessel for the pixel detector. The vessel is a rectangular box with a length of $\sim$ 165 cm and a height of $\sim$ 60 cm. Particles within 300 mrad traverse only the pixel stations and the 0.5 mm thick Al exit window. The graphite substrates will be attached to a support frame made out of carbon fiber composites. The position of the pixel detectors relative to the positions of the colliding beams will be controlled by motors located outside the magnet with actuators attached to the vacuum vessel.

4.4 Summary of completed R&D

4.4.1 Introduction

Since the submission of the BTeV Proposal three years ago, we have made great progress in the development of the individual components required to build the BTeV pixel detector. The major components of the pixel detector system are the sensor, readout chip, sensor-readout-chip connection (bump bonding), high-density interconnection between the pixel readout chips and the system control elements, and the mechanical support and cooling systems. We have been designing and purchasing prototypes of these components, assembling units and testing them in beams and exposing them to intense radiation. We have also performed detailed simulation studies to understand the various design issues for the components as well as system aspects. Through these efforts, not only are we learning what is needed for BTeV, but we are gaining the necessary experience and know-how to build the actual pixel detector for the BTeV experiment. One of the highlights of this effort is the successful demonstration in a test beam during the 1999 Fermilab fixed target run of the resolution and

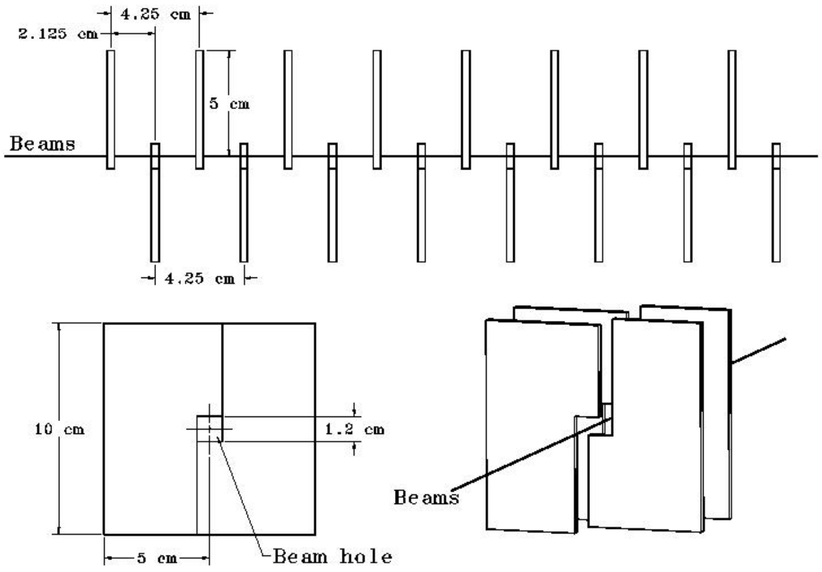

Figure 4.1: Schematic drawing of part of the pixel detector.

pattern recognition power that can be achieved with a pixel detector [1]. Our R&D effort has also addressed the system engineering aspects. The vacuum system and RF shielding was reviewed by the Fermilab Accelerator Division in October 2003. The baseline design concept of the two systems were well received by the review panel.

Our R&D program has so far led to more than 40 publications and a large number of internal documents and reports. A complete list of all the published papers can be seen in [2]. This section summarizes the main accomplishments.

4.4.2 Sensor Development

4.4.2.1 Introduction

The dimensions of the pixel unit cell determine the hit resolution and occupancy. In turn, they affect the complexity of the system, the space available for the pixel electronics, and the demands posed on the cooling system. The sensor thickness affects the signal to noise achievable in the course of the detector lifetime, and the resolution achievable for large angle tracks that share the charge signal among several pixel cells. The overall material budget is determined not only by the thickness of the active elements in this system (sensor and readout electronics), but also by the mechanical support and cooling system.

The BTeV pixel detector will be placed very close to the colliding beams and will be

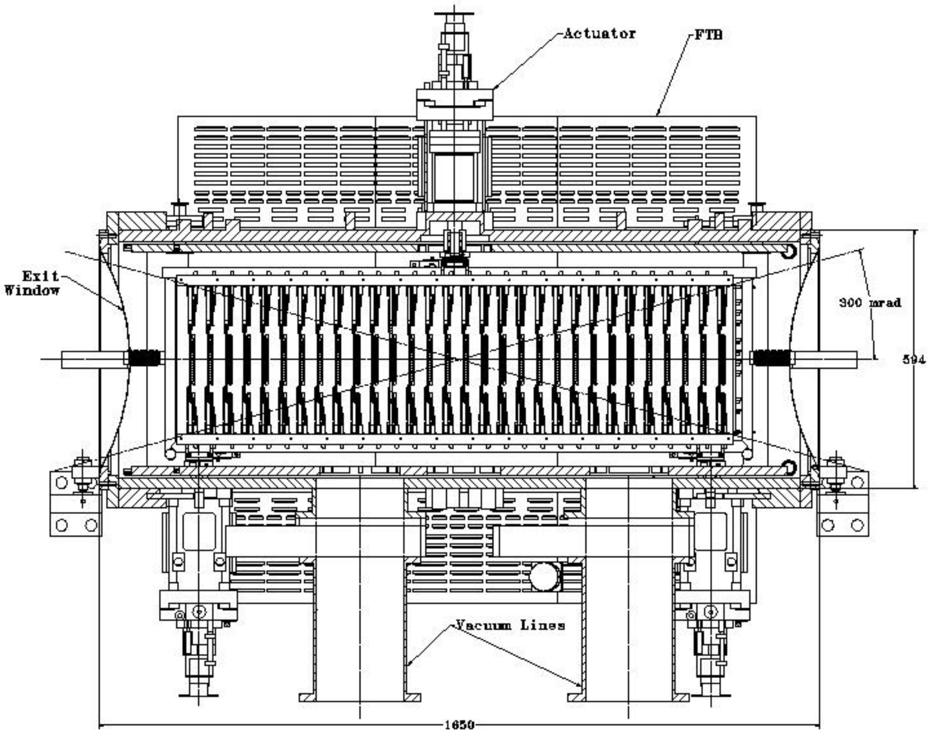

Figure 4.2: Side view of the vacuum vessel and support structure for the pixel detector. The pixel stations are mounted in two halves inside the vacuum vessel. Between the pixel stations and the colliding beams, there will be a thin RF shield. Signals are fed through the vacuum vessel via printed circuit boards with high density connectors. Also shown in the figure are actuators to move the detectors in and out of the beams for data-taking and beam refill.

exposed to a significant level of irradiation. At the full luminosity that we plan to operate, it is expected that the innermost pixel detector will receive an equivalent fluence of 1×10^{14} particles/cm^2 per year of running. This will lead to radiation damage to both the surface and the bulk of the silicon pixel detectors.

4.4.2.2 Sensor Design Considerations

The main challenge is to have a radiation hardened detector which will survive and remain operational after significant radiation damage to both the surface and the bulk of the silicon sensors.

Ionizing radiation leads to the charge-up of the surface, which anneals out in less than an hour at room temperature and to the formation of trapped charge both in the oxide and the interface to the silicon bulk. This charge is mainly positive and its presence results in the accumulation of an electron layer under the oxide. This leads to an increase in the interpixel capacitance with irradiation. The trapped charge density depends on the crystal orientation because of the amount of dangling bonds available. Therefore, the crystal orientation is an important parameter in the design of the detectors. In particular, test results on silicon strips showed that the interstrip capacitance is strongly affected by radiation for $< 111 >$ substrate. Surface currents due to the oxide charges have been observed but they are less important than the bulk currents induced by irradiation.

The bulk damage is mainly due to the non-ionizing energy loss (NIEL) which, through the displacement of atoms in the crystal lattice, creates new energy levels, effectively acting as acceptors. Therefore the effective doping concentration will change with irradiation. For very-high-dosage irradiation, this will eventually lead to inversion of the conduction type of the bulk material (type-inversion), increases in leakage current and depletion voltage, changes in capacitance and resistivity, and charge collection losses. These are problems that need to be addressed by all the next generation hadron collider experiments. As a result, there is a worldwide effort to address these technical challenges.

In order to increase the useful operation time of the silicon sensors, operation with partial depletion has to be considered. This is more suitable for n-type pixel readout, because after type inversion the depleted region will grow from the n$^+$ side of the junction. For this reason, the BTeV pixel sensors have $n^+/n/p^+$ configuration. In these detectors, the charge collecting pixels are defined by the n-implants that are isolated from their neighbors. Without isolation, the accumulation layer induced by the oxide charge would short the individual n^+ pixels together. We have explored two isolation technqiues:

- The p-stop isolation where a high dose p-implant surrounds the n-region.
- The p-spray isolation developed by the ATLAS collaboration, where a medium dose shallow p-implant is applied to the whole n-side. To increase the radiation hardness and also the breakdown voltage before irradiation, a "grading" of the p-spray implantation (moderated p-spray) is required [8].

4.4.2.3 Sensor Prototypes

Similar radiation environment is expected in the high luminosity LHC collider experiments ATLAS and CMS. As a result, there is a worldwide effort to study the various design issues affecting the radiation hardness of silicon sensors. Since our pixel size (50 μm x 400 μm) is the same as ATLAS, we have followed rather closely their development path. The design of our silicon sensors is guided by the necessity to operate the device at hundreds of volts without the risk of junction breakdown or micro-discharge. For this, a multiple guard ring structure is used to control the potential drop toward the cut edge on the p-side. These structures maintain the p edges of the sensors at the same potential as the n$^+$-side, which sits at the input potential of the readout chip. Finally, the hardening of the silicon itself is accomplished following the ROSE collaboration results, which developed the diffused oxygenated float-zone (DOFZ) silicon where the oxygen impurity concentration in the silicon wafer is enriched in a controlled way by a diffusion process. Our design takes advantage of all these previous results. We have signed a non-disclosure agreement with the ATLAS pixel sensor group. Through this arrangement, we have purchased sensor wafers from them as well as gained access to their design. These wafers include both p-stop and p-spray sensor wafers. Some of these sensors were used in our test beam run in 1999 and we studied charge collection for both types of sensors.

We are also developing sensors of our own design. Our first effort was a joint development with the US CMS. We made a joint submission in Spring 1999 to SINTEF Cybernatics (Oslo, Norway). These wafers contain $n^+/n/p^+$ sensors with different p-stop isolation geometries. This submission also included wafers from oxygen enriched silicon. In the summer of 2002, we received from TESLA (Prague, Czech Republic) a new batch of 15 pixel sensor wafers. These wafers contain sensors with the size and form factor to meet the needs of the BTeV pixel detector. For this submission, we used the moderated p-spray technology.

4.4.2.4 Test Results on sensor prototypes

We have tested sensors from three vendors: the p-stop sensors are from SINTEF, the p-spray sensors are from TESLA and from CiS (Erfurt, Germany). The base material for the p-stop sensors was low resistivity (1 - 1.5 kohm/cm), 270 μm thick $< 100 >$ silicon. The p-spray sensors were fabricated using higher resistivity (2-5 kohm/cm) $< 111 >$ silicon, 250 μm thick. Some of the SINTEF and CiS wafers and all the TESLA wafers have been oxygenated. We tested three different pixel array sizes for p-stop sensors and one for the p-spray. The first p-stop array (called test-sized sensor) contains 12 x 92 cells and all these cells, except for four, are connected together. This structure was designed to study the behavior of a single cell. The second array (called FPIX0-sized sensors) contains 12 by 64 cells and it is designed to be read out by a single FPIX0 chip [10], the very first readout chip implementation for BTeV. The third array (called FPIX1-sized sensors), both for p-stop and p-spray, contains 18 x 160 cells and it is designed to be read out by a single FPIX1 chip. We have four different guard ring structures on the tested devices.

SINTEF p-stop sensors We have tested prototype p-stop sensors produced by SINTEF. Figure 4.3 shows the typical I-V curves measured for two of the test-sized sensors from a non-oxygenated wafer. These curves show very small leakage current and a reverse breakdown voltage of 500 V or higher (breakdown voltage is defined as the voltage for which the current increases steeply and is larger than 1 mA at room temperature). We have probed all sensors on all the wafers that we have received. To characterize these sensors before and after irradiation, we measured bulk parameters of the sensors including the bias voltage dependence of the leakage current, the full depletion voltage, breakdown voltage, and the temperature dependence of the leakage current [5]. Other parameters studied include the voltage distribution across the guard rings, effect of dicing, temperature and humidity dependence. Most of the sensors meet the specifications: leakage current less than 50 nA/cm^2 and breakdown voltage above 300V. Typical depletion voltage is about 180V. We have found the

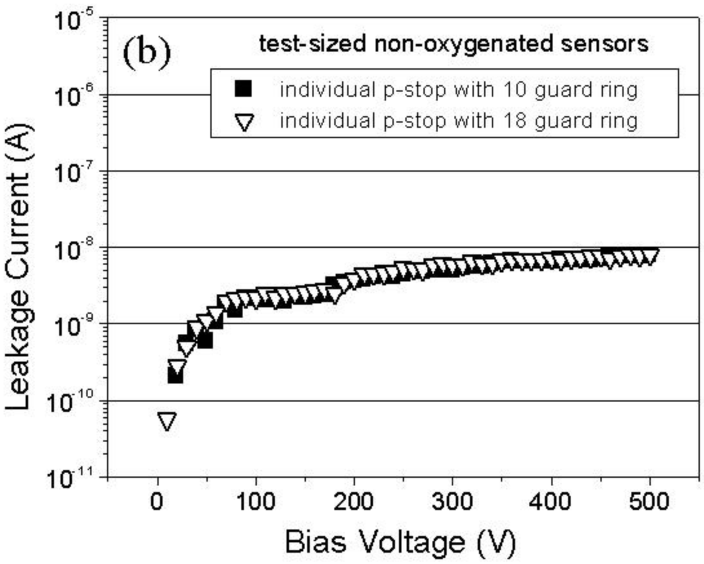

Figure 4.3: Typical I-V characteristics for non-irradiated test-sized pixel sensors

same results for both common and individual p-stop pixel isolation, for sensors with different guard ring layout and also between oxygenated and non-oxygenated wafers.

We also noticed that during wafer probing the test-sized sensors had better performance, i.e., higher breakdown voltage (> 500 V) and small leakage current ($\sim$10 nA/cm^2 after full depletion). For the FPIX0-sized and FPIX1-sized bare sensors, although the current was also small, the breakdown voltage was lower (typically just above 300V). The same results were found for all the sensors that were tested. The poorer breakdown voltage performance for the bare FPIX0-sized and FPIX1-sized sensors is due to the fact that we could not bias properly all the cells on the bare sensors. Fig. 4.4 shows the I-V of a FPIX1-sized sensor before and after bump bonding to a readout chip and one can clearly see the difference. In fact, the breakdown voltage performance improved significantly and was similar to that obtained for the test-sized sensors. This was observed for all the sensors that were bump bonded to readout chips.

A few of these sensors have been exposed to a 200 MeV proton beam at the Indiana University Cyclotron Facility (IUCF). Fig. 4.5 shows the leakage current measurements before and after irradiation up to a fluence of 4×10^{14} 200 MeV protons cm^{-2} for a SINTEF p-stop sensor. The leakage current after irradiation increased by several orders of magnitude. However, operating at lower temperature can signifcantly reduce this leakage current. Fig. 4.6 shows that the leakage current decreases exponentially with temperature. Up to 6×10^{14}p/cm^2, the sensors have a breakdown voltage higher than 500 V.

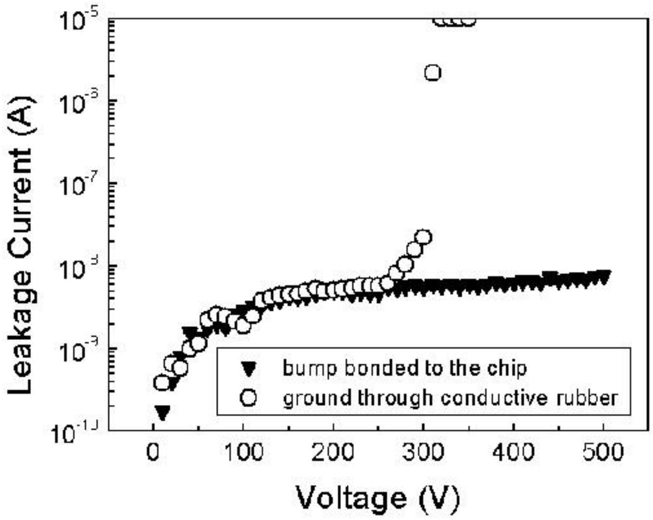

Figure 4.4: I-V characteristics for a FPIX1-sized p-stop sensor before and after bump bonding to the readout chip.

The leakage current after irradiation has a nearly linear dependence on fluence. In fact, the increase of the leakage current ΔI (i.e. the difference between the currents measured after and before irradiation) shows a linear dependence on the fluence: $\Delta \mathrm{I} = \alpha \Phi \vee$ where α is the damage constant, Φ is the fluence, and $\vee$ is the sensor volume. Fig. 4.7 shows the fluence dependence of the increase in leakage current normalized to volume. We obtained a value for the leakage current damage constant α of 3.8×10^{-17} A/cm, comparable to previous measurements [3].

The other bulk damage is the change in effective doping density which is reflected in a change in the full depletion voltage. Fig. 4.8 shows the dependence of the full depletion voltage on the proton irradiation fluence for a few p-stop sensors made from standard and oxygenated wafers. At a fluence of 6×10^{14} p cm^{-2}, the full depletion voltage is still rather low, even lower than the value before irradiation. This characteristic is due to the low resistivity of the starting silicon material. This result, together with the fact that the breakdown voltage is still high compared to the full depletion voltage after irradiation, means that the BTeV pixel detector can be fully depleted without excessively high bias voltage even after a few years of operation. These tests show acceptable operation of the irradiated sensors in terms of leakage current, required depletion voltage, and breakdown voltage[5]. However, for this pixel layout there is still the problem with determining the breakdown voltage in

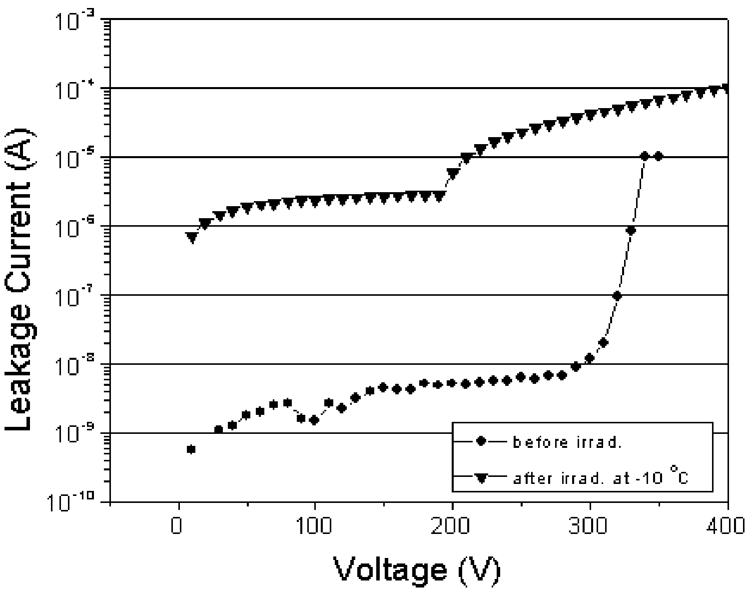

Figure 4.5: Leakage current measurements before (at room temperature) and after (at -10^0C) irradiation to 4×10^{14} p/cm^2 for a SINTEF p-stop sensor.

wafer probing. In this design, it is not possible to implement a bias grid in the layout and, therefore, we cannot bias simultaneously all the cells before connection to the readout chip.

P-spray sensors Several p-spray wafers from CiS and two from TESLA were tested. These were ATLAS pre-production pixel sensor wafers. Apart from a few sensors that show higher leakage current and low breakdown voltage (< 300V), the typical I-V curves for FPIX1-sized p-spray sensors show a breakdown voltage higher than 500V and a low leakage current. We have irradiated these sensors in a few steps up to a total of $4.2 \times 10^{14} p/\mathrm{cm}^2$. Fig. 4.9 shows the increase in the leakage current due to irradiation for the sensor irradiated up to 2.3×10^{14} p/cm^2. The current increased by several orders of magnitude, as was the case for the p-stop sensors that we tested. We investigated the dependence of the full depletion voltage on proton fluence (see Fig. 4.10) and again we found that up to 4.2×10^{14} p/cm^2 the depletion voltage is still very low compared with the breakdown voltage (> 500V). From a comparison between Fig. 4.8 and Fig. 4.10, we can see that the type inversion occurs at a lower dose for the high-resistivity p-spray sensors than for the low-resistivity p-stop sensors.

FPIX2 sized p-spray sensors We received in the summer of 2002 15 wafers from TESLA with the sensor layout matched to the size of the new FPIX2 resdout chip (decsribed in the next section). These are low resistivity moderated p-spray sensors. Probing tests have been completed. We have found satisfactory yield also from this batch of wafers. We plan to

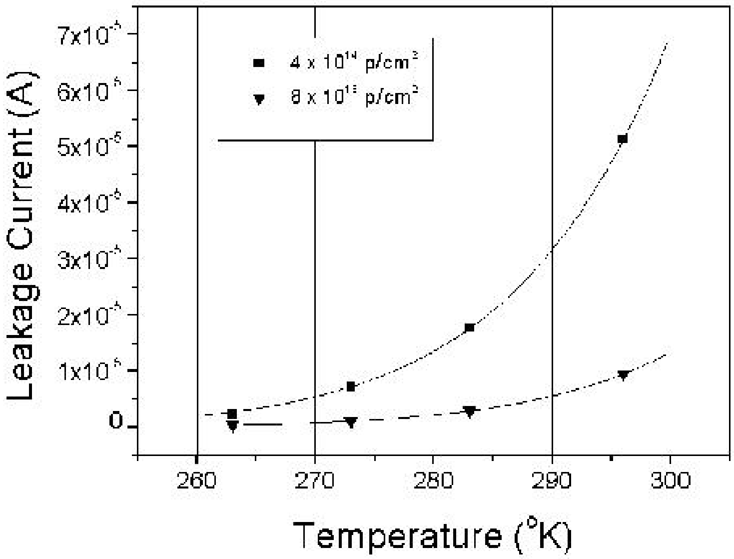

Figure 4.6: Leakage current as a function of temperature for two sensors. One was irradiated to 8×10^{13} p/cm^2, and the other to 4×10^{14} p/cm^2.

characterize these new sensors before and after irradiation and readout by the new FPIX2 readout chips.

Our plans for the future are to continue the radiation hardness investigation for the p-spray type of sensors. We plan to study the moderated p-spray detectors in a test beam to study the charge collection properties before and after irradiation and compare the results with the predictions from simulation. The p-stop sensors are used in a beam telescope that we have built for the test beam. Besides using these detectors to provide the beam reference, we will also check the charge collection properties and resolution of these sensors.

4.4.2.5 Simulation

A detailed understanding of the factors affecting the sensor performance is crucial to its design. We have studied a number of issues through simulation. These include charge collection, radiation damage effects (including the deterioration of the noise performance due to the increased leakage current and the change in detector response induced by the change in the effective donor concentration), charge sharing, resolution achievable as function of track angle, and mapping of the electric field throughout the whole sensor. Other factors that affect the ultimate resolution achievable in this system are related more closely to the design approach and the performance of the readout electronics. In particular, the electronic noise, and the threshold that determines the minimal charge deposition that will be recorded as a signal hit, are important. The sensitivity to these parameters has been studied, as well as the tradeoff between analog and digital readout.

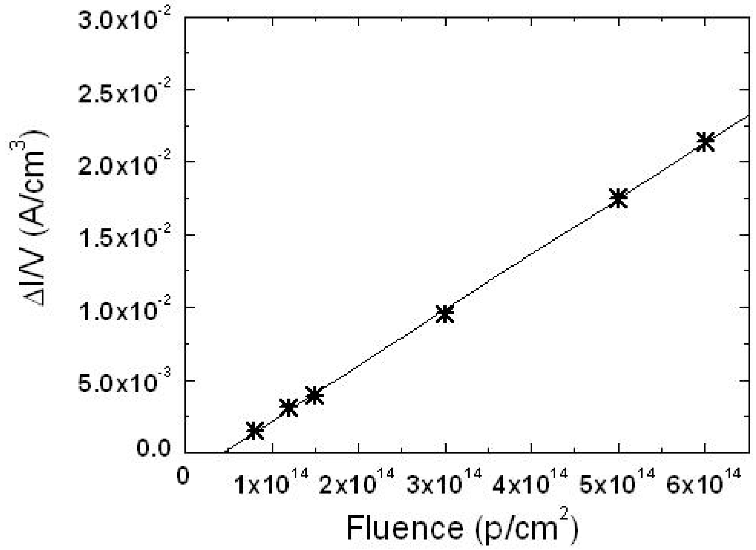

Figure 4.7: Fluence dependence of the increase in leakage current for p-stop sensors. All measurements were taken at room temperature.

In order to understand these effects, we have developed a stand-alone simulation, based on a two-dimensional model of the signal formation in silicon. This program has been interfaced with the Monte Carlo software used to study our physics reach. This integration allows us to have a more realistic model of the detector occupancy, crucial in trigger simulations, and also provides a more realistic implementation of the hit resolution achievable for different track angles of incidence. These studies allow us to map the achievable hit resolution for any given geometry as a function of the track incidence angle. They have also provided us with more accurate information on the hit multiplicity associated with a given track angle. We have used this more realistic information to achieve a better understanding of several key features of our detector performance.

Fig. 4.11 shows the resolution as a function of the incident beam angle for a pixel detector [1]. Two curves and data points are included in the figure: the solid line and circles show prediction and measurements done with an eight-bit ADC external to the pixel readout chip; the dashed curve and triangular data points illustrate the simulation and measurements obtained if we were only to use digital readout. The clear advantage of the analog readout is evident and for all incident angles, a resolution of better than 9μm has been obtained.

4.4.3 Pixel readout chip

4.4.3.1 Introduction

The use of the pixel detector data in the first level trigger means that the BTeV pixel readout chip must be capable of reading out all hit information from every beam crossing.

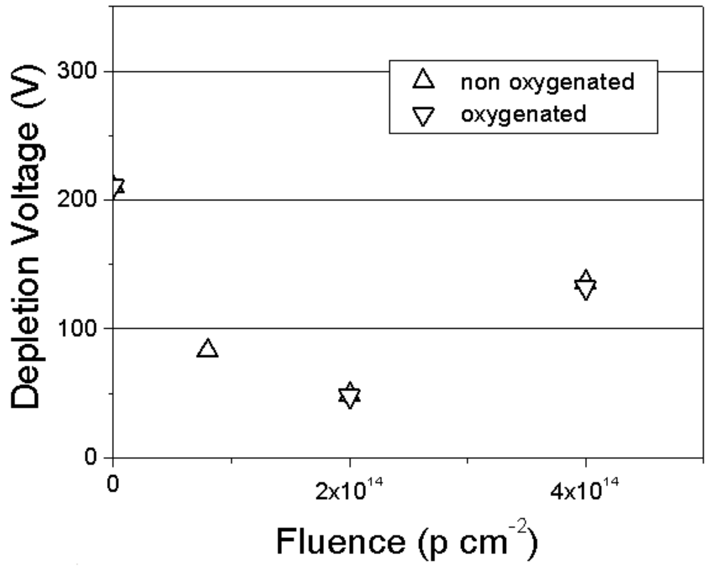

Figure 4.8: Full depletion voltage as a function of the fluences of the proton irradiation for normal and oxygenated p-stop sensors.

Furthermore, the pixel readout chip should be optimized for the bunch crossing time planned for the Tevatron operation when BTeV is running. It must be radiation hard so that it can be used close to the beamline. This requires a pixel readout chip with a low noise front-end, an unusually high output bandwidth, and implementation in a radiation-hard technology. During the last few years, a pixel readout chip has been developed at Fermilab to meet these requirements. This has been done through several stages of chip development, each of increasing complexity [9].

As described above, the baseline BTeV design calls for n^+ on n silicon sensors with appropriate guard ring structures for high voltage operation. These sensors provide adequate signals after significant radiation exposure, but also have rather large radiation-damage-induced leakage current. The BTeV pixel readout chip must be able to tolerate this leakage current at least up to 25-50 nA per pixel.

4.4.3.2 FPIX0 and FPIX1

An R&D program was started at Fermilab seven years ago whose goal was the design of a pixel readout ASIC for BTeV. The program envisioned a series of prototype pixel readout chips, each with specific engineering goals. The first two prototype chips, FPIX0 and FPIX1, were designed and fabricated with the migration to a radiation hard Honeywell 0.5 μm CMOS Silicon-On-Insulator (SOI) proecess in mind. Both chips have been extensively tested, both alone and bonded to a sensor. Furthermore, a beam test of pixel detectors using both chips was carried out at a test beam at Fermilab in 1999. As shown in Fig. 4.61 in

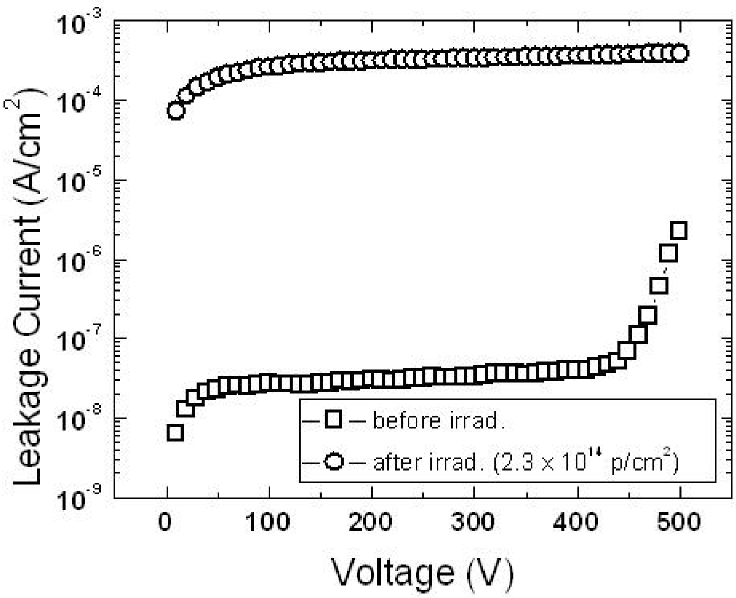

Figure 4.9: I-V curves for a FPIX1-sized p-spray sensor before and after irradiation up to 2.3×10^{14} p/cm^2. The measurements were performed at room temperature.

the "Performance" Section, the beam test results showed that for resolution, 2-bit ADC information will be adequate[1]. We have now chosen to have a 3-bit FADC for each pixel since this gives an extra margin as well as allows for better monitoring and control of effects due to the very non-uniform radiation dosage to the pixel detectors in BTeV.

The FPIX1 readout chip is the first implementation of a new column-based pixel architecture designed to meet the requirements of BTeV. The most stringent requirement is that all pixel hit information from every Tevatron crossing must be digitized and read out so that it may be used to form the primary trigger for the experiment. Simulations indicate that, with a 26.5 MHz readout clock, FPIX1 is capable of reading out an average of more than three pixels per beam crossing (BCO), assumed to be 132 ns. Relatively straightforward extensions of the FPIX1 architecture should increase the readout bandwidth by a factor of four or more.

FPIX1 was fabricated using the HP 0.5μ CMOS process. This choice was made in order to facilitate the production of a final BTeV pixel readout chip using the radiation hard Honeywell 0.5μ SOI CMOS process. This is costly and time consuming. Moreover, there is also an uncertainly about whether this process will be available when BTeV is ready for production. Thus, in May 1999, there were two outstanding issues in the design of the pixel readout chip. These were the number of ADC bits that would be needed to achieve the required resolution and the rad-hard technology. Since then, two positive developments have resulted in a much better understanding of the two issues. These two developments are the successful beam test mentioned above and the increasingly encouraging results on deep-

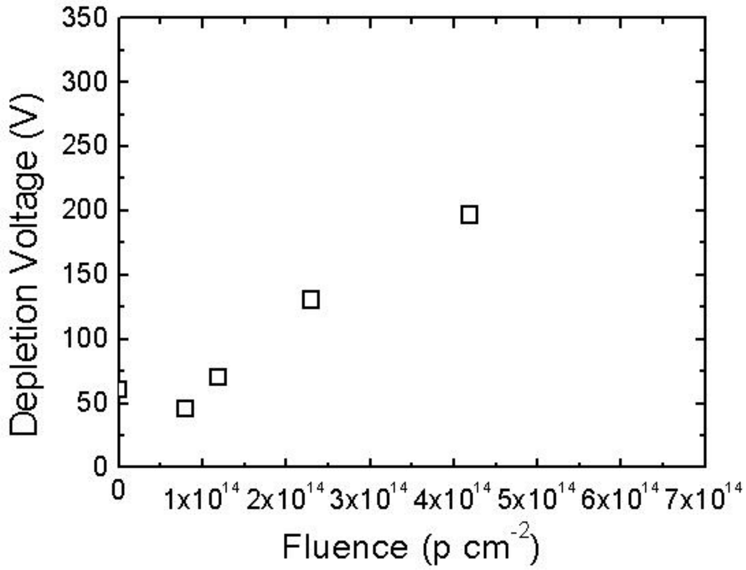

Figure 4.10: Depletion voltage as function of proton fluences for p-spray pixel sensors.

sub-micron CMOS process for readout circuit prototypes obtained at Fermilab and other places.

4.4.3.3 0.25 μm CMOS pixel readout chips

During the last few years, results from groups at CERN and Fermilab indicate that standard commercial deep-submicron (0.25 μm and below) CMOS processes are even more radiation hard than military processes such as the Honeywell 0.5 μm SOI, provided only that a set of special design rules is followed. We have chosen the 0.25μm CMOS process as the baseline technology for the pixel readout chip. A full prototype pixel readout chip (FPIX2), was submitted last Fall using this process. This chip follows the design philosophy developed in the earlier prototypes (FPIX0 and FPIX1), but incorporates new circuit design and implementation features appropriate for direct, radiation-hard use of the chips. The use of standard deep-sub-micron technology would allow for more rapid development cycles and reduced cost for the production quantities that we will need.

The development path of the pixel readout chip using the 0.25μm CMOS process included a number of submissions, implemented in two different commercial 0.25 μm CMOS processes following radiation tolerant design rules (enclosed geometry transistors and guard rings) [4]. The preFPIX2I chip, containing 16 columns with 32 rows of pixel cells, and complete core readout architecture, was manufactured by a vendor through CERN [10]. The preFPIX2Tb chip, contains, in addition to the preFPIX2I chip features, a new progamming interface and 14 digital-analog-converters (DAC) to control the operating and threshold settings of the whole chip. It was manufactured by Taiwan Semiconductor Manufacturing Company (TSMC). The last block to be tested was the high-speed data output serializer. This is

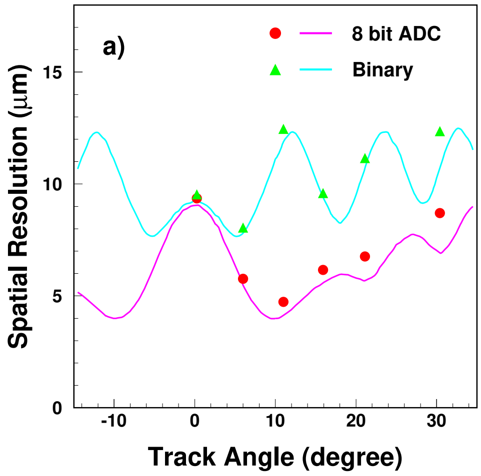

Figure 4.11: Resolution as a function of the angle of the incident beam. Data was taken with prototype pixel detectors during the 1999 Fermilab fixed target run. The detectors were instrumented with the earliest versions of the pixel readout chip FPIX0 at Fermilab. The curves represent the predicted resolution: the oscillating curve is the simulated digital resolution and the lower one assumes 8-bit charge digitization. The circles and triangles are extracted from the data.

needed to minimize the number of output signals, without compromising the high readout bandwidth. This was implemented in a small serializer test chip, again manufactured by TSMC.

An important feature of the preFPIX2Tb chip is the implementation of on-chip DAC's in order to minimize the number of external I/O lines. The change of the DAC behavior due to the proton irradiation has been measured and is shown in Fig. 4.12. The three curves shown correspond to the deviation from the linear fit to the unirradiated data for total dose of 0, 14, and 43 Mrad. It can be seen that the linearity and accuracy of the DAC output remains acceptable after 43 Mrad total dose.

To study total dose and Single Event Effects (SEE), samples of these prototype chips have been exposed to 200 MeV protons at IUCF. The comparison of the chip performance before and after exposure shows the high radiation tolerance of the design [6]. Chips have been exposed to as much as 2×10^{15} protons-cm^{-2} (about 87 Mrad) and no evidence of catastrophic failure or deterioration of the functionality of the readout chip has been observed. In particular, no radiation induced SEE, such as Latch-Up or Gate-Rupture has been observed. After heavy irradiation, the prototype pixel readout chip shows little change in noise and threshold dispersion[6]. The comparison of the chip performance before and after exposure (Fig. 4.13) shows the high radiation tolerance of the design. Fig. 4.14 shows the time walk after 43 Mrad of irradiation. Between a threshold of 1000 e^{-} and a threshold larger than

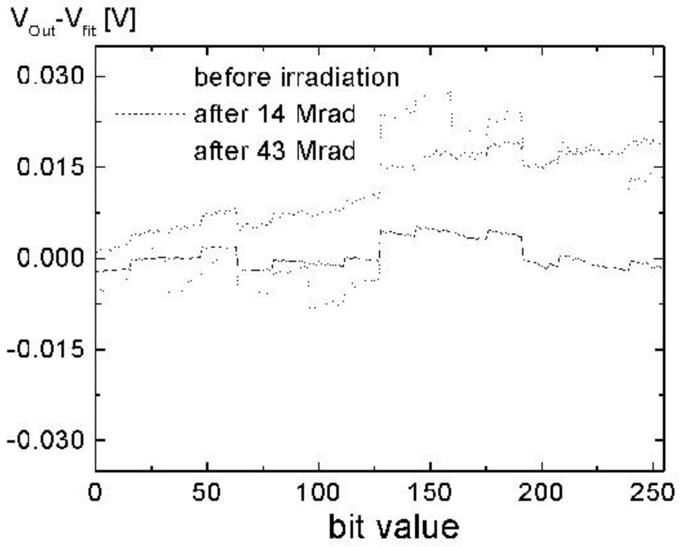

Figure 4.12: DAC analog response before and after 14 and 43 Mrad total dose exposure to 200 MeV protons. The full scale (255 counts) corresponds to about 1.7V

$4Ke^-$, the measured timewalk is about 50 ns, certainly more than adequate even with a BCO of 132ns. We verified, at the required high speed and low power consumption, the complete functionality of our design up to total dose of 87 Mrad of 200 MeV protons. We tested all circuit blocks implemented in several prototype chips: the pixel cell, the data-driven and column-based readout architecture, the on-chip digital-analog converters, the programming interface, and the 140Mbit/s data output serializer. In particular, we show in Fig. 4.15 the good quality of the 140Mbit/s eye-pattern of on-chip LVDS drivers driving 50 foot cable. This implies that repeaters between the pixel detector and the data combiner boards located behind the magnet will not be needed.

In the BTeV operating environment, an intense radiation field will be present, which can induce Single Event Upsets (SEU) in the data transmission. These soft errors can result in data corruption, equivalent to digital noise, and loss of driver-receiver synchronization, introducing readout dead time. We have measured extensively the SEU cross section of the static registers implemented in the readout chip (mask and charge-injection registers, DAC registers, and serializer registers), and the radiation induced error rate of the data output serializer running at the nominal speed of 140Mbit/s. The measurements consisted of detecting bit error rates in the static registers controlling the readout chip front-end operating conditions and the pixel cell response. The single bit upset cross-section measured for the DAC's located on the chip periphery was $(5.5 \pm 0.6 \pm 0.5) \times 10^{-16}$ cm^2 while for the

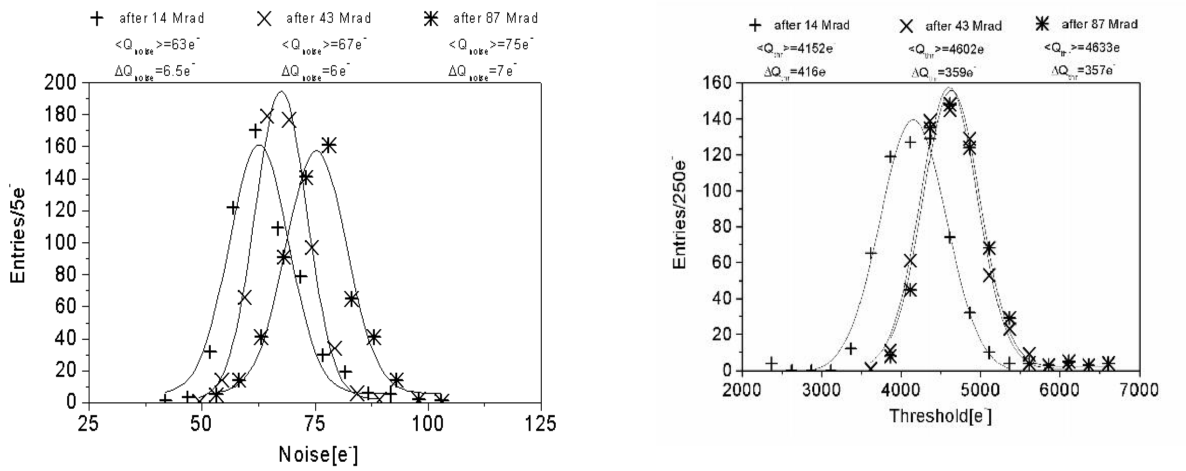

Figure 4.13: Noise and threshold distributions of BTeV prototype $0.25\mu m$ CMOS pixel readout chip after irradiations to 14, 43, and 87 $Mrad$. For comparison, before irradiation, the mean noise and threshold dispersions were measured to be 106±4 e$^-$ and 345e$^-$ resepctively.

mask and charge-injection registers located inside each pixel cell was $(1.9 \pm 0.2 \pm 0.2) \times 10^{-16}$ cm^2 (where the first error is statistical and the second systematic due to uncertainty in the beam fluence) [7]. We tested and did not observe any dependence of the upset rate on the beam incidence angle or clock frequency up to 16 MHz. Our measurements of the SEU rate implies that the SEU bit error rate in the BTeV pixel detector operating at the nominal luminosity is small enough that it will not be necessary to design explicitly SEU tolerant registers. Rather, the SEU rate can be comfortably handled by a periodic readback of the chip configurations during data-taking and a download of the chip configuration whenever an upset is detected.

Based on the experience gained, we have moved on to a full-size BTeV pixel readout chip (FPIX2). This chip has 22 columns by 128 rows and includes all features of the preFPIX2Tb chip and the high speed data output interface which accepts data from the pixel unit cell and the column logic, serializes the data, and transmits the data off chip. We received at the end of 2002 about 20 wafers. For this submission, we had three different versions of the front-end design. Starting from Version A which is an improved and optimized (to the TSMC process) design of the preFPIX2tb, we added modifications to the discriminators (version B), and then further modfications to the second stage of the preamplifier. First results from bench tests of these chips are very impressive. All versions seem to be working fine. Fig. 4.16 shows the noise and threshold dispersion of version C of this chip. We have recently completed the probing of five wafers of the FPIX2 chip. The tests include powering up, checking of the

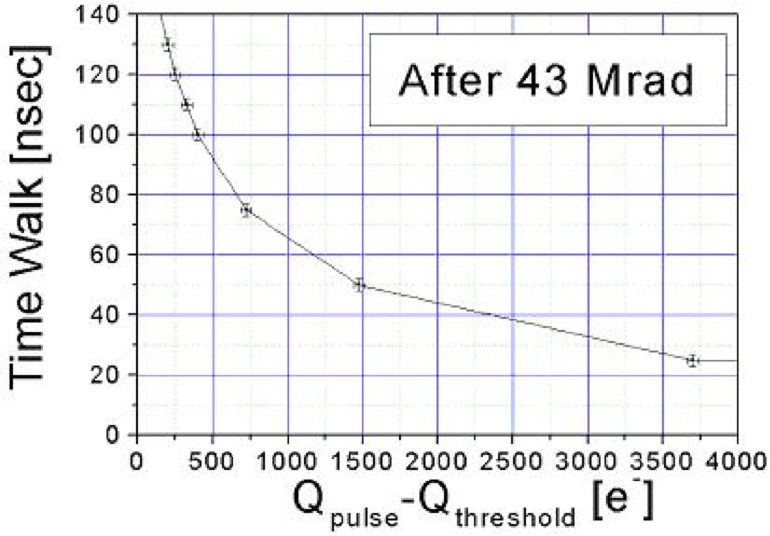

Figure 4.14: Time-walk of an irradiated preFPIX2Tb chip after a fluence of 43MRad

Figure 4.15: 140Mbits/s eye-pattern of on-chip LVDS drivers driving 50 foot cable

voltage and current levels during quiet state and during operation, loading and reading back of pattern at high clock speeds using one or more serial lines. The yield is excellent, well above 90%. The design appears to be acceptable for the final BTeV pixel system, pending on tests (both bench and beam test) with sensor bump-bonded to it before and after irradiation.

4.4.4 Bump bonding development

The BTeV pixel detector, like all other pixel systems used in or planned for HEP experiments, is based on a hybrid design. With this approach, the readout chip and the sensor array are

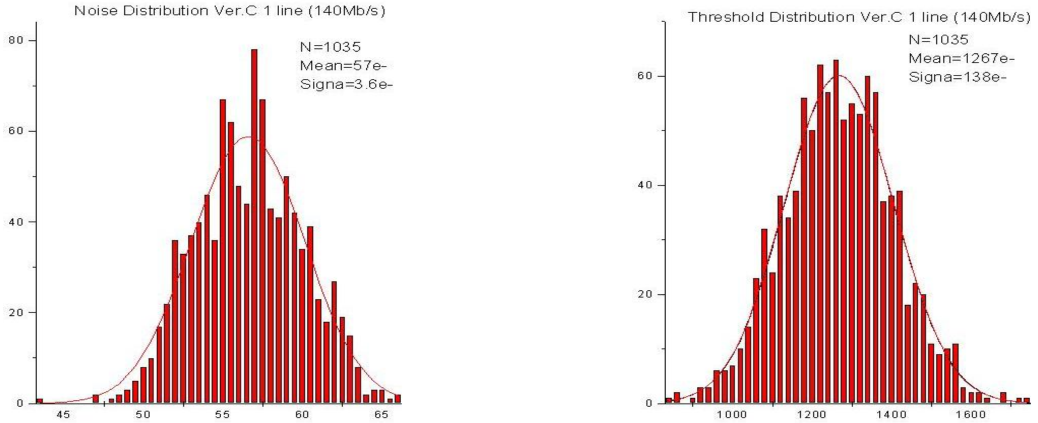

Figure 4.16: Noise and threshold distributions of BTeV FPXI2 pixel readout chip

developed separately and the detector is constructed by flip-chip mating the two together. This method offers maximum flexibility in the development process, choice of fabrication technologies, and sensor materials. However, it requires the availability of a highly reliable, reasonably low cost fine-pitch flip-chip attachment technology. The technology has to be able to fulfill the following requirements:

- small bump - the typical bump diameter and height for our pixel detector is between $10 - 12\mu$m.
- fine pitch (50μm)
- high yield - a defect rate of better than 10^{-3} is required.

We have focused our study on two options: indium bumps, and Pb-Sn solder bumps.

A series of yield and stability tests were performed on bump-bonded test structures. These tests were done with indium, fluxed-solder, and fluxless-solder bumps from a number of commercial vendors. Our tests have validated the use of indium and fluxless-solder as viable technologies. The failure rate obtained from this large scale test is about 2×10^{-4} which is adequate for our needs [11].

In order to check the long term reliability of the bump-bonding technology, we monitored the quality of the connectivity over a period of one year. In addition, we performed thermal cycling (exposure to -10^0C for 144 hours and $+90^0$C for 48 hours in vacuum). Furthermore, we irradiated some of these test structures with a ^{137}Cs source up to a dose of 13 Mrad. The typical failure rate of both types of bumps under these stringent tests was found to be a few $\times 10^{-4}$. These results show that both techniques are highly reliable [12].

One of the remaining concerns is thermal stress on the bumps due to the coefficient of thermal expansion (CTE) mismatch of the bump material, silicon, and the substrate material on which the detector is placed. Questions still remain on the long-term reliability of the bumps due to thermal cycle effects, senstivity to low temperatures, attachment to a substrate with a different CTE, and radiation.

We have carried out studies on effects of temperature changes on both types of bump bonds by observing the responses of single-chip pixel detectors and a five-readout-chip pixel detector assembly exposed to a ^{90}Sr source. After going through 60°C thermal cycles, the hit maps, the responses of the single-chip pixel detectors to a radioactive source as a function of temperature indicated that basically all channels remain active after many thermal cycles. There is indication that a small number of pixels (about 0.3%) become slightly more noisy after thermal cycling for detectors using indium-bumps. With solder bumps, we have not observed any change.

We have also studied the strength of the bumps by visual inspection of the bumps bonding silicon sensor modules to dummy chips made out of glass. There, the bumps were clearly visible and we could observe any deformation of the bumps after thermal cycles and irradiation (figs. 4.17 and 4.18). While we have not observed any shorts or bridges, we do see changes in both indium and solder bumps at the level of 0.3% and 0.5% respectively. We are still investigating with the vendors on the possible causes of the changes observed and their significance [13]. In summary, both indium and Pb-Sn solder bumps are viable technologies and we have qualified three vendors.

The other uncertainty is wafer thinning. For material budget reasons, we would like to have the readout chip wafers thinned down to 200 μm. One challenge to the bumping process is wafer thinning. After the CMOS fabrication sequence, the wafers may be reliably thinned to 100 μm or even lower, before the bumping process. There has been a lot of experience in this with the SVX chips which are thinned down to 300 μm. However, the bumping of thinned wafers is technically very difficult. There is significant risk of damage to the thinned wafers during the multi-processing steps required for wafer bumping. Also, the thinned wafers may pose processing challenges during photolithography. This is particularly true in our cases where fine pitch and small bumps are required. There are two approaches to solve this problem.

The first approach is to process the thinned wafers through the bumping sequence by temporarily attaching them to a wafer carrier with an appropriate polymer (adhesive). The risks associated with this method are basically solvent attack on the polymer layer during any of the process steps.

The second approach is to thin the wafers after bumping. This requires protection of the bumped surfaces during the thinning process. We are currently working with three bump-bonding vendors to test both approaches. A large scale qualification program is underway and we expect results will be available some time during 2004.

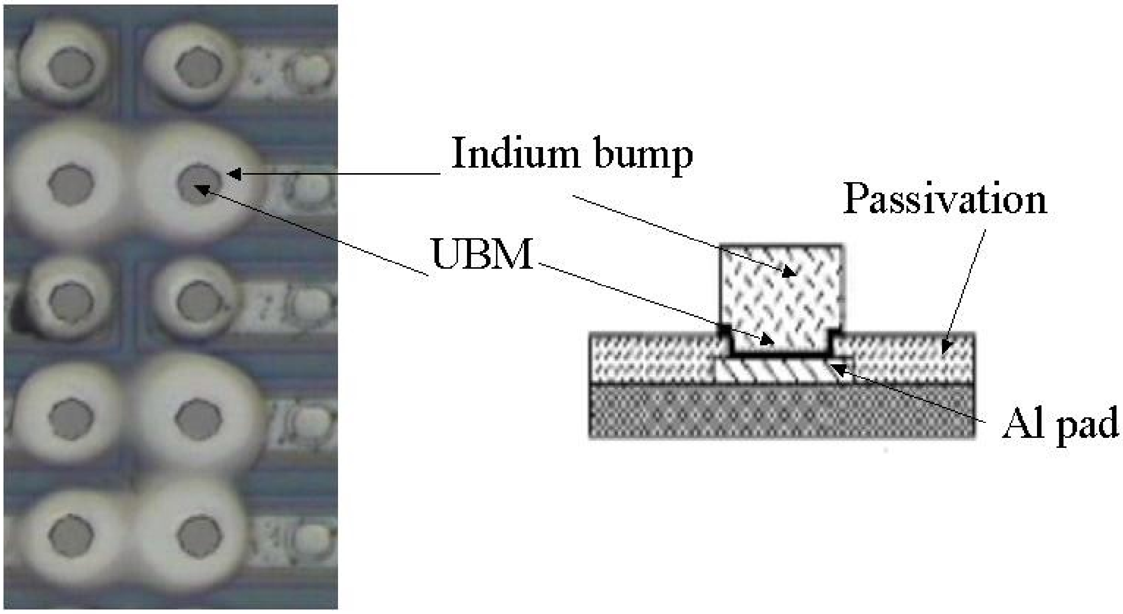

Figure 4.17: Sketch showing cross-section of indium bumps on the right. On the left is shown a picture under optical microscope of a region of the glass-Si module where the bumps are clearly visible.

4.4.5 Multichip Module

Each pixel readout chip includes a high density of control and data output lines at the periphery. These lines need to be connected to the back-end electronics. A full set of pads is available on the readout chip for these interconnection purposes. This is achieved through a high density, low mass flex circuit wire bonded to a number of readout chips to form a multichip module.

Each pixel half-plane will be made up of a number of these multichip modules. The module is the basic building block of the pixel detector system. Each pixel module is composed of three layers. One of the layers is formed by the readout integrated circuits (ICs) which are flip-chip bump-bonded to the pixel sensor. A low mass flex-circuit interconnect is glued either on the top of or underneath this detector assembly, and the readout IC pads are wire-bonded to the flex-circuit. Fig. 4.19 shows the pixel module with the HDI glued to top of the detector assembly.

4.4.5.1 First prototype

Figure 4.20 shows a picture of the first prototype of the pixel module. It is composed of a pixel sensor bump-bonded to five FPIX1 readout chips and a four layer high density flex circuit made by Fujitsu Computer Packaging Technologies (FCPT, San Diego). This flex circuit has line traces of 20 μm in a 40 μm pitch, copper line thickness of 5 μm, vias spaced by 200 μm, via cover pads of 100 μm and average via hole diameter of 26 μm. In this

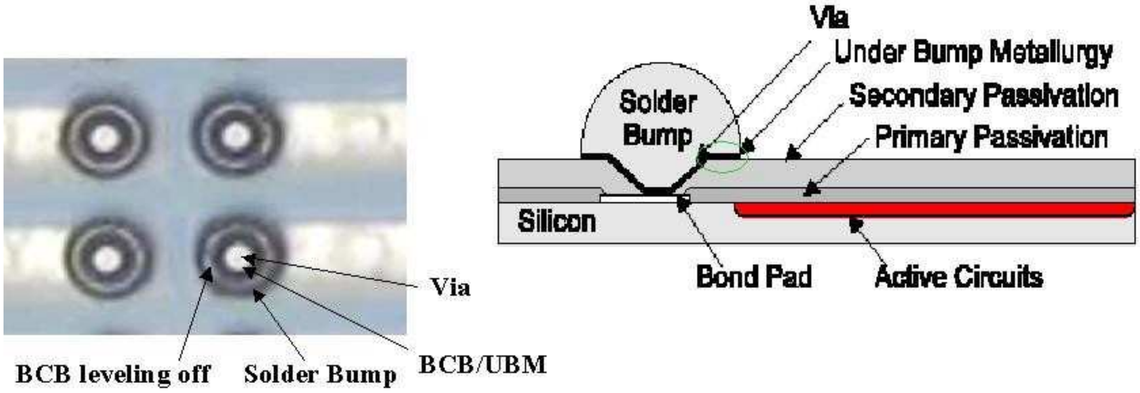

Figure 4.18: Sketch showing cross-section of solder bumps. On the left is shown in detail a few bumps as seen under the microscope of a glass-Si module.

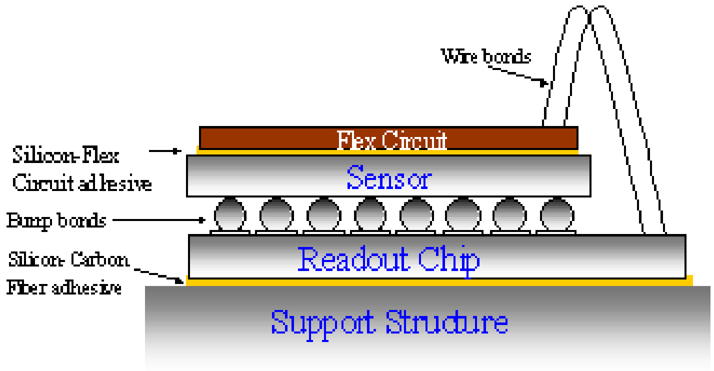

Figure 4.19: Sketch of the second pixel multichip module stack

prototype the flex interconnect is located on the side of the readout chips instead of on the top of the sensor or underneath the readout chips (as in the baseline design described below). The pixel sensor used is oversized; it can be bump-bonded to a total of 16 readout chips.

The threshold and noise characteristics of this pixel module have been studied. These characteristics were measured by injecting charge in the analog front end of the readout chip with a pulse generator and reading out the hit data through a logic state analyzer. The comparison of these test results with the results of a single FPIX1 chip shows no noticeable degradation in the noise and threshold characteristics of the chip. Furthermore, tests with a deadtimeless mode, where the charge injected into the front end is time-swept in relation to the readout clock also does not reveal any degradation in performance, indicating no crosstalk problems between the digital and analog sections of the FPIX1 and flex circuit.

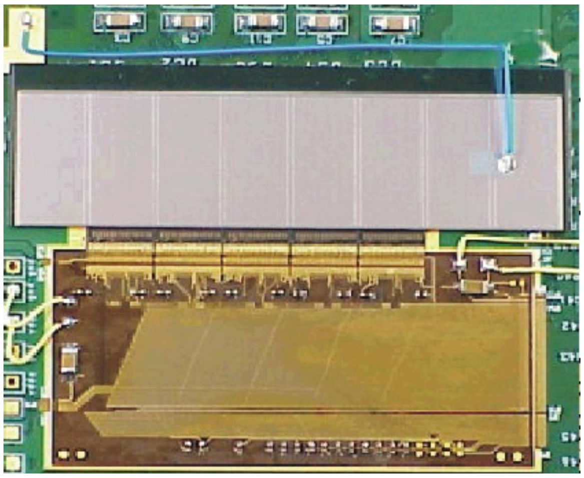

Figure 4.20: The first prototype pixel 5-chip module

4.4.5.2 Second prototype

This prototype is composed of the three layers as described in Fig. 4.19. It also used the FPIX1 chips. The goals for this development were to assess the electrical and mechanical performance of such assembly, as well as to acquire insights into the construction process and yield. The prototypes built include four five-chip modules (two with sensors and two without). We have also tested the HDI by comparing the performance of single chip detectors read out using the HDI and a standard printed circuit test board.

The FPIX1 interface with the data acquisition system was not optimized to reduce the number of interconnections. The large number of signals in this prototype imposes space constraints and requires aggressive circuit design rules, such as 35μm trace width and trace-to-trace clearance of 35μm and four metal layers. A circuit with such characteristics is very difficult to obtain and very few places have such manufacturing expertise. The Engineering Support and Technical Division at CERN manufactured the FPIX1 interconnect flex circuit. Fig. 4.21 shows a picture of the flex circuit. Several design strategies to minimize electrical noise and guarantee signal integrity were incorporated in the layout and are being evaluated.

The interface adhesive between the flex-circuit and the pixel sensor has to compensate for mechanical stress due to the coefficient of thermal expansion mismatches between the flex circuit and the silicon pixel sensor. For this prototype phase, we chose to use a conductive silver epoxy. Figure 4.22 is a picture of a five-chip module that we have assembled and tested.

These modules were characterized for noise, threshold dispersion and their variances. These characteristics were measured by injecting test charge into the analog front end of the readout chip with a pulse generator. The results for various thresholds are summarized in Table 4.1 and 4.2 [15]. These results are comparable with previous characterization results of single readout IC mounted on a printed circuit board. No crosstalk problem has been observed among the digital and analog sections of the readout chip and the flex circuit.

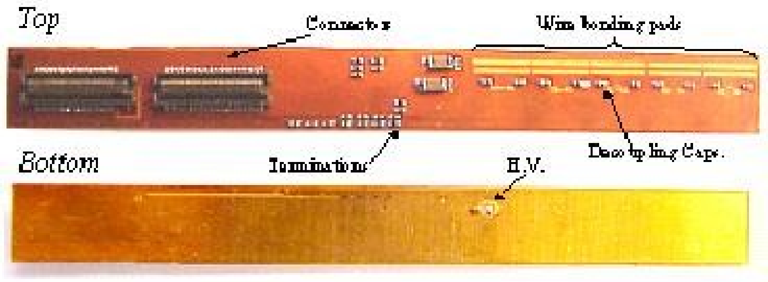

Figure 4.21: Picture of the flex-circuit made by CERN.

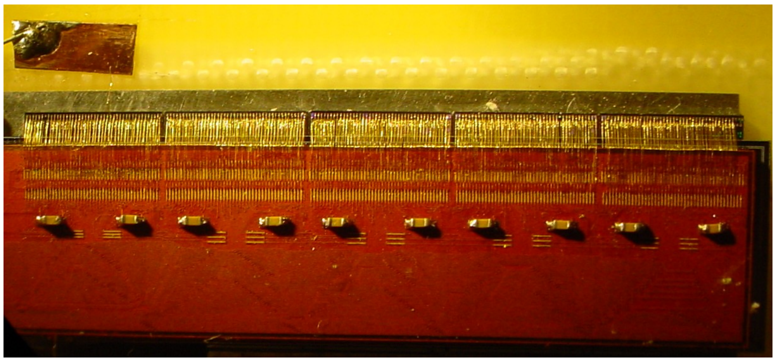

Figure 4.22: The second prototype pixel 5-chip module

The connectivity of the bump-bonds was tested by shining a radioactive source (^{90}Sr) onto the sensors, while the absolute calibration of the modules is achieved using X-ray sources. Figure 4.23 shows the hit map of a five-chip module using a ^{90}Sr source. This figure shows that most of the bump-bonds in the module are functioning, although chip 3 has a bad column (traced to be a digital control logic defect in this particular readout chip), and chip 5 has several broken bump-bonds. However, for this prototyping phase, none of the chips were tested before the flip-chip mating process. We plan to do wafer probing and use only known-good-dies for all future assemblies including production. For this prototype module, the threshold dispersion is $380e^-$, while the noise mean is around $260e$. These results are comparable to the single chip with no sensor used as a benchmark in these tests.

4.4.5.3 Third Prototype

This prototype is designed for the pixel modules using the FPIX2 chips. Based on the experience of the first two prototypes, we realized that placing the HDI on top of the pixel module would pose serious technical challenges to the design of the HDI and the assembly of the module. In this design concept, the width of the HDI is limited to a little narrower than the width of the sensor module (8.4 mm). This in turn means narrow line width and spacing and rules out the possibility of having one HDI for an 1x8 pixel module. For the assembly, with the HDI on top of the sensor module, we have found that it is difficult to

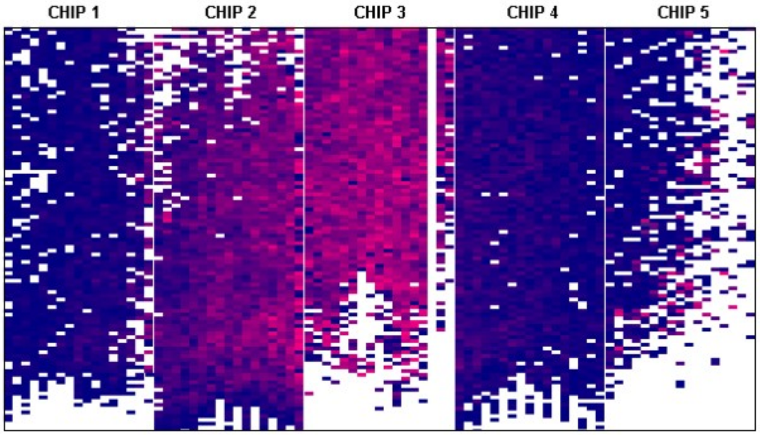

Figure 4.23: Hit map produced by a radioactive source moved from spot to spot.

Single bare chip				*Single chip with sensor*			
μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}	μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}
7365	356	75	7	7820	408	94	7.5
6394	332	78	12	6529	386	111	11
5455	388	79	11	5500	377	113	13
4448	378	78	11	4410	380	107	15
3513	384	79	12	3338	390	116	20
2556	375	77	13	2289	391	117	21

Table 4.1: Performance of the one-chip FPIX1 module without and with sensor. All numbers are given in equivalent electrons. There is no significant increase in noise and threshold dispersion with the sensor attached.

connect the HV bias to the sensor since the bias pad would be covered by the HDI. Also, wire bonding of the HDI to the readout chips is potentially dangerous to the bump bonds holding the sensor to the readout chips. Lastly, our experience with pixel modules based on FPIX1 chips showed that for stable operation, the chips would need to be sitting on top of a ground plane. With this design, the chips will be sitting on the substrate and a solid ground plane may not be easily achievable.

These concerns lead us to a new alternative design which puts the HDI on the bottom of the readout chips. In so doing, all the previous concerns will be removed. The HDI can now be wider (up to 11 mm), making the design less challenging and feasible for an 1x8 pixel module. The readout chips will now be sitting on the HDI which has a solid ground plane as the top layer. Assembly of the module will also be much simpler. One of the remaining issue is that the part of the HDI which sticks outside the readout chip is not wide enough to provide space for both the wire bond pads and the fast decoupling capacitors. This is usually desirable to provide high frequency filtering (low inductance connection) for the low voltage

Chip 1		*Chip* 2		*Chip* 3		*Chip* 4		*Chip* 5	
μ_{Th}	μ_{Noise}	μ_{Th}	μ_{Noise}	μ_{Th}	μ_{Noise}	μ_{Th}	μ_{Noise}	μ_{Th}	μ_{Noise}
7204 ± 352	267 ± 17	8241 ± 396	226 ± 28	7328 ± 388	215 ± 20	7324 ± 395	181 ± 10	7146 ± 391	240 ± 24
6760 ± 381	307 ± 23	7123 ± 400	232 ± 18	6253 ± 403	217 ± 20	6226 ± 383	184 ± 11	6150 ± 404	250 ± 26
5364 ± 359	262 ± 19	5900 ± 412	225 ± 19	5250 ± 400	230 ± 19	5124 ± 380	181 ± 12	5020 ± 420	243 ± 24

Table 4.2: Performance of the five-chip FPIX1 module. All numbers are given in equivalent electrons.

supplies to the chips. Characterization tests with the pixel module prototypes will determine if such capacitors are indeed necessary, since the HDI has a power and a ground plane that will act as a capacitor (~800 pF) and the HDI has decoupling capacitors located near the connector. Nevertheless, if necessary, the extra capacitors will be located at a "mezzanine" flex circuit assembled on top of the sensor, as shown in Figure4.24. The first prototype pixel module with this stack concept has a connector to interface the pixel module to the PIFC (fig.4.25). Future prototypes will connect the HDI to the PIFC via wire bonds. This new HDI will be available for testing in Spring 2004. The corresponding PIFC (both data and power flex cables) have been designed, submitted for fabrication, and will be available for testing soon.

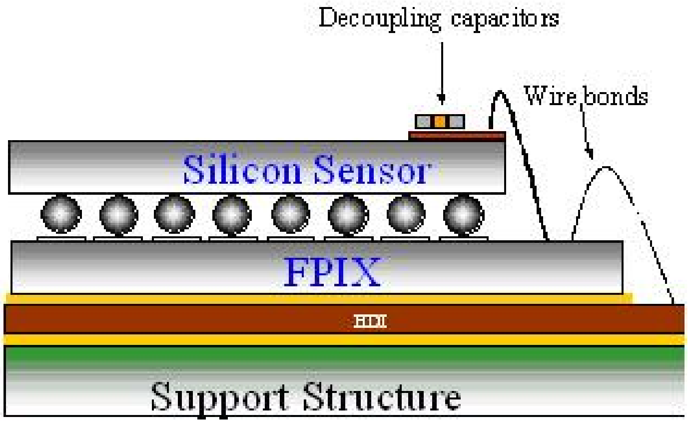

Figure 4.24: New design for the third prototype pixel multichip module

4.4.6 RF shielding issues

The pixel detector will be installed inside the beam vacuum enclosure in the C0 interaction region. This raises concerns both for the operation of the pixel detector, and for the operation of the Tevatron collider. The bunched Tevatron beam could potentially excite microwave resonances in the pixel vacuum enclosure. If high Q resonance modes exist, they could destabalize the circulating beams. High microwave power in the vacuum box might also interfere with the operation of the pixel detectorF.

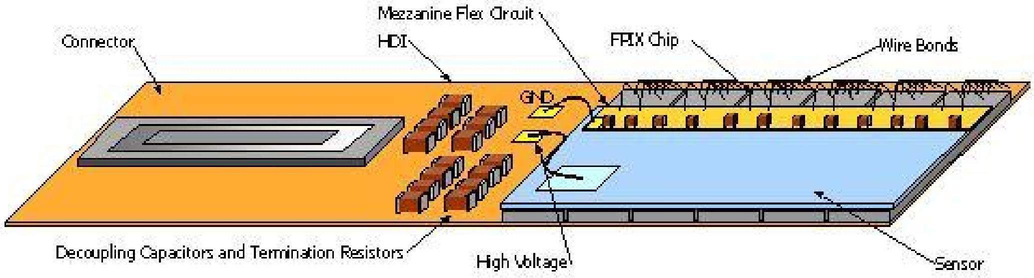

Figure 4.25: Sketch showing the new 6-chip module prototype

4.4.6.1 Beam simulator test

In order to better understand these issues, we have built an apparatus to simulate the pixel vacuum vessel in the Tevatron (see Fig. 4.26). The basic structure of the test apparatus is a rectangular box made out of aluminum with two narrow diameter pipes at either end. The box and the two pipes are simplified full size models of the pixel vacuum vessel and the beam pipes outside the pixel region. In the center of the setup, a thick wire (8 mil Cu/Be) or an Aluminum tube was strung through the whole length of the box and pipes. A series of strong rf pulses, which mimic the Tevatron bunches, can be sent down the central wire or tube and the resonance structure of the apparatus can be measured with a network analyzer.

As is shown in Fig. 4.27, a series of strong resonances exist at frequencies above 1 GHz. These resonances are suppressed by more than three orders of magnitude by the addition of eight 5 mil Cu/Be wires surronding the central wire. These test results have been reviewed by the Fermilab Accelerator Division. The reviewers concluded that a set of wires similar to those used in the test apparatus would be sufficient to ensure that resonances in the pixel vacuum vessel would not limit the Tevatron performance. The review panel also noted that the BTeV pixel vacuum vessel will contain a large amount of dielectric material (cables, etc.) that was not included in our test apparatus. This material will also tend to de-Q resonance modes and reduce the potential for problems[16][17].

We will continue to investigate various shielding configurations. We will also test the operation of prototype modules using this setup.

4.4.7 Mechanical support, cooling and vacuum system

4.4.7.1 Introduction

The mechanical support design for the BTeV pixel detector system is dominated by the dual needs to have a stable and repeatable set of detector positions and to keep the amount of material to a minimum. These requirements are motivated by the consequences for the physics goals of BTeV of resolution smearing in both space and mass. The former of these is the most critical, since it influences many elements in the final capability of BTeV: separation

Figure 4.26: Picture showing the beam simulator. The inset on the top right corner shows the central wire and the ring of surrounding wires.

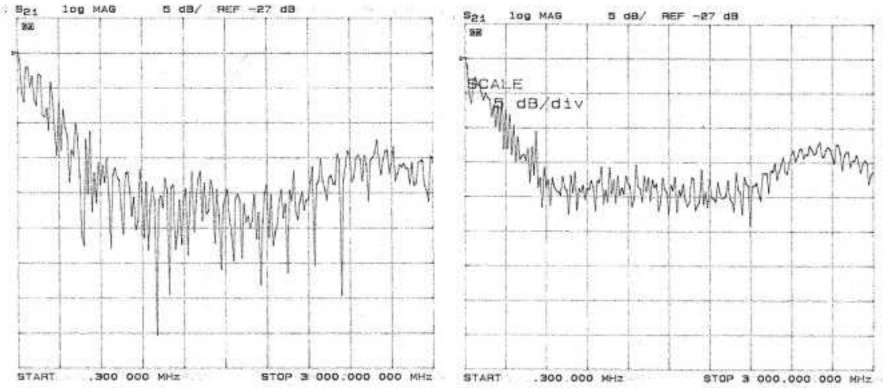

Figure 4.27: Results of the measurements with no wires (left) and with 8 thin wires shielding the central wire carrying the signal from the network analyzer.

of decay vertices from interaction vertices, trigger efficiency and enrichment, signal to background levels, proper time resolution, and sensitivity to multiple interactions per crossing. The mass resolution is also important, but mostly influences just the signal to background quality of BTeV data.

The pixel detector should be as close to the beam as possible to minimize the extrapolation distance from the first measured hit to the primary vertex. The pixel modules will be precisely placed on a support substrate which will also provide cooling to the detectors. The substrate will have a notch built in to allow the beam to pass through. The pixel detector needs to be retractable to a distance of ± 2 cm from the beam while the collider is being filled and until the beams are brought to their final stable configuration. For this, a set of actuators and position sensors are required. Because of this dynamic aperture (separation) between the beams and the detector, the pixel stations will be placed inside a vacuum vessel. For the data, control and power signals I/O, we need to have a large number of vacuum feed-throughs. Significant progress has been made on the engineering design of the overall mechanical support, the vacuum vessel, motor drive assembly, and the individual substrates on which the pixel modules will be mounted. In some cases, early prototypes have been made and evaluated.

Major assembly steps have been worked out for the current baseline design. The mechanical stiffness of all the important elements such as the substrate mounting brackets, C-fiber support cylinder, and vacuum vessel were checked with finite-element-analysis (FEA) calculations to make sure that any deflections and stresses under load are acceptable.

Work has also started on the vacuum system design. One of the first tasks is to understand the gas load. We have built a 5% mock-up pixel system using as close as possible the same material as the real detector and measured the outgassing rate as a function of operating temperature. Prototype printed circuit boards for signal feed-through in and out of the vacuum vessel have been tested and the results validate our conceptual design. To check the robustness of the high density flex circuits after multiple flexes due to the movement of the pixel detector in and out the beam, cable flexing tests have been carried out including tests at low temperatures and after heavy irradiation. Initial results show the cables can withstand a large number of flexes ($10,000$ times) without any deterioration in performance.

4.4.7.2 Carbon support structure

The pixel stations require a very lightweight and rigid support structure, constructed to tight mechanical tolerances. Furthermore, the structure should have no long term deformations and can keep the alignment precision over a long period of time. Carbon fiber composite provides the best combination of low density and rigidity along with ease of manufacturability. To verify the FEA calculations, the manufacturing process, and assembly procedure, prototype support half-cylinders and support brackets were made using carbon fibers. Dummy aluminum substrates were then mounted (see Fig. 4.28) to the cylinder using the brackets on a coordinate measuring machine table. Known loads were then applied to the substrate and the deflection of the brackets were measured. Good agreement with the FEA results were obtained. To check the long term deformations and creep effect caused by small temperature gradients, we have studied using novel techniques such as Electronic Speckel Pattern Interferometry (ESPI), Fiber Bragg Grating (FBG) methods the displacement of the prototype carbon support structures.

A few ply lay-ups have been checked to identify a lay-up with highest possible modulus of elasticity and smallest coefficient of thermal expansion. Finally a 6-layer [0/45/90/90/-45/0] lay-up was chosen for building a full scale support structure prototype. To build this prototype, the material used is 76 μm thick K139/BT250E-1 55 gsm prepreg (carbon fiber pre-impregnated with epoxy) made by BRYTE Technologies, Inc. This prototype has been

Assembled Half- Plane Prototype

Two Installed Half- Plane Prototypes

Figure 4.28: Picture shows aluminum dummy substrates supported by brackets made out of carbon fiber on to a carbon support frame.

completed. We are now working on a mounting fixture and a program to test the structure. This prototype will be mechanically and thermally tested to check whether the measurements are consistent with FEA predictions.

The mechanical stability of the pixel station can be monitored by use of FBG sensors. FBG sensors are optical fiber sensors acting as strain gauge, with unrivalled long-term stability, electromagnetic field insensitivity, mass lightness and radiation hardness. Use of FBG sensors can provide, during data acquisition, real time monitoring of the deformations occurred by the mechanical structures that hold and keep in position pixel detectors.

Use of FBG sensors and ESPI was adopted to test the carbon support half-cylinder structure reduced-size prototype. The measurements were intended to test the structural behaviour of the half-cylinder with respect to both thermal and mechanical stressing, thus characterizing both structural design and the production materials. The results would then be used to plan extended tests on the full-size prototype, with the aim of developing a complete system based on FBG sensors that will provide real-time monitoring of the final support half-cylinder structure during the operation and running of the experiment. The results obtained from the first set of tests show that detector position monitoring can be efficiently worked out by supporting structure deformation analysis [18, 19]. Specific investigations will show the feasibility of embedding FBG sensors in the composite materials of BTeV mechanical structure. Such an option will be considered as a valid alternative to gluing the FBG sensors on the surface of the structure.

4.4.7.3 Substrate

Each pixel half-station is assembled on two substrates, with the pixel modules placed with a small overlap on both surfaces of the substrate to provide complete coverage of the active area. For a number of years, the baseline design was to use a substrate made out of a novel material called "fuzzy carbon" with a number of embedded cooling tubes made out of glassy carbon. However, fuzzy carbon is very fragile and is made by a proprietary process owned by a single vendor. More importantly, such a design will have a large number of cooling joints and pipes containing coolants placed inside a vacuum system. The reliability and the risk of a leak in the system is a subject of grave concern. On another front, the outgassing tests of a 5% model of the pixel detector at various temperatures suggested that the use of a cryogenic panel at -160°C might provide sufficient pumping to achieve the required vacuum level. The presence of the cryogenic panels and liquid nitrogen lines inside the pixel vacuum vessel provides a convenient heat sink. Cooling for the pixel substrate can now be done by conduction without the need of flowing coolant through the substrates. We will then have a joint-free and leak-tight cooling system. A material with very high thermal conductivity is needed for this kind of heat transfer mechanism in order to minimize the temperature gradient across the substrate. After some preliminary study among carbon-carbon, carbon-fiber reinforced plastics, carbon foam, flexible pyrolytic graphite sheet (PGS) and thermal pyrolytic graphite (TPG), TPG was chosen because of its outstanding thermal properties and low radiation length. To avoid any stresses due to the difference in CTE amongst the various materials that will be used (e.g. TPG, carbon fiber, LN_2 tubes, cooling blocks), the more flexible and light weight PGS will be used to connect the TPG substrate to the cooling blocks. TPG is a unique form of pyrolytic graphite manufactured from the thermal decomposition of hydrocarbon gas in a high temperature, chemical vapor deposition reactor. Pressure and thermal annealing are then performed in order to enhance its thermal properties as desired. The thermal conductivity of TPG, after this sort of annealing, can be as high as 1,700 W/m-C at room temperature. This property is temperature dependent, and it even surges to a peak of about 3,000 W/m-C at -160°C. TPG is currently used by the ATLAS SCT barrel modules and outer forward silicon modules. It has also been used by HERA-B and AMS and is proven to be a good candidate for such a substrate design.

The fundamental heat removal mechanism in this design is conduction. The conceptual design of the TPG substrate is shown in Fig. 4.29 and Fig. 4.30. The pixel modules are placed in an alternative stagger pattern on both surfaces of the TPG substrate to provide full coverage. The TPG substrate can be divided into two working areas. The first is the active or heat source area in the middle of the substrate where the pixel modules are placed. The second is the extended area that provides the needed channel between the active area and the heat sink.

Material budget is always minimized in the substrate design. TPG has a radiation length of about 18.9 cm while for the flexible PGS, it is about 42.7 cm. The thinner the material, the higher the temperature gradient across the substrate will be. Since temperature gradient will generate thermal stresses and displacements in turn, the TPG substrate cannot be too thin and these stresses and displacements should be kept within acceptable limits. The work on the TPG is divided into four key areas:

- Thermal/structural modelling
- Study of Material properties
- Substrate design issues
- System issues and manufacturability

The goal in the thermal/structural modelling and substrate design is to identify the thickness of the substrate based on the balance of material budget and thermal performance, and to verify whether the corresponding thermal displacements and stresses are acceptable. Finite Element Analysis (FEA) was used as a design tool to investigate the different configurations and to study possible temperature stability control methods.

Based on the material budget requirement, the thickness of the substrate is the key parameter in the substrate design Through the FEA calculations, we have established that a configuration with cooling at two ends of a TPG substrate arranged vertically with a uniform thickness of 0.38 mm (corresponding to 0.20% X_0) would meet our needs. This is shown schematically as in Fig. 4.29. This would generate a temperature gradient across the active area of the X and Y-measuring planes of about 15.1°C and 8.4°C respectively [20].

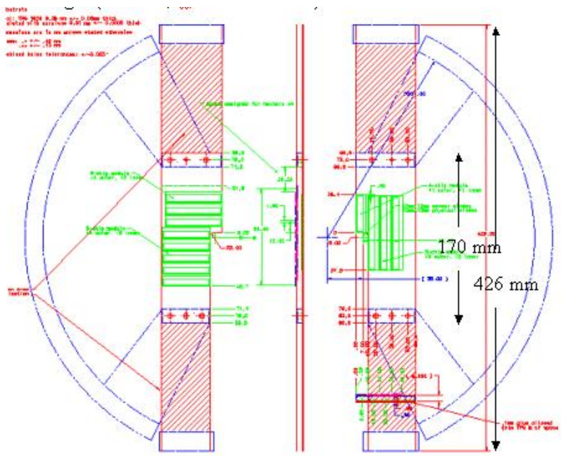

Figure 4.29: Layout of the TPG substrate

After the basic configuration has been established, a complete FEA model with multichip modules placed on both surfaces of a TPG substrate (fig. 4.30) was made. The temperature dependence of the thermal properties of the TPG was included in the model. A uniform heat load density of 0.5W/cm^2 was assumed to be generated from the readout chips. Displacement restraints were applied to those nodes representing the precision hole and slot (used for station assembly and thermal stress relief purposes) where only in-plane displacement was allowed. The thermal profile across the substrate and modules are shown in Figures 4.31 to 4.34. In addition, thermal stresses and displacements were checked and they appeared to be acceptable[21].

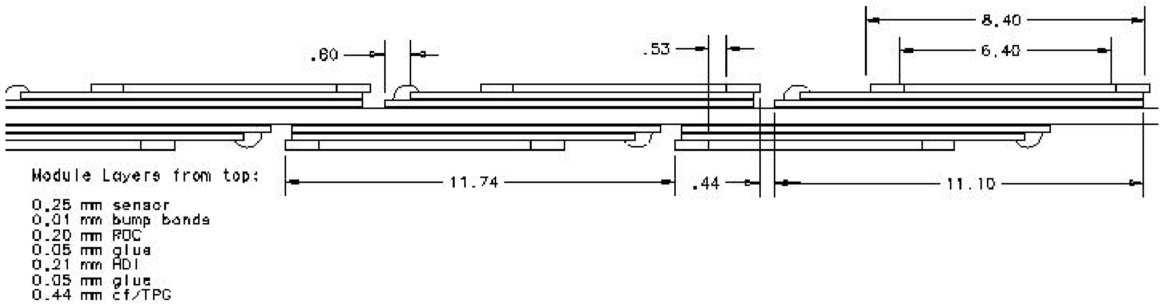

Figure 4.30: Layout of the multichip modules on the TPG substrates

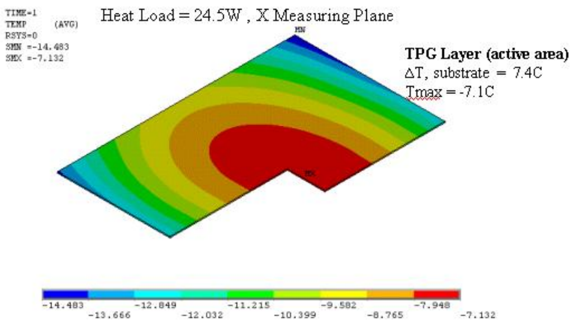

Figure 4.31: Thermal profile of TPG substrate within the active area in the x-measuring plane

We have recently changed our pixel module configuration so that the HDI will be placed underneath the pixel readout chips, directly on top of the TPG substrates. A preliminary FEA was done to compare the thermal performance of this design against the previous design which had the HDI placed on top of the sensor. The result showed little difference in the thermal uniformity across the substrates but the temperature of the readout chips would be up to 5°C higher in the new design. This can be compensated by keeping the ends of the TPG substrates at a slightly lower temperature.

Referring to Figure 4.35, there are three possible configurations of attaching the substrate to the heat sink. Configuration A, which is similar to the Atlas SCT Barrel module design that uses spring clips to keep the TPG in contact with the cooling block and allow a thermal in-plane sliding, is foreseen inappropriate in our complicated 3-D environment.

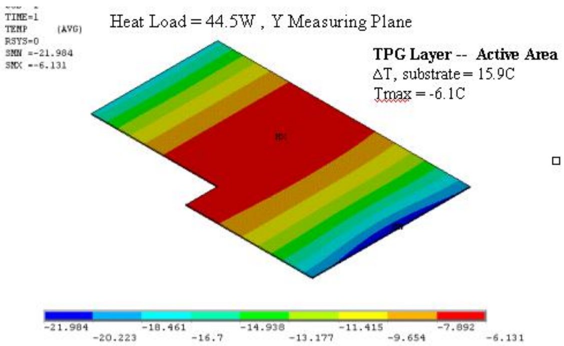

Figure 4.32: Thermal profile of TPG substrate within the active area in the y-measuring plane

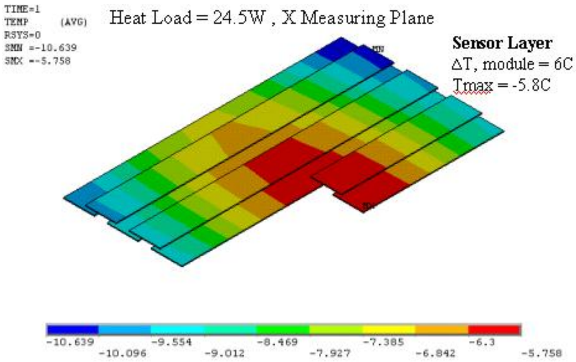

Figure 4.33: Thermal profile of sensors in the x-measuring plane

Configurations B and C, which use PGS as a flexible coupling, were studied carefully. The only difference between B and C is the location of the flexible joint. PGS in configuration B is directly attached to the heat sink beyond the extended TPG substrate, while the PGS in configuration C is placed immediately beyond the core of the TPG substrate and another piece of TPG is used to attach to the heat sink. In this study, the basic joint structure is a PGS-TPG-PGS sandwich with an overlap in each joint of 12 mm. Both TPG and PGS were modeled with temperature-dependent thermal properties.

It was found that configuration B always needed larger dimensions than Configuration C to achieve this. However, the extra joint employed in the configuration C reduced this saving substantially because more materials to make up a joint were used. In addition, as configuration B has a simpler design and the loop of the PGS flexible coupling of configuration C is likely to have some interference with the cable, material saving is thus not the driving factor for selection and hence configuration B has been chosen for further studies and prototyping.

The future and final step in the FEA study will be to check the performance of the

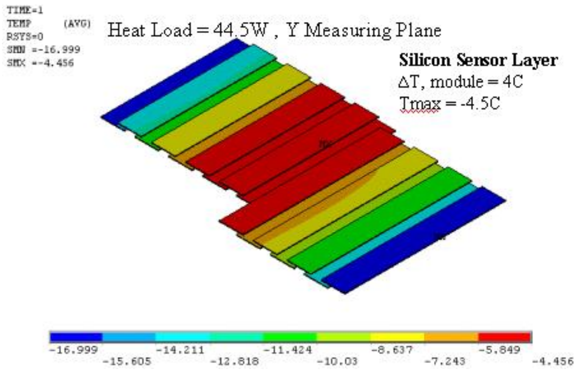

Figure 4.34: Thermal profile of sensors in the x-measuring plane

TPG substrate with additional heaters which will be used in order to achieve the needed temperature stability. A number of power outage or spike scenarios will be assumed. In addition, thermal radiation effects, even though expected to be very small, will be included in the simulation.

The study of material properties of TPG and PGS include the measurement of the coefficient of thermal expansion, thermal conductivity, and elastic modulus as functions of temperature down to liquid nitrogen temperatures. Possible effects due to magnetic field and radiation have also been investigated. Fig. 4.36 shows the measured thermal conductivity of TPG and PGS as a function of temperature. One can see the strong temperature dependence for TPG. In contrast, the thermal conductivity of PGS is rather stable within the range of temperatures that are of interest to us.

TPG is intrinsically friable and delaminates rather easily. Moreover, since sensitive pixel readout chips will be placed on top of it, we are concerned about carbon dust that it may generate. The surface needs encapsulation and we have tried several encapsulation techniques. Due to the material budget constraints, however, choices for the encapsulation material is limited. These include a thin coat ($\sim 10\mu$m) of parylene, epoxy, and carbon fiber. We have tried to encapsulate by using one ply of carbon fiber about 30 micron thick. Before the encapsulation, a pattern of perforated holes are drilled on the TPG substrate. By doing so, hundreds of resin bonds interconnecting the top and bottom layers are formed. Since getting fracture across the wider cross section of area is unlikely to happen, carbon fiber is only added along the long side to stiffen the much vulnerable smaller cross section area as needed. The carbon fiber lamination strengthens the TPG significantly and addresses the concerns with routine handling of the substrate.

Other tests include the flatness measurement of TPG and outgassing studies before and after encapsulation. The outcome of these tests show that TPG with the carbon fiber sheets laminated to the surfaces are robust enough for handling and modules placement. We are currently working out quality assurance issues.

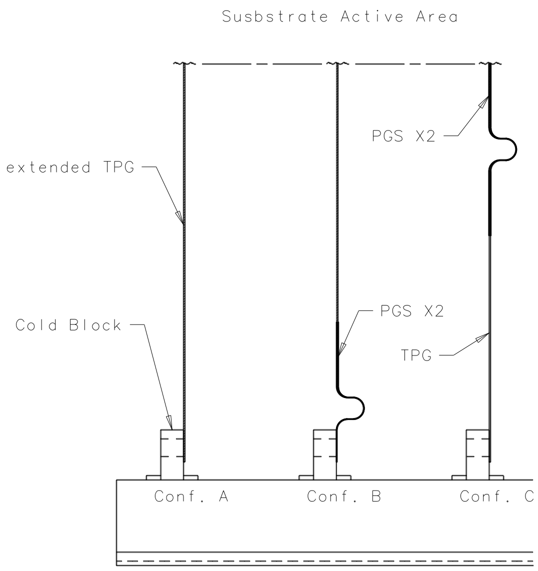

Figure 4.35: Joint Configuration in the extended area

4.4.7.4 Feed-through Board

The feed-through board (FTB) is primarily dedicated to bring signals from and the power to the pixel modules. The huge number of lines and tight space available do not allow the use of commercially available feed-throughs. The solution to this problem is to use a custom made multilayer printed circuit board as the feed-through core element.

The preliminary specification of the FTB has been completed [23]. Based on this, a full layout has been done, and suitable connectors have been chosen. The board is very complicated and in order to realize this, there are quite a few issues which need to be addressed:

- The potential pitfalls of making such large size thick multilayer board. Each board measures 27.5" by 17". The current layer count is 36 because of the numerous numbers of signal and power traces that will be needed. On the other hand, the board cannot be too thick because of geometrical constraint due to the magnet and to the depth of the connector that can be placed on the board. A potential problem is board warping

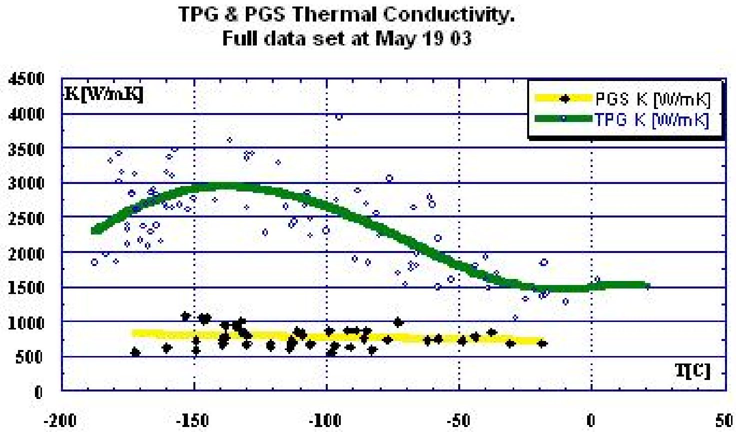

Figure 4.36: Thermal conductivity of TPG and PGS as a function of temperature

during the assembly. Another problem is impedance matching and the fine trace width and spacing. There are only a few vendors for such complicated boards.

- The possibility of making a vacuum tight board. With so many layers and different connectors and slots on the board, it will be challenging to make such a board that can hold the required vacuum level.
- Robustness of the board and the fine traces during assembly and operation and effect of irradiation.
- Reliability of vacuum tight joint in between boards and aluminum plates.

For the first three questions, a full scale board prototype has been designed. Fig. 4.37 shows a schematic of the full-sized feed-through board prototype. We have contacted a few vendors on fabrication issues such as material selection, thickness, insertion of connectors, and the possibility of warping. A couple of these prototype feed-through boards have been ordered and will be available for testing in 2 months' time. We are also looking into ways of simplifying this board. Small test boards will be built to test new design concepts and layout ideas. These test boards will be made using two materials of different dielectric constants. We will perform tests to check the outgassing and dielectric properties before and after irradiation. To answer the last question, a mechanical FTB prototype was built. Multilayer boards were substituted by regular fiberglass plates of the correct thickness. Then they were joining together by gluing on the aluminum plates. The assembly was checked and no leak found. A load was next applied to the ends of the board. Even after the FTB was bent (Fig. 4.38) no leak through the joints was detected.

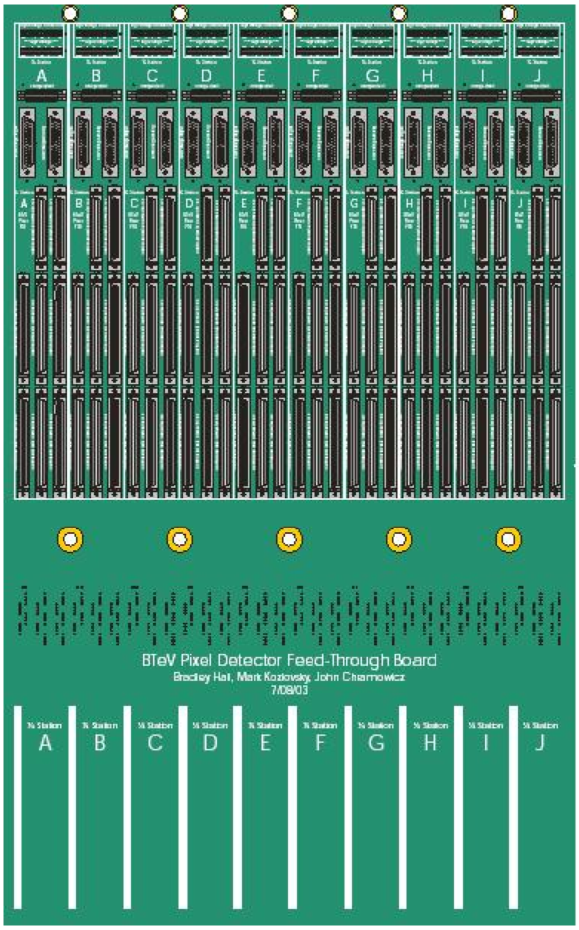

Figure 4.37: Front view of the Feed-through Board now being layout and reviewed.

4.4.7.5 Outgassing test and 5% model test

A model comprised of about 5% of the BTeV Pixel Detector (in terms of surface area) was built for the purpose of measuring its gas load due to outgassing and to understand how the gas load affected the ultimate vacuum pressure of the chamber. The model consisted of six substrates with dummy modules. A carbon-fiber shell supported the substrates. Kapton strips simulated the electrical flex cables. An aluminum plate served as a cable strain relief plate and a heat sink. The test was set up so that the model and the cable strain relief plate/heat sink was each cooled independently. Fig. 4.39 and Fig. 4.40 show the model.

When the model and heat sink were at room temperature, the vacuum pressure was 3.4×10^{-7} torr and the gas load was 5.2×10^{-4} torr-L/sec. Cooling the model and heat sink

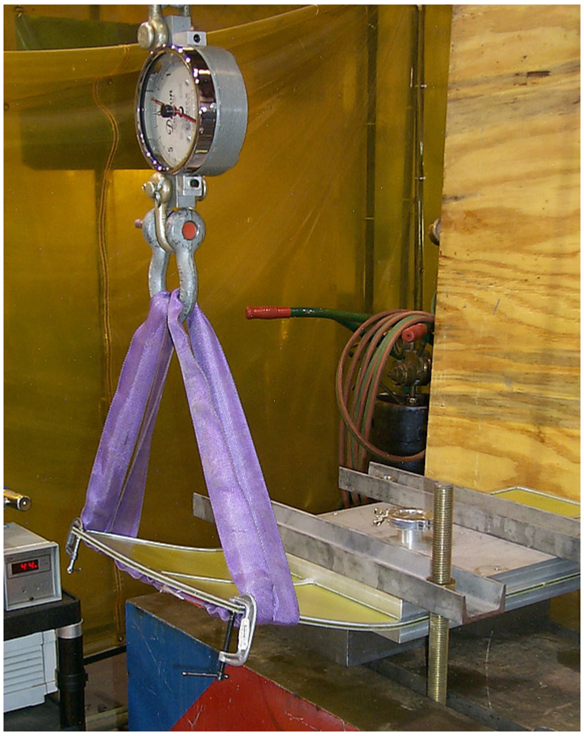

Figure 4.38: Prototype feed-through board being tested for vacuum properties.

to $-10°$C cut the gas load and the vacuum pressure in half. By cooling the heat sink to $-160°$C, the vacuum pressure was brought down to 1.0×10^{-8} torr. Analyzing the residual gas analyzer (RGA) readings at each temperature, it was found that water vapor was the main load and that cooling the heat sink to $-160°$C resulted in the heat sink acting as a cryo-panel that pumped water at a rate of 19,000 L/sec [22]. Thus, using the cryo-panel in conjunction with other pumps such as turbopumps or cryogenic pumps can result in the pixel vacuum vessels ultimate pressure to be $< 10^{-8}$ torr, which is the minimum acceptable pressure in the beam regions.

Several tests need to be run to fully understand the ramifications of having a cryo-panel in the vacuum vessel. To address question of the cables passing a very cold heat sink, the effects of cold temperature on the electronic flex cables have been tested. A prototype signal cable and a power cable were completely immersed in liquid nitrogen. The ends of these cables were then repeatedly flexed for a distance of about 3 cm while having current run through them (10 mA for signal cable, 1.5 A for power cable). The voltage of each cable was recorded. The flex test ran for 100,000 flex cycles. The cables continued to show consistent voltages, indicating that the cold temperature did not have an effect on the structural integrity or performance of the cables. Future testing will include measuring the position and temperature of the support structure and the substrates when the cryo-panel is cooled and understanding the long-term effects of the cryo-panel, such as ice buildup and structural effects. We will also do a complete FEA model of the temperature profile of each of the main elements inside the vacuum vessel.

One of the implications of the results from the 5% model outgassing test is that by using cryo-panels inside the detector vacuum vessel, we no longer need any separation between detector and beam volumes. This means that we will not need big rectangular bellows that appeared in earlier designs. Furthermore, we can choose to split the two halves of the pixel detector either vertically or horizontally. The test results gave us a few new ideas on how we can improve the reliability of the BTeV pixel detector. A major concern of our baseline design is that we will have numerous joints, connections and manifolds filled with coolant inside a high vacuum vessel. Any leak in such a system will have significant impact on the operation of the Tevatron. Based on the results of the outgassing test and the presence of cryopanels inside the vacuum vessel, as discussed before, our substrate and cooling system has been changed to a joint-free design based on liquid nitrogen lines and the high thermally conductive TPG substrate.

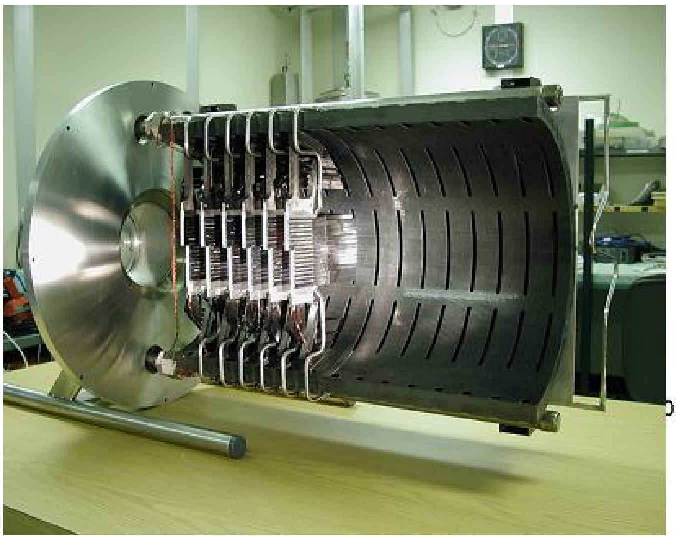

Figure 4.39: 5% model of the BTeV pixel detector, with dummy silicon modules assembled on six Al substrates.

4.4.7.6 Positioning system

The positioning system will provide precise independent motions of half-detectors in both x and y direction (where z is beam direction). The pixel detector has to be moved out of the beam during beam refill and returned precisely to its original position once stable beam is established. Because of possible variation of beam position from store to store, we have to be able to adjust the detector position to correct for long term beam position drift. While the nominal beam hole is fixed at 12 mm, we may want to change the beam hole for various

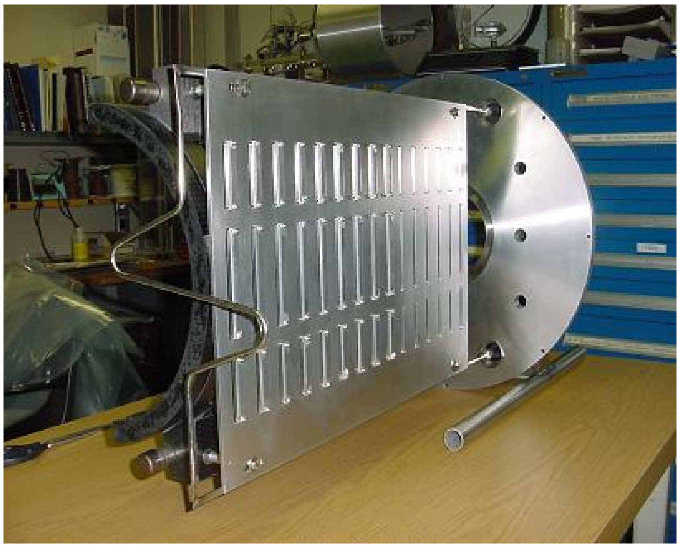

Figure 4.40: 5% model of the BTeV pixel detector, with cable strain relief/heat sink and its cooling channel.

reasons. The design of the positioning system is driven by these requirements. We would like to achieve a precision of 2 μm or better for the movement and the position of the whole system should be repeatable to better than 50 μm.

The positioning system consists of two major components:

- actuators: the elements that move the half-detectors; and
- sensors: these define the actual position of the half-detectors and are used to direct the movement of the actuators.

Actuator Progress has been made in design of the pixel positioning system. We have built a prototype air-actuated motion device (Fig. 4.41) This prototype contains a carbon steel gearbox, feed screw and slides, which is of a concern when operated in a magnetic field, Results of testing this prototype are summarized as follows:

- Incremental step motion of under 1 micron level precision is achievable with the chosen design;
- The actuator is robust and can withstand the design load without excessive deformation;
- The pneumatic indexer is not sufficiently reliable. It broke after the actuator had made about 100 motion cycles;

- Independent checking of the harmonic gearbox used in the actuator showed that when operating in a magnetic field, the power required to rotate the gearbox is about 6 times higher than the power required when there was no magnetic field. Extensive wear of the gearbox parts was noticed after about 20 hours of operation inside the test magnet;
- No significant effect of the magnetic field on feed screw mechanism was found.

These results lead to the following design changes:

a. The pneumatic indexer will be replaced by a conventional electromotor installed outside the magnet, at an easily accessible location. A long flexible shaft will be used to transmit motor rotation to the actuator;

b. A gearbox built of non-magnetic components will be used in the actuator;

c. Non magnetic slides will be used.

Special attention was paid to design of attachment of the detector to actuators. The most important requirement to the attachment design is that there should be no backlash. In the near future, we are going to build a prototype of these attachments and test them mechanically and thermally.

Position Sensors These sensors are used to measure the position of the pixel half-detectors after each movement during the beam refill. The sensors have to be operated inside a magnetic field and in vacuum. The required precision is about 1 μm or better and the sensors have to be very robust and reliable. For these reasons, capacitive sensors have been chosen as the primary candidates. Tests on capacitive sensors are currently under way.

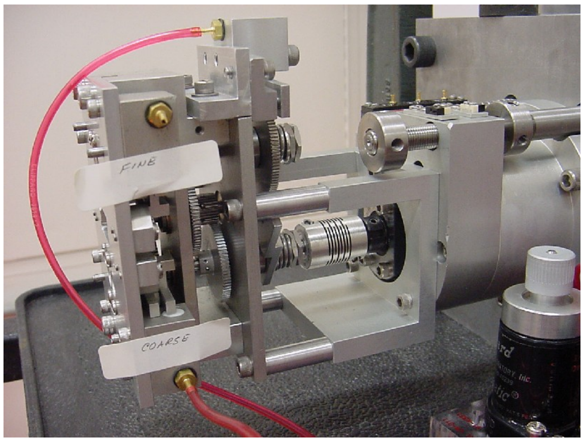

Figure 4.41: Sideview of the prototype actuator.

4.5 Technical Description

The technical design of the BTeV pixel detector is based on the results and experience that we have acquired during the last few years of R&D as summarised in the last section. The design for the mechanical support, vacuum system, and RF shielding have not been finalized, but will follow closely the results obtained and the anticipated results from testing of our prototypes.

4.5.1 Pixel Detector Specifications

The baseline pixel vertex detector consists of a regular array of 30 "stations" of "planar" silicon pixel detectors distributed along the interaction region sitting inside the 1.5T SM3 dipole magnet. Each station contains one plane with the narrow pixel dimension vertical, and one with the narrow dimension horizontal. The stations are split, having a left half and a right half. Each half-station contains one (approximately) 5 cm $\times$ 10 cm precision vertical-position-measuring half-plane, and a smaller, (approximately) 3.8 cm $\times$ 7.3 cm horizontal-position-measuring half-plane. The left half-stations are positioned at regular intervals along the beam, and the right halves are similarly positioned, but midway between the left-half stations. This allows for possible overlap of half-planes with a variable-sized, small hole left for the beams to pass through. Table 4.3 summarizes the properties of the pixel detector.

The vertex detector contains $\sim 30 \times 10^6$ pixels, each 50 μm $\times$ 400 μm, and covers a total active area of $\sim 0.5\text{m}^2$. Each sensor pixel is read out by a dedicated electronics cell. The sensor pixel and the readout cell are connected by a "bump bond." The basic building block of the detector is a pixel module which is a hybrid assembly consisting of a sensor, a number of readout chips, and a flexible printed circuit (a high-density interconnect, HDI) which carries I/O signals and power. The sensors are variously sized to accept variable numbers of readout chips to make the required half-plane shape. Each readout chip is "flip-chip" mated to 22 columns of 128 rows of pixels on the sensors, corresponding to 2,816 active channels per readout chip. Each readout chip covers an active area approximately 0.64 cm $\times$ 0.92 cm. To avoid any dead space between adjoining read out chips, the pixels on the sensors corresponding to the edge of the readout chip (first and last column) are extended to 600 μm. These pixel modules are supported by a movable carbon substrate that allows the pixel sensors to be positioned a safe distance away from the beam-line until stable conditions have been established in the Tevatron, at which point they are moved as close to the beam-line as radiation damage considerations will allow. This substrate also provides cooling through conduction for the readout electronics. To minimize the material, the pixel half-detectors sit in vacuum, separated from the beams by only a set of rf shielding wires or strips.

4.5.2 Front-end chip

The pixel electronics must not only satisfy the efficiency requirement as outlined in the Requirements section, and provide charge sharing information to allow the position resolution

Table 4.3: Pixel Vertex Detector Properties

Property	Value
Pixel size	rectangular: 50 μm $\times$ 400 μm
Outer Plane Dimensions	10 cm $\times$ 10 cm
Central Square Hole (adjustable)	nominal setting: 12 mm $\times$12 mm
Total Planes	60 (each splits into left and right half)
Total Stations	30 (split into left and right half-stations)
Pixel Orientations (per station)	one with narrow pixel dimension vertical & the other with narrow dimension horizontal
Separation of Half-stations	4.25 cm
Staggering of the two half-detectors	offset by half of the station separation
Sensor Thickness	250 μm
Readout Chip Thickness	200 μm
Total Station Radiation Length (incl. rf shielding)	3.0%
Total Pixels	2.3×10^7
Total Active Area	$\approx$0.5m^2
Readout	analog (3 bits)
Trigger	Signals are used in Level I trigger.
Rate Requirements	Time between beam crossings is 396 ns 132 ns BCO also fully supported
Noise Requirement	desired: $< 10^{-6}$ per channel/crossing required: $< 10^{-5}$ per channel/crossing
Resolution	better than 9μm
Radiation Tolerance	$> 6 \times 10^{14}$ particles/cm^2
Power per Pixel	$\sim$60 μWatt
Operating Temperature	$\sim$-5 °C

requirement to be met, but also must be robust and easy to test, and must facilitate testing and monitoring of the pixel sensors. The pixel readout chip has to satisfy the following requirements:

- **Dynamic Range**: The dynamic range of the front-end amplifier should cover up to the mean charge as deposited on the sensor by a normally incident minimum ionizing particle.

- **Noise of Front-end**: The design of the system shall be such that before irradiation, the front-end electronics noise should be less than 200 equivalent electrons and this should not increase significantly after irradiation to a fluence equivalent to 10 years of BTeV operation.

- **Leakage Current Compensation**: as silicon sensors get damaged by radiation, their leakage current will increase. Each pixel must compensate for this increase in leakage current up to 100nA per cell.

- **Threshold and Dispersion**: Each pixel input shall be compared to a settable threshold. This analog threshold of each readout-chip shall be settable via digital control. Typical settings shall be from 2000 to 6000 equivalent electrons at the input. Threshold dispersion must be low enough that the chip can be operated stably and efficiently at 2500 electrons threshold setting. With a 250μm thick sensor which roughly gives a signal size of 20K electrons, this gives a ratio of signal/threshold of 8. Typically, the threshold dispersion should be comparable and not significantly larger than the noise of the front-end during its entire operational lifetime. The threshold overdrive should also be low enough so that signal just above the threshold will be correctly time-stamped.

- **Analog Information Availability**: Analog information from each pixel cell shall be available. This helps in improving the spatial resolution, but more importantly, it helps in monitoring the performance of the sensors. After careful study including beam tests and simulation, we conclude that a 3-bit ADC will be adequate both for resolution and monitoring.

- **Masking: Kill and Inject**: Each pixel channel must be testable by charge injection to the front-end amplifier. By digital control, it shall be possible to turn off any pixel element from the readout chain.

- **Cross-talk**: A tolerable cross-talk is such that at no time shall it exceed the threshold. We require the cross-talk to be less than 5%.

- **Power Consumption**: The total power consumption of the readout chip must be no more than 0.5W/cm^2. This roughly corresponds to about 60 μW per pixel.

- **Time Stamp**: Each pixel hit must be given a correct timestamp which identifies the beam crossing number.

The pixel size will be 50 μm by 400 μm. Each FPIX2 pixel readout chip will read out an array of 22 columns by 128 rows of pixels. Fig. 4.42 shows the FPIX2 layout. The chip consists of five functional sections: the pixel array, the end-of-column logic the command interface, the programmable registers and digital to analog converters(DAC), and the data output interface. The pads located on the top edge of the chip in figure 4.42 are for debugging purposes only and will be removed for the production version. Connections to the chip are made by using a single row of 70 wire-bond pads located at the bottom edge of the chip.

The pixel unit cells, each of which contains an amplifier and a 3-bit flash ADC, the end-of-column logic associated with each column of pixels, and core logic, which controls the flow of data from the core to the data output interface are together referred to as “the core”. The rest of the chip is referred to as the “periphery”. The programming interface accepts commands and data from a serial input bus, and, in response to commands, provides data on a serial output bus. The programmable registers are used to hold input values for the DACs that provide currents and voltages required by the core, such as the discrimination threshold and the threshold levels for each of the FADC bits. The data output interface accepts data from the core, serializes the data, and transmits it off chip using a point-to-point protocol operating at 140 Mbps. All I/O (except the test signal inject) is differential and uses Low Voltage Differential Signaling (LVDS). Since the average number of hits per crossing is very non-uniform across the whole half station, the required output bandwidth also varies greatly. To account for this fact, each FPIX2 chip can be programmed to use 1, 2, 4, or 6 serial output links. The only supply voltages required are 2.5V and ground; all other bias voltages, currents, and threshold settings are generated internally by the programmable DACs.

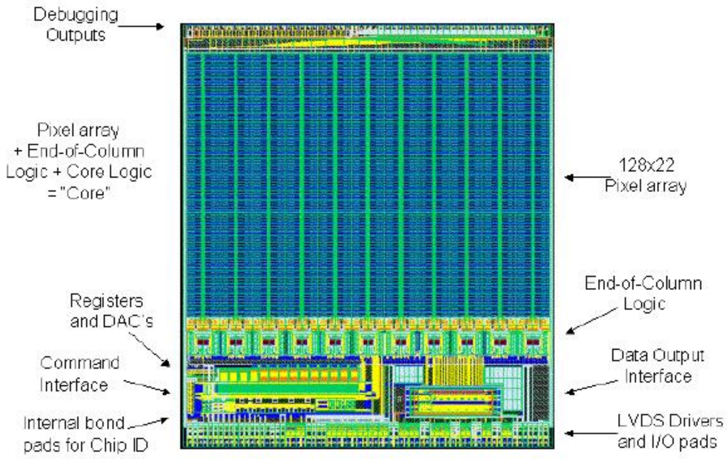

Figure 4.42: FPIX2 layout.

4.5.3 Sensor

The BTeV pixel cell size is 50 μm by 400 μm, where the small dimension is dictated by the needed spatial resolution. The technology chosen is $n^+/n/p^+$. Because of the accumulation layer induced by the oxide charge, the individual n^+ cells would be shorted together unless some electrical insulation is provided. Various isolation techniques have been developed for silicon pixel sensors. We have explored two techniques: p-stop and moderated p-spray. Both techniques seem to give good results before and after irradiation based on electrical characetrization results. The final choice depends on the results of the charge collection and efficiency studies of both types of detectors before and after irradiation. Recent results from CMS have shown that the p-stop sensors had significant charge losses around the corners of the p-stop region, particularly after heavy irradiation [24]. On the other hand, the charge loss observed in the p-spray sensors were a lot less and this was found to be around the bias dot region [24],[25]. We plan to confirm these results in a test beam starting Spring 2004.

Another major issue is on testing the sensors before bump bonding. We have discussed in previous section that wafer probing of p-stop sensors do not give the correct breakdown voltage. This is due to the fact that not all the pixels are biased properly. In the p-spray technique, a bias grid structure can be implemented which allows the testing of the sensors under full bias before assembly. This structure is very important for quality control during mass production. Moreover, in case of missing bonds, this bias grid acts as a safety feature during operation, maintaining the unconnected n^+ electrode potentials close to ground. The bias grid connects every pixel via an equally sized punch-through gap, preventing excessive potential on any individual pixel. For this reason and because of the charge loss problem observed on the p-stop sensors, the p-spray sensors will be used as our baseline technology for the final production.

The sensors will be fabricated on 4" wafers of n-type silicon. Each wafer will consist of sensor modules of different sizes. We will discuss with the vendors on the optimal layout to maximize the yield. In addition, there will be a few single chip sensors, test structures, gate-controlled diodes, and MOS capacitors for quality control purposes. All wafers will be oxygenated.

The following geometrical tolerances need to be met:

- Misalignment of p^+ implant, n^+ implant and metal layers $\pm 2\mu$m,
- Mask alignment precision between front and back side $\pm 5\mu$m,
- thickness 250 μm,
- uniformity of wafer thickness (wafer to wafer) $\pm 10\mu$m.

The following electrical specifications need to be met:

- Operating voltage V_{op} at 20°C: 200V or 1.3x full depletion voltage, whichever is greater;
- Leakage current at 20° C $\leq$50 nA/cm^2 at V_{op};
- Current slope measured at 20°C: I(V_{op})/I(Depletion voltage) $\leq$ 2;
- Bulk resistivity 1.0-2.5 KΩ-cm;
- Breakdown voltage $\geq$ 300 V or 1.5 V_{op} whichever is greater
- Detector current shall increase by no more than 25% after 12 hours of operation in dry air at V_{op}

4.5.4 Bump Bonding

Both indium and solder bumps are viable technologies to meet our requirements. Over the years, we have qualified three vendors. These are AIT (Hong Kong), MCNC (North Carolina), and VTT (Finland). Solder bumps are used by all three companies while only AIT can provide indium bumping. Besides these three companies, we have kept in contact with the LHC experiments about their plans and qualified vendors. The choice of the technolgy and vendor will depend on the availability and capacity of the vendors as well as QA plans and issues. Solder bumps have a few advantages over indium:

- Mechanically more robust
- Process can be fully automated and handle large volume
- Mainstream in industry and cheaper for large production
- More vendors available

For these reasons, in our base estimate, we have used solder bumps as the baseline technology with indium as a viable alternative.

4.5.5 Modules

The main components of the pixel module are:

- Pixel readout chips
- Silicon sensor bumped bonded to the readout chips
- High density interconect HDI flexcircuit with surface mount components
- Two Pixel interconnect flex cables (PIFC): one for the power and the other for data and control signals. These will be connected to the HDI with the connection technology still beting studied. Options include small, fine pitch connectors, wire bonding, solder pads, and the use of a fine-pitch z-axis conductive film.

The pixel multichip module is built as a three-layer stack. The bottom layer is the high-density interconnects (HDI) circuit, to which all FPIX chips are wire-bonded. The bottom of the FPIX chip is mounted on top of the HDI, while the top of the FPIX chip is flip-chip bump bonded to a silicon pixel sensor. The bottom of the FPIX chip is in electrical contact to the ground plane on the top metal layer of the HDI. The HDI also provides low voltage (2.5V) to the FPIX chip and high voltage (up to 1000V) to bias the pixel sensor.

The modules come in four different sizes: 1x4 (with one long piece of silicon sensor bump-bonded to 4 readout chips arranged in a linear array), 1x5, 1x6 and 1x8. The HDIs will accordingly come in 5 different sizes, with the 1x4s having two versions, one being the mirror image of the other one. The PIFC's will come in 4 different sizes to match the corresponding HDIs.

The pixel detector design is severely bounded by several constraints which impacts on the choices of high density inerconnect (HDI) cables. These constraints include readout speed, material budget, outgassing, distribution of the high voltage for detector bias, radiation environment, reliability, and cost.

The circuit density of the HDI is highly associated with the read out speed of the pixel chip. All data generated inside the pixel chip has to be readout for the lowest level trigger decision. In order to accommodate reasonable read out throughput, several readout buses will have to be routed for the data serializers on the pixel readout chips. Based on the space available for routing, one can see that very high density circuits need to be used. Several factors impact the amount of data that each readout chip needs to transfer: readout array size, distance from the beam, and the data format. Further details of the data structure and throughput are given in the Chapter on Electronics.

Since the pixel detector will be placed inside a strong magnetic field , the flex circuit and the adhesives cannot be ferromagnetic. The pixel detector will also be placed inside a high vacuum environment, so the multichip module components must have a low outgassing rate. The severe radiation environment and planned operating temperature (-5 to -10°C) also impose severe constraints on the pixel multichip module packaging design.

Another important constraint of the HDI is the ability to distribute the high voltage for detector bias. The pixel detector receives different radiation levels depending on the distance from the beam and therefore, it has to be biased with different high voltages to obtain the optimal performance and account for different detector degradation with radiation. The circuit interconnect will have to reliably deliver the high voltage to different points of the pixel plane and avoid high voltage breakdowns that may short circuit the high voltage traces with signal traces or power and ground.

The HDI will be made out of low-mass flex-circuit interconnect. This approach will effectively meet all the constraints outlined. The baseline design for the interconnect is to glue the HDI directly to the TPG substrate, with the pixel modules placed on top of it. In this way, a solid ground plane can be provided by the HDI to the back side of the readout chips. The HDI will consist of the following four layers of flex-circuit:

- one layer for the ground plane.
- two layers for signal interconnects,
- one more layer for power and other signals.

These layers are quite thin and can be kept within 18 μm of copper thickness or less. The PIFC consists of a power flex and a data flex. Each of these flex cables has two layers and uses standard flex circuit design rules. We are also investigating the use of Aluminum for the power flex cable to reduce mass.

4.5.6 Readout and control

The success of the experiment relies critically on the quality of the data provided by the pixel system to the Level 1 trigger. The trigger imposes the following readout requirements on the readout of pixel system:

- **Data Sparcification**: The data output from the pixel detector shall be only of those cells that are above the settable threshold.
- **Pixel output data content**: The pixel hit data must include the beam crossing number, chip identification number, and the pixel hits for that beam crossing. The pixel data must have row and column numbers, and pulse height information for each hit.
- **Minimum Data Rate Capability**: The data output from each pixel readout chip shall be data driven, and capable of continuous readout at a minimum rate of 4 hit pixels per beam-crossing time.
- **Graceful Degradiation above rate capability**: The data output from the pixel system may be lost for rates well above the minimum rate sepcified above. However, the loss should be in a fashion that when the burst in data rate is passed, the system shall return to normal operation without external intervention.
- **Readout Abort**: The system must have a means of recognizing and aborting the readout of any chip that has an unusually high volume of data output (e.g. due to oscillation).

The readout architecture is a direct consequence of the BTeV detector layout. The BTeV pixel detector covers the forward direction, with an angular acceptance of 10-300 mrad, with respect to both colliding beams. Hence, the volume outside this angular range is outside the active area and can be used to house heavy readout and control cables without interfering with the experiment. The architecture takes advantage of this consideration.

The Data Combiner Board (DCB) located approximately 10 meters away from the detector remotely controls the pixel modules. All the controls, clocks and data are transmitted between the pixel module and the DCB by differential signals employing the Low-Voltage Differential Signaling (LVDS) standard. Common clocks and control signals are sent to each module and then bussed to each readout IC. All data signals are point to point connected to the DCB. This readout technique requires the design of just one rad-hard chip: the pixel readout chip. The point-to-point data links minimize the risk of an entire module failure due to a single chip failure and eliminate the need for a chip ID to be embedded in the data stream. Simulations have shown that this readout scheme results in readout efficiencies that are sufficient for the BTeV experiment.

In order to maximize the data throughput, the FPGAs on the DCB latch the signals on both the rising and falling edges of the 70MHz clock. The 24-bit long hit data (5 column-number bits, 7 row-number bits, 3 pulse-height bits, 8 timestamp bits, and 1 word mark bit) are serialized onto 1, 2, 4, or 6 programmable serial links. The serializer-FPGA synchronization is established and maintained by sending a Sync/Status word when no data are to be sent and just before each time the Token-Pass signal is launched to the first pixel column. More details will be given in the Electronics Chapter.

4.5.7 Mechanical Support

4.5.7.1 Introduction

One of the main requirements of the mechanical support strcture for the BTeV pixel detector is to keep the amount of material to a minimum. Counter to the material budget requirement are the needs for reproducible, stable position-determining supports, to remove significant amounts of heat directly from the active sensor areas, to move the detectors back from the interaction region during injection and machine-study periods, and to reposition the detectors reliably and accurately for physics data-taking. The detector needs to be retractable to a distance of $\pm$ 2 cm from the beam while the collider is being filled. When stable beams are established, the detector will be moved back with good precision to its nominal position. Because the pixel information will be used in the Level 1 trigger, the pixel detector needs to be aligned fairly quickly and easily (using tracks from data obtained by a short interaction trigger run) to a precision which is necessary to obtain the required spatial resolution of 9μm or better for all tracks and remain stable during data-taking. Note that for the current RUN II, the typical store time is between 12-24 hours and the refill time is up to 4 hours. It is envisaged that when BTeV comes online, the store and refill time will be significantly reduced.

4.5.7.2 Requirements of the Mechanical support system

Since the pixel detector will be installed close to the Tevatron beam, it must meet the requirements of the Beams Division. The following criteria have to be met:

- **Beam Conditions at other IR**: The presence of the detector must not degrade the beam conditions at other IR's by parasitic RF coupling.
- **Tevatron Operation**: Static and dynamic pressure effects inside the vacuum vessel must be low enough so that it will not affect the operation of the Tevatron.
- **Vacuum Loss**: A detailed vacuum loss and failure mode analysis has to be performed to safeguard the operation of the Tevatron and avoid potential damage to the Pixel System.

To achieve the physics goals of BTeV, the mechanical support system of the pixel detector has to meet the following requirements:

- **Acceptance**: The Pixel detector mechanical support structure should have low mass within the geometrical acceptance (300x300 mrad^2) of the spectrometer so that the performance of the other systems in the spectrometer not be compromised;

- **Alignment**: The pixel system must be alignable during each of the the assembly stages by suitable inclusion of alignment marks;
- **Effect on the Spectrometer dipole magnet**: The whole detector will be placed inside the aperture of a dipole magnet with a field strength of 1.5 T; it should not have any effect on the local magnetic field strength;
- **Effect of the dipole magnet**: Between stores, the dipole magnet may be ramped down. After the refill, the magnet will be ramped up from 0 to 1.5T. All support and motion control structures for the pixel system should not be damaged or affected by this ramping or by tripping of the magnet. Furthermore, the alignment of the pixel stations must not be influenced by the magnetic field by more than 20 μm and must have a ramp to ramp stability better than 10 μm.
- **Operating Temperature**: The design must take into account that the operating temperature of the detector will be in the range between -10°C and -5°C. Thermal stress must be considered so that the mechanical stability of the system will not be affected.
- **Pressure**: The goal for the pressure inside the pixel vacuum box is 10^{-8} torr.

All alignment requirements are given in terms of the narrow pixel direction.

- **Initial Alignment on Half-Planes - Narrow Pixel Direction**: The individual sensor subassemblies shall be mounted on their half-plane support to an accuracy of 5 microns, and measured to an accuracy of 2 microns before the substrate is mounted on its frame.
- **Initial Alignment of Half-Planes on Frame**: The individual half planes must be mounted with a precision of 20 microns or better, and the positions known to 10 microns before the half-planes are inserted in the vacuum container.
- **Alignment of the Two Halves**: The two halves of the detector must be positioned with respect to each other with an accuracy better than 50μm in x and y, and 200μm in z (longitudinal direction).
- **Offset**: the left and right halves of the detector should be staggered in the longitudinal direction to allow for minimal dead space;
- **Retractability**: The detector has to be retracted to a distance of 2 cm away from the beam and after each refill, the detector has to be moved into position for data-taking. The reproducibility should be better than 50μm and the position sensors must be read out with a precision of 1-2 μm.
- **Centering the Assembly on the Beams**: The full assembly must be such that the full detector can be centered on the nominal location of the Tevatron beams.

- **Alignment Monitoring**: The System must include some means of alignment monitoring online to a precision of better than 50μm for each station;
- **Stability**: the system should be stable to within 2μm during each store for data-taking;
- **Direction of motion**: the two halves can be moved in x and y independently so that we can accommodate the beam if it is not positioned exactly as expected, and so that we can operate with a square beam hole which is either larger or smaller than the nominal value.

4.5.7.3 Substrate

The pixel modules will be placed on a supporting substrate made out of thermalized pyrolytic graphite (TPG). The thermal conductivity of TPG at room temperature is about 1700 W/mK in-plane with roughly a -0.4%/^{c}ircC change, reaching a maximum of about 3000 W/mK at -180°C. Its thickness is $380 \pm 15\mu$m. .

The TPG material, is however, intrinsically friable and easily delaminates in the out-of-plane direction. In addition, some trace of graphite dust exists and TPG therefore must be encapsulated. It will be encapsulated on each surface with a single ply of prepreg (carbon fiber with epoxy) $\sim 30\mu$m thick. Before the encapsulation, a matrix of perforated holes are planned to be laser-drilled on the substrate. During the lamination of the carbon fiber sheets to the TPG substrates, hundreds of epoxy bonds interconnecting the top and bottom layers of the CF are formed and hence the overall stiffness of the substrate is greatly improved.

Each substrate will have an extended region outside the active area to allow the placement of fiducials, brackets mounts (to the carbon support cyclinder), and temperature control and sensing elements. It is L-shaped and measures 170 mm x 65 mm at the widest region. Pixel modules will be placed on both sides of the TPG substrate to form a half-plane. To provide mechanical stability, an x-measuring half-plane and a y-measuring half-plane will be bolted together to form a half-station. Figure 4.43 shows in detail the pixel modules assembled on the substrate.

With FEA as the chief design tool, we have chosen a substrate based on 0.38 mm thick TPG with a simple, vertical 2-end cooling configuration. This will be adequate to remove the 60 W of heat that will be generated by the pixel modules. As shown in Fig. 4.44, the substrate is thus a long piece of TPG consisting of a core area, which houses the modules, and an extended area, which channels the heat to the heat sink that is kept at cryogenic temperature. In the extended area, a pair of precision hole-and-slot washers is glued. These washers, together with the precision pins extended from the Carbon Fiber Reinforced Plastic (CFRP) brackets, are to determine the alignment of the substrate to the CFRP cylinder. In addition, this hole-and-slot arrangement will facilitate the thermal displacement of the substrate with respect to the CFRP brackets without creating any additional unwanted thermal stresses and distortion. Temperature control and sensing elements will be placed here also to dynamically control and monitor the operating temperature of the modules in case different operating conditions and failure scenarios arise. A flexible thermal coupling made of

PGS is glued to both ends of the TPG core substrate. This is needed to provide mechanical decoupling of the precisely assembled and aligned substrates from the less accurately made (brazed) cold blocks (see section of Cooling). Extensive FEA and experimental tests are ongoing to optimize the length and width of each component of these thermal joints.

The X- and Y- measuring half-plane substrates are both made in this way. They are glued together with CFRP hollow spacers in between. This spacer is made hollow so that those HDI cables inside the substrate can be led through for outer connection. To allow non-functioning modules be replaced during production assembly and testing, removable glue like NEE001 is to be used.

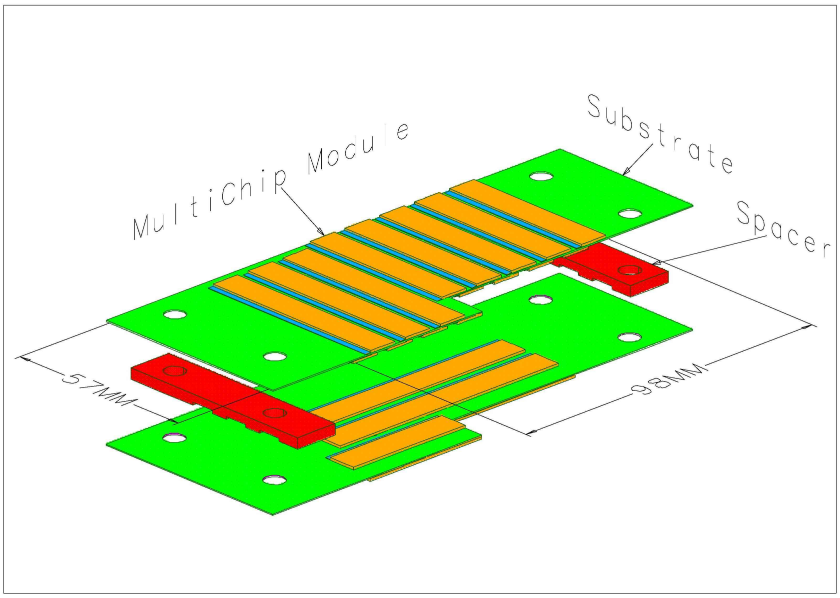

Figure 4.43: Schematic drawing of pixel modules assembled on the TPG substrates.

4.5.7.4 Assembly of modules

The modules are planned to be placed on the both sides of TPG alternatively to provide full coverage of the tracking area. To ensure a successful tracking, 0.53 mm of overlapping of the adjacent modules is allowed. The accuracy of the module placement with respect to the half-plane TPG substrate is within 5 μm in the X-Y pixel plane. Some precision fixture is needed to achieve this goal. As there are 120 half-plane substrates in the pixel detector, the ultimate goal of this fixture assembly is to produce all these substrates identically so that they can be placed in any CFRP bracket location.

The assembly process starts with gluing a couple of precision hole and slot washers on the half-plane substrate. A gluing fixture can be used so that all the half-plane substrates

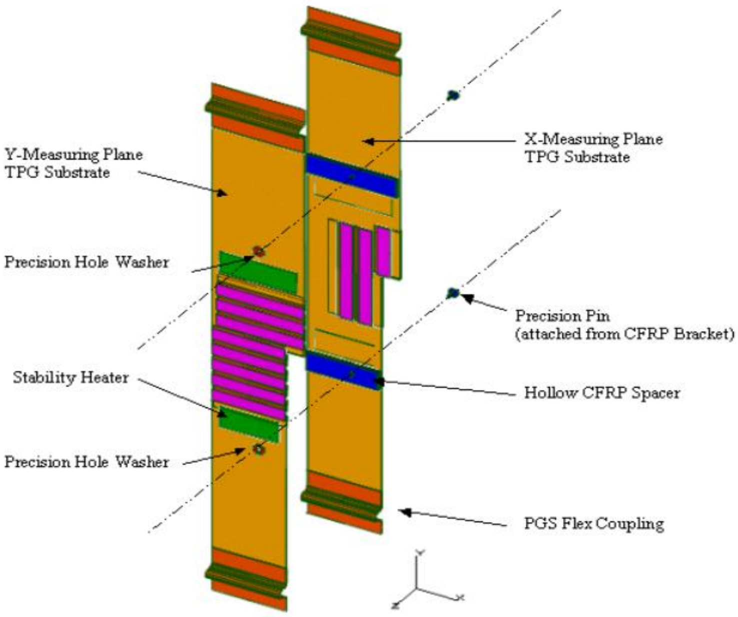

Figure 4.44: Schematic drawing of two TPG substrates to form a pixel half-station.

are made in the same way, and the accuracy of this gluing process is to be good to within 5 μm. This half-plane substrate is then placed on the module placement fixture assembly as shown in Figure 4.45. This module placement fixture assembly consists of several flat tooling plates and has a space in the middle to be allowed for the exchangeable plate. Two precision pins and two fiducials are made in the fixture. Since their locations are fixed, the reference to each other is thus locked and hence all the data with respect to either pin or fudicial reference system are transferable. The half-plane substrate will be engaged with the pins of the fixture assembly through the precision washers. After the application of a uniform layer of 0.075 μm-thick glue to the pixel module by means of another glue dispensing fixture, the module is held by a module holder which is mounted on 3 translational stages and has 1 angular moving capability. The module is then oriented and positioned with reference to the fiducial marks. Slight pressure is applied on the module to accomplish this gluing process. To take this slight loading pressure off the TPG substrate, there will be a supporting plate underneath the TPG. To ensure the placement of this set of modules matching the set of modules on the other side, a couple of targets that can be visible from either side will be placed on the substrates for checking the placement precision.

The same module placement fixture assembly will be used for fixing the CFRP bracket position so that the same precision pins reference system will be used for the whole assembly process. Template stations will be built on the same fixture to be used for CFRP bracket installation (see the following section).

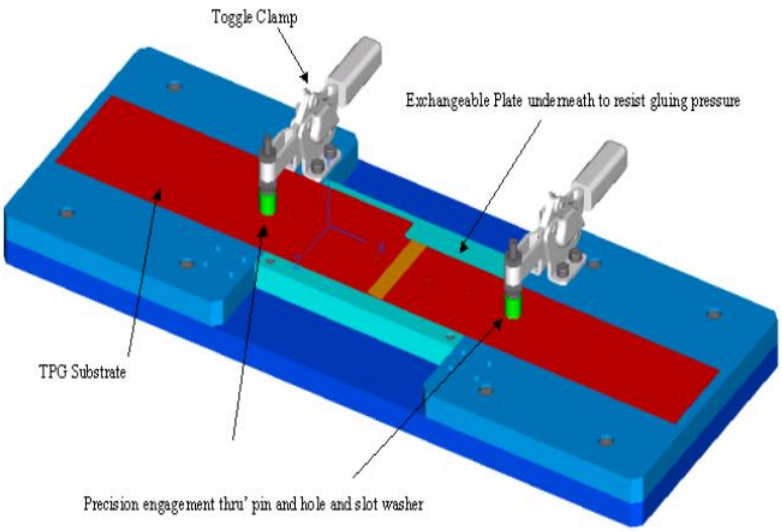

Figure 4.45: Schematic drawing showing the fixture used to assemble the pixel modules on the substrate.

4.5.7.5 Carbon support structure

The support structure for the pixel half-planes consists of inner and outer shells connected to each other by a number of ribs. Shells and ribs are made of carbon fiber laminates of 12 and 6 carbon fiber plies respectively. Figure 4.46 shows the design of the support structure for the pixel detector. Each pixel half-station will be attached by CFRP brackets to a C-shaped support structure. Fig. 4.47 is a technical drawing showing details of the carbon fiber support structure. Using the Template station, discussed in the previous section, the CFRP brackets will be positioned to 20 μm of their ideal locations within the support strcture and bonded in place. This assembly method ensures that all station mount locations be identical

Use of FBG sensors has been successfully tested for real-time and long-term monitoring of tracking detector structures. Monitoring directly provides the deformations due to either thermal or mechanical loads, and allows for working out the position displacements of the detector hold by the deformed structure. Resolution of 1μStrain for deformation measurements and 1mm for displacement measurements have been obtained. FBG sensors were used glued on metallic and CFRP structures, thus allowing their usage on already engineered structures. FBG sensors were also embedded in CFRP components thus providing the possibility of planning detector supporting structure with built-in structural monitoring system.

We will use two arrays of FBG sensors to monitor both the mechanical stability and the relative position of the carbon support structures. The first FBG array will be installed on the support structure to monitor its mechanical stability with respect to both thermal

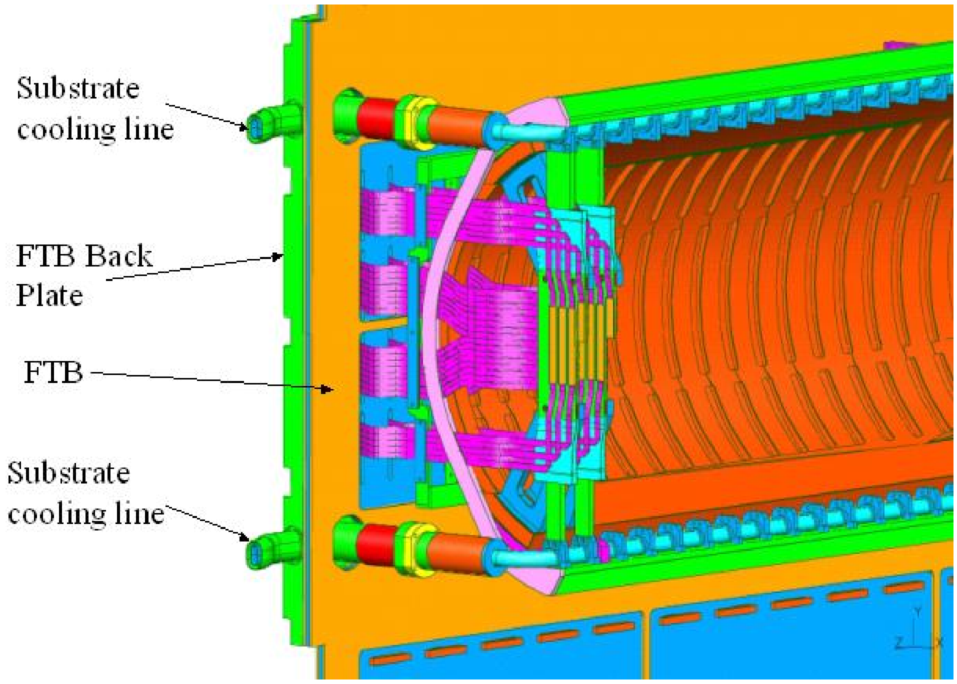

Figure 4.46: Side view of the support structure for the pixel detector. Also shown in the figure are a few pixel half-stations with flex cables coming off the pixel modules and feeding through slots on the feed-through board. The main cooling line and cooling blocks are also shown.

and mechanical loads. The second FBG array will be installed on the positioning system as an extra and independent check to precisely monitor the repositioning of the pixel detector after each movement during the beam refill. Figure 4.48 shows a schematic view of the FBG monotoring system proposed for the Pixel Cylinder Support structure and positioning system. A total of 48 FBG sensors fibers are installed on each half-cylinder structure: sensors are arranged in 12 strings of 4 sensors each; sensor strings are bounded in three bundles of 4 fibers each; each bundle is connected to a fiber optic ribbon cable to deliver to the optical switch. A total of 16 FBG sensors are installed on the positionining system of each half-cylinder structure: sensors are arranged in 4 strings of 4 sensors each; each sensor string is directly connected to an optical fiber to deliver the signal to the optical switch. The optical signal of the sensors is delivered to the Optical switch by use of fiber optic patch cords and vacuum connectors. The Optical Switch selectively address (time multiplexing) the signal of all the sensor strings to the Interrogation System, that both feeds coherent light to the FBG sensors and performs the analysis of the optical signals provided by the FBG sensors. The Optical Switch and the Interrogation System are both controlled by the Local Controller; the Local Controller is connected to remote systems for controll, data analysis and data storage.

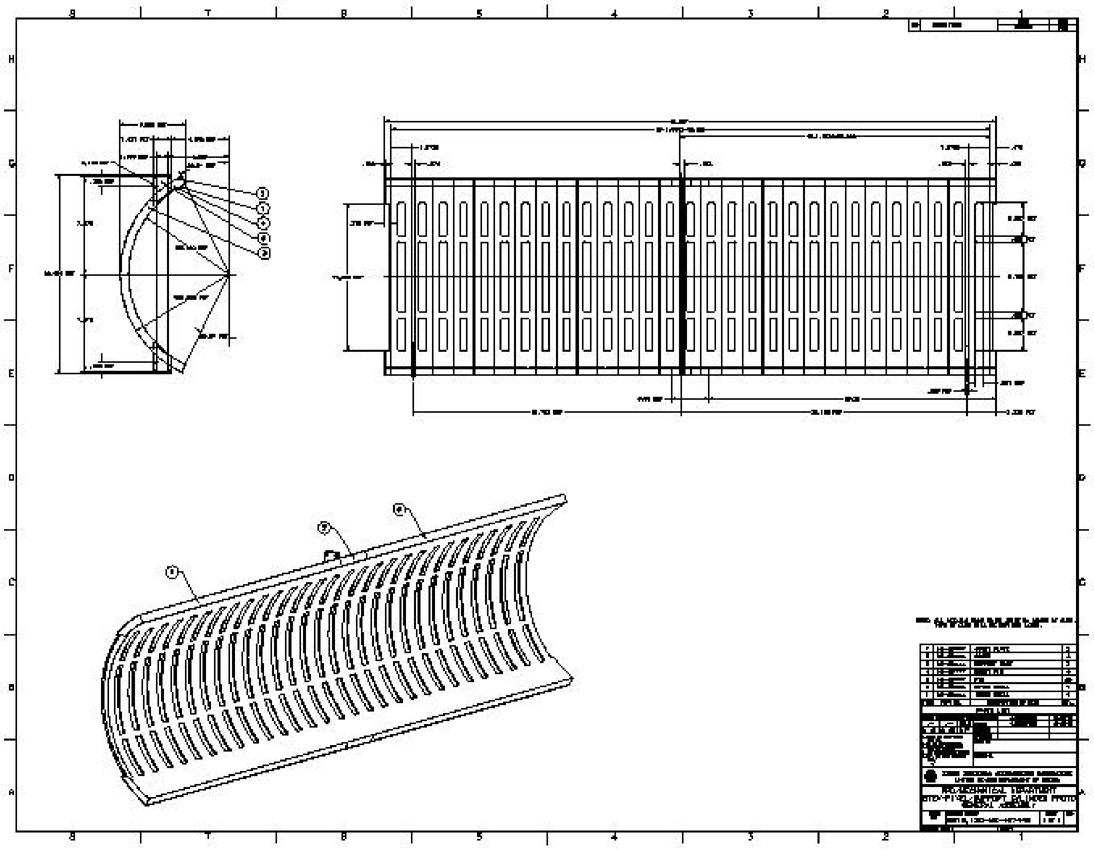

Figure 4.47: Side view of the support structure for the pixel detector.

4.5.8 Vacuum vessel

The whole pixel detector will be placed inside a vacuum vessel. Figure 4.49 shows a conceptual design of the vacuum vessel. The vessel is a rectangular box with a length of 165 cm and a square cross-section of 59.5 cm on a side. The vacuum vessel has a number of penetrating holes. Those holes are needed to provide the connections to the beam pipe, vacuum, cooling and positioning systems. The design of the vacuum vessel is driven by its functional requirments:

- Because of the presence of a strong magnetic field of about 1.5 T and the vacuum requirement, stainless steel 316L will be used;
- The body of the vessel should be vacuum tight;

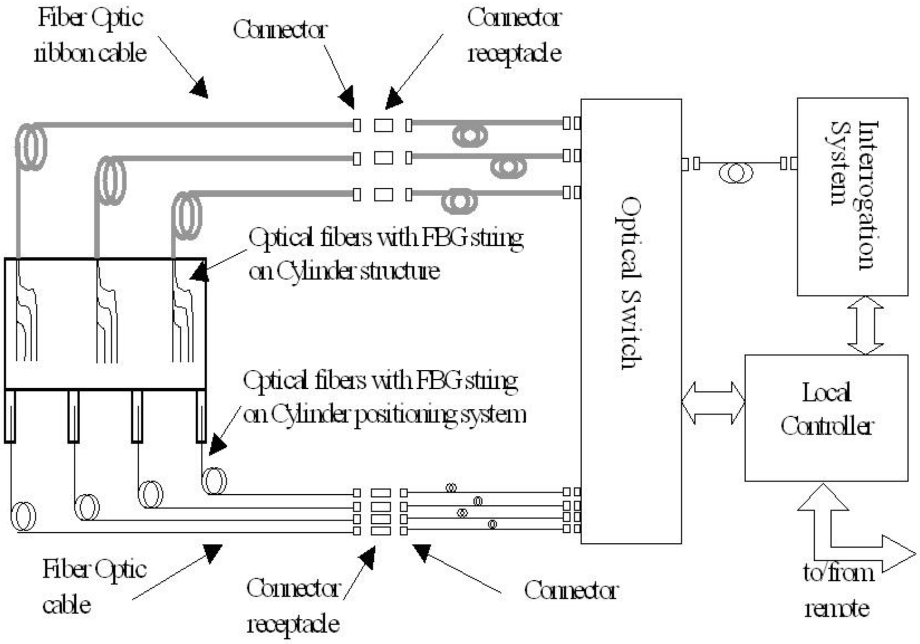

Figure 4.48: Schematic of the FBG system.

- The vacuum vessel has to be mechanically stiff enough to maintain position of the pixel planes to within 20 μm during data taking.

FEA is used to calculate distortion of the vacuum vessel under different loading conditions. As a result of this calculation, we will use 1 and 1.5 inch thick stainless steel plates to build the vessel. The final number of penetrating holes, as well as their diameters and positions, are not yet fixed because of uncertainties about final configuration of vacuum, cryogenic and detector positioning systems. When all these systems are finalized, we will perform another round of FEA calculation and complete the detail engineering drawings.

4.5.9 Cooling

The full heat load is dominated by the readout chip. This heat load is expected to be ~ 0.5 W/cm^2. A much smaller load comes from the sensor leakage current. This latter heat load will grow with radiation damage, from about a few μW/cm^2 to up to few tens of mW/cm^2 after a few Mrad of irradiation. The pixel device is expected to operate at temperatures from -10 to -5°C. Maintaining these temperatures even when the devices are not in use minimizes the effects of radiation damage. Thus, a cooling system must be designed for these temperatures. The maximum operating temperature of all the pixel sensor modules

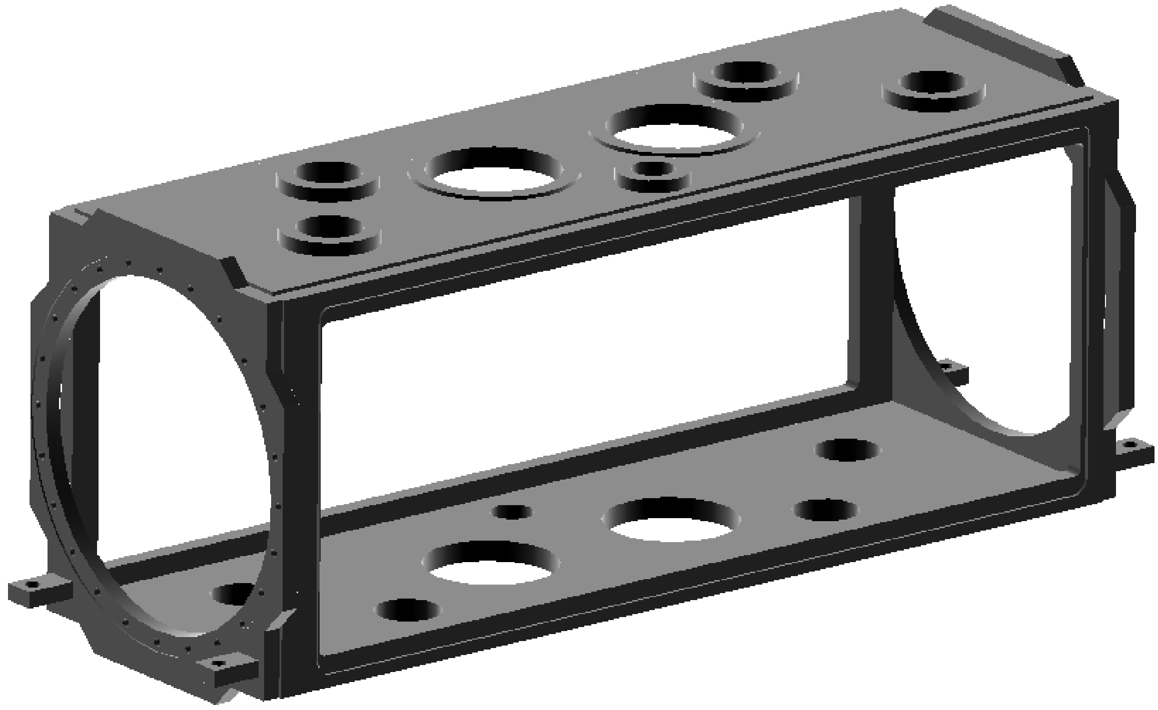

Figure 4.49: Schematic showing the pixel vacuum vessel.

shall not exceed 0°C. To avoid any excessive stress on the bumps, the minimum operating temperature of the pixel sensors shall be above −15°C.

The alignment precision of the modules has to be kept to a high precision. Thus, the temperature must be controlled and reproducible. Since the operation is well below the temperatures at which the devices will be assembled, the coefficients of thermal expansion must be considered in the mechanical designs. Thermal uniformity across the substrate is determined by the potential thermal warping due to mis-match in CTE between substrate and silicon, (hence loss in alignment accuracy) and by the thermal stress on the bump bonds (leading to damage and possible dead channels). The thermal uniformity shall not create any thermal stress on the substrate, the bumps, and the epoxy layers which may lead to the loss in alignment precision of the modules. The maximum temperature excursion, once equilibrium is reached, shall not exceed ±3°C on any sensor module, and the deviation from the median temperature for different areas on the whole substrate shall be kept to a minimum so that no thermal stress and distortion of the substrate will be created.

Cooling of the pixel detector is done by conduction using the excellent thermal conductivity property of TPG. The vacuum system will have cryopanels and liquid nitrogen lines placed inside the vacuum vessel. We take advantage of this and use the liquid nitrogen lines as a heat sink. Fig. 4.50 shows the design of the cold block assembly placed inside the vacuum vessel which consists of a liquid nitrogen tube and copper tabs. The tube is made of 5/8" diameter (outer) stainless steel and will carry liquid nitrogen at a pressure of 8 bars. To spread heat coming from the pixel modules on the half-stations and to allow attachment of the TPG substrates to the tube, copper tabs will be brazed to the tube to serve each half-station. To accommodate the movement of the detector during beam refill, bellows will be added to the tube at both ends. Each half-detector will have two cold blocks assemblies. The whole assembly will be placed outside the geometrical acceptance of the pixel detector. Control heaters will be attached to the substrates to maintain the stability of the temperature under various conditions.

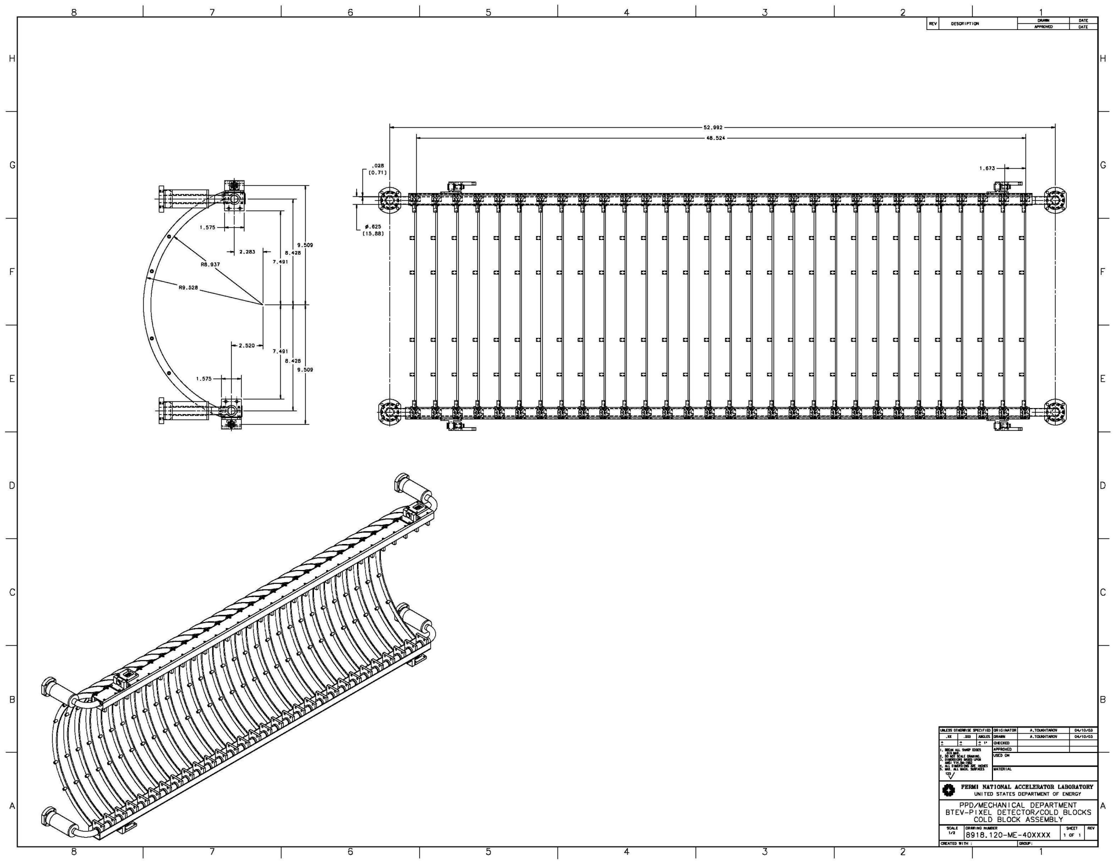

Figure 4.50: Drawing showing the liquid nitrogen cooling line inside the vacuum vessel.

4.5.10 Vacuum system

The design goal of the vacuum system is to have a pressure of 1×10^{-8} torr inside the pixel vacuum vessel, especially in the region where the colliding beams will go through. The pumping requirement for the BTeV Pixel Detector is based on the gas load measurements of the 5% model. The outgassing rate of the model at room temperature was measured to be 5×10^{-4}torr-L/sec. The main component was water with the next component being nitrogen which was present at the level of 1% of the total. For the entire pixel detector, at room temperature, the expected gas load due to outgassing is roughly 10^{-2} torr-L/sec. The vacuum pumping system will consist of surfaces that are cryogenically cooled. The amount of cold surfaces required to pump water and to pump nitrogen is calculated considering the density and flow of the particles inside the vertex detector.

The vertex detector vacuum specification of 1×10^{-8} torr requires a gas density of 5.3×10^{-10} mole/m^3 regardless of the temperature. A gas load of 10^{-2} torr-L/sec at room temperature is equivalent to a particle flow released inside the vertex detector of about 5×10^{-7} mole/sec. At this molecular flow rate, we have calculated that with a cryogenically cooled surface area of 5.4 m^2, the required gas density is achievable.

4.5.10.1 Description of the Vacuum System

The vacuum system is made up of two integrated "cryopumps" plus additional surfaces at liquid nitrogen (LN_2) temperatures within the vacuum vessel [26]. A set of liquid helium cooled surfaces will pump gases such as nitrogen and hydrogen that are not condensable on a surface at the LN_2 temperature. A set of liquid nitrogen cooled surfaces will pump water vapor. The major pumping components are shown in Figure 4.51. The cryopumps, shown in Figure 4.52 and 4.53 have LN_2 cooled copper surfaces surrounding a set of surfaces cooled by gaseous helium (GHe) to about 20°K and inside those a set of about 4°K liquid helium (LHe) cooled tubes covered in charcoal. The innermost, and coldest surfaces are primarily for pumping hydrogen. The 20°K surfaces are for pumping nitrogen and the large LN_2 cooled surfaces are for pumping water. The cryopumps are located along the top and bottom walls of the vacuum vessel. The water pump is made of several components. Besides the LN_2 surfaces in the two cryopanels, the cold block assembly in the pixel cooling system and the cable strain relief bars provides additional LN_2 surfaces for pumping water vapor.

Figure 4.54 shows the details of the layout of the piping for the vacuum and cooling system. Each LHe cryopump is supplied by its own dewar. Liquid helium enters the pixel vacuum vessel in the cryopump at 4°K. Helium gas leaves the cryopump at 20°K. A cold block assembly and the thermal shields for a LHe cryopump share a LN_2 dewar. For conservation, liquid nitrogen is pumped from a phase separator back to the inlet. When the BTeV vacuum vessel is brought up to atmospheric pressure, nitrogen coming from the phase separator is used.

Pump for non-condensable gas The option of using commercial cryopumps has been investigated. Due to the limited space around the vacuum vessel inside the magnet, the conductance any piping leading from the vacuum vessel to a remotely located cryopump is not adequate to remove the non-condensable gas. This leaves the requirement that the cryopump be located directly on the vacuum vessel. However, after installation of the vessel inside the magnet, the cryopump is not accessible for maintenance. As a result, it is not

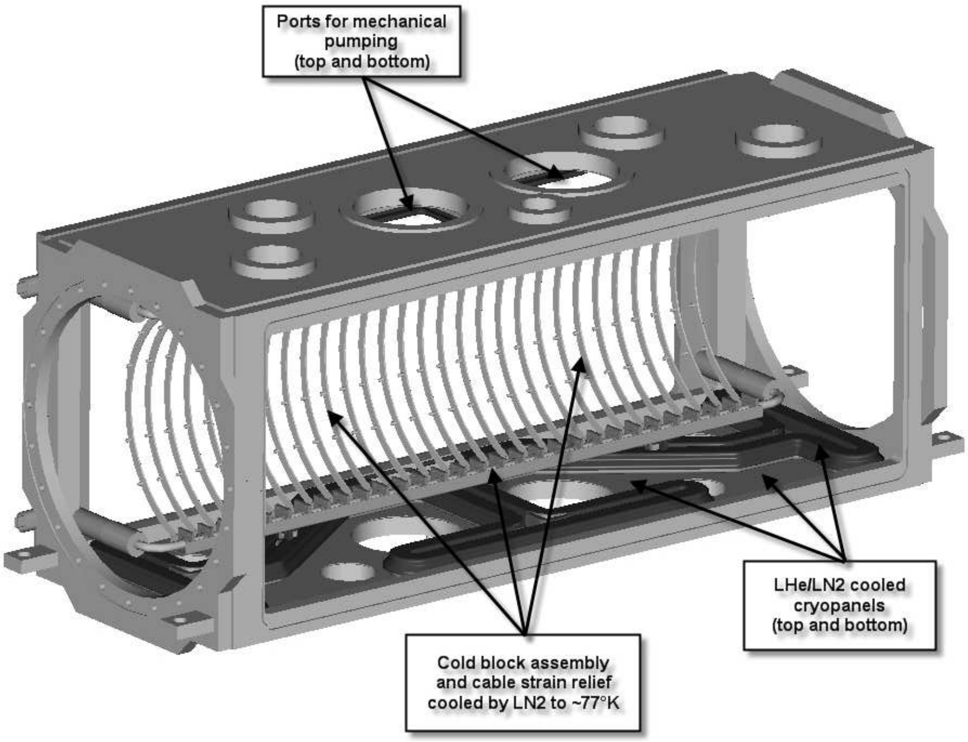

Figure 4.51: Components of the vacuum system for the pixel detector.

possible to use commercial cryopumps because they require maintenance service every 10,000 hours. Also, the commerical cryopumps need to be magnetically shielded so they can operate in a magnetic field of less than 300 gauss. The required magnetic shield will not fit in the space that we have. As a result, it is not possible to use commercial cryopumps.

To pump non-condensable gases such as nitrogen and hydrogen, we will install inside the pixel vacuum vessel two liquid helium cryopumps as shown in Fig. 4.53. Figure 4.52 shows the thermal shields layout on top of the vacuum vessel wall. Figure 4.53 shows the cross section of the thermal shields and the piping within the cryopump. The central part of the pump is made of 4-mm stainless steel pipes carrying liquid helium ($\sim 4°$K). They are covered by charcoal to pump hydrogen. The charcoal capability to be degassed at room temperature is very important for this application. The gaseous helium boil-off ($\sim 20°$K) cools a set of thermal shields that surround the charcoal-covered pipes. The copper shields, each having a thickness of about 1 mm are thermally coupled to these helium gas pipes. The warmest stage of the cryopump is the set of copper radiation shields that are cooled by liquid nitrogen. The decreased liquid nitrogen temperature reduces the power going to the liquid helium lines so that less liquid helium needs to be supplied to the cryopump. The liquid nitrogen flows through the 6-mm inner diameter pipes. The full cryopump assembly takes up a space if 130 cm by 45 cm by 4.7 cm. The overall pumping speed of these two cryopumps

Figure 4.52: Thermal shields of the cryopump.

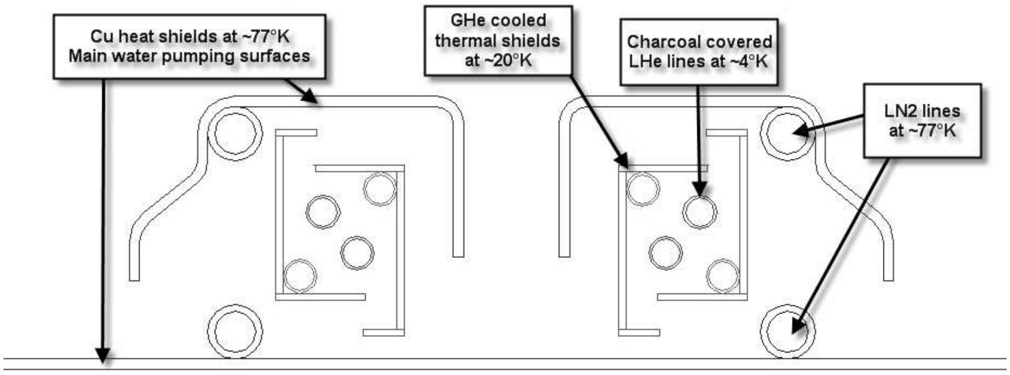

Figure 4.53: Cross-section of the three-stage LHe cryogenic pump. As LHe is heated, the GHe flows through the lines that cool the inner thermal shields to 20°K. The LN_2 shield sits 3 mm away from the room temperature vacuum vessel wall.

for hydrogen depends on the charcoal temperature; it changes from about 500L/sec at 5°K (hydrogen condensation coefficient on the charcoal about 0.05) to more than 5000 L/sec at less than 3°K (when the condensation coefficient should be about 1).

Water Pump There are serval parts to the water pump: the cold block assembly, the cable strain relief structure, and the radiation shields of the cryopumps. The cold block assembly is the heat sink for the substrate temperature control system (see "Cooling" section). For each half of the detector, there are 60 tabs (copper cold blocks) that are the thermal connections

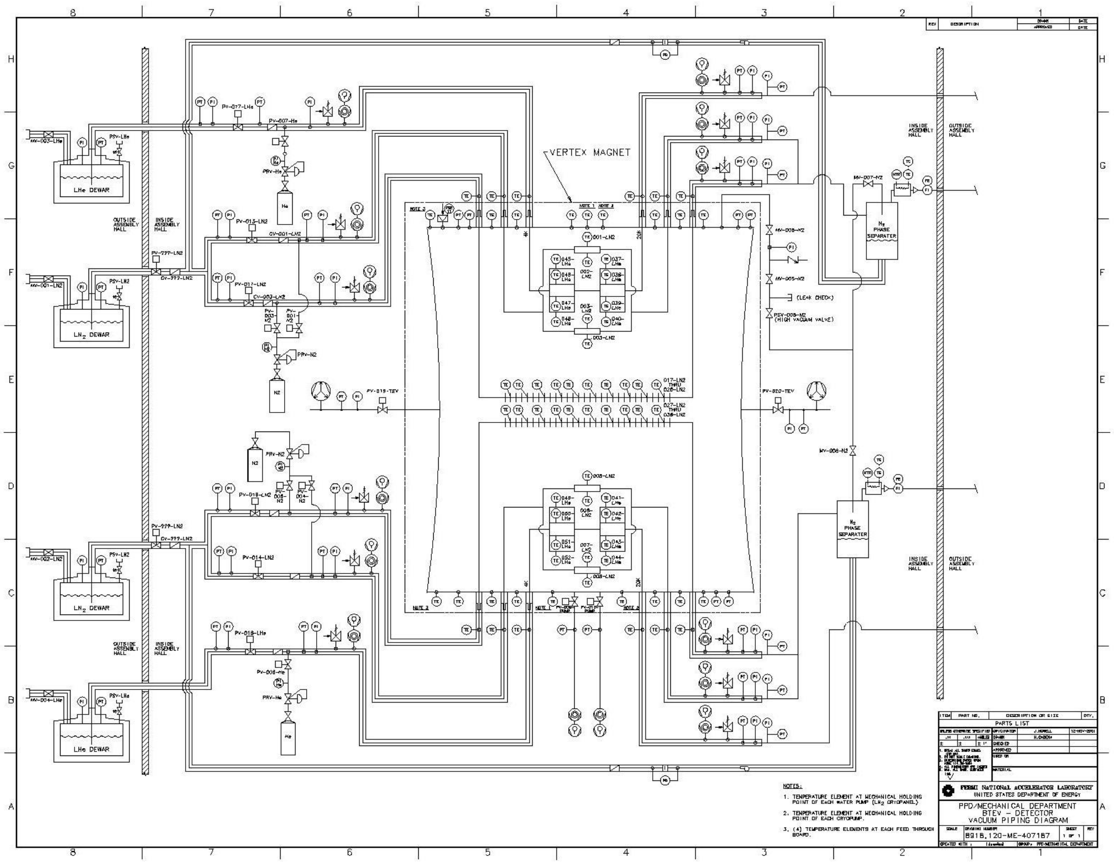

Figure 4.54: Layout of the vacuum system for the pixel detector.

from the substrates to the liquid nitrogen heat sink. Liquid nitrogen flows through two tubes passing through tabs (copper cold blocks). The surfaces of the cold block assembly that are readily exposed to the pixels, namely the channels and the tabs, are cold enough to act as water pumps with a total surface area of 5200 cm^2.

Each of the two cable strain relief structures consists of 30 aluminum C-shaped plates. The aluminum structures are thermally connected to the heat sink. The thermal conductance of the aluminum makes the temperature in the structure range between -195°C and -139°C, if the heat sink is at a temperature of -195°C. Note that a secondary benefit of the cable strain relief structure is that it acts as a radiation shield around the sides of the pixel detector, thus reducing the temperature of the detector and helping to reduce outgassing. The surface area of one plate is 170 cm^2. Thus the total surface area of the strain relief structure as shown in Fig. 4.55 that pumps water is 5000 cm^2.

Another large contribution to the water pumping comes from the thermal shields of the two liquid helium cryopumps. The toal effective area of the cold block assembly, the cable strain relief structure, and the shields of the liquid helium cryopumps is 5.4 m^2 and a water pumping speed of 800,000 L/sec. Note that in all the calculations, we have used the outgassing rate measured at room temperature and not considered the significant reduction of this rate at the low temperature of the pixel detector and with the elapsed time under vacuum.

The layout of the vacuum system is as follows: two liquid helium cryopumps will be placed directly inside the vacuum vessel. On the top and bottom plate of the vacuum vessel, there will be vacuum ports with vacuum lines leading from the vessel out to the roughing pumps, which are located remotely outside the magnet. The expected conductance through the lines is on the order of 10 L/sec. An isolation valve is placed in the line between the vessel and each of the roughing pumps. A safety valve is also placed in the system to prevent the vacuum vessel to build up pressure if there is a power failure.

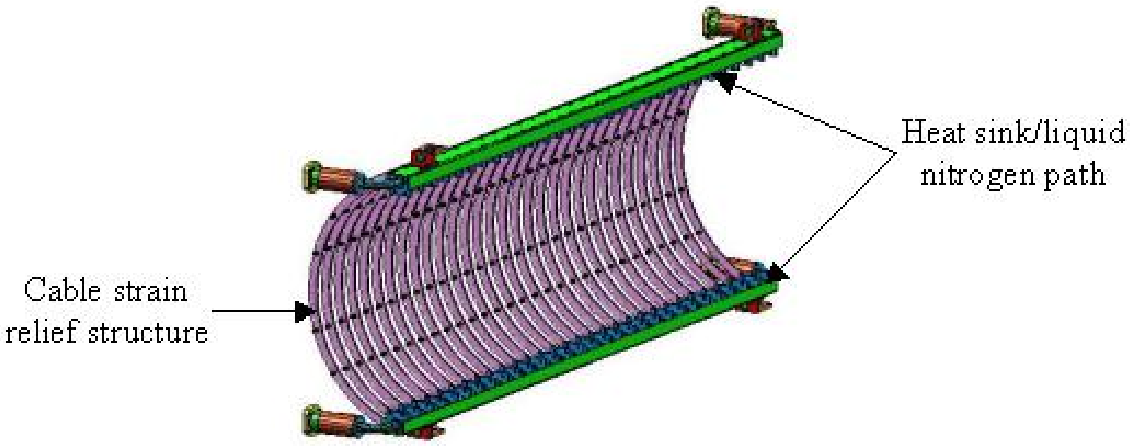

Figure 4.55: Drawing showing the cold block inside the vacuum vessel.

4.5.10.2 Regeneration of cryopanel

Th long-term capacity of a cryopanel cooled with a liquid nitrogen was measured to understand how long it can pump before regneration is needed. The test showed that the cryopanel pumped for an equivalent of 44 weeks of detector operation without any degradation in performance [27]. This was a lower limit because the test was ended only because our supply of liquid nitrogen ran out. This means that we can operate the detector for one full year of running without regeneration. The test also verified that the water condensation coefficient on the cryopanel was about one. Thus the expected pumping speed of $5.4m^2$ of the liquid nitrogen cooled surface is 800,000 L/sec for water vapor. This is enough to bring the detector pressure to 1.3×10^{-8} torr for a gas load of 0.01 torr-L/sec.

4.5.10.3 Pump down procedure

The proposed sequence to pump down the pixel vacuum system is:

1. At room temperature, use roughing pumps to bring the vacuum to 1×10^{-3}torr at speeds of greater than 10 L/sec. This pumping speed depends on the number and dimension of the pipes connecting the fore vacuum port of the cryopumps to the turbo. The larger this pumping speed is, the lower the vessel pressure at which we start the cool down procedure will be.

2. Slowly feed liquid nitrogen to bring all the water pump surfaces to the LN_2 temperature and wait until the pressure and temperature become stable. The substrate temperature is kept stable by balancing the heat applied to the control heaters on the substrate and by flowing cold nitrogen gas through the cold block assembly. The pressure will be brought to the 1×10^{-5} torr scale.

3. Change the setting of the substrate temperature control heaters and adjust the liquid nitrogen flow rate through the cold block assembly to reach the working temperature (-10°C). Then turn on the pixel modules and continue to adjust the control heaters and the liquid nitrogen flow rate to keep the pixels at the desired working temperature.

4. Send the liquid helium to the two cryopumps and wait until the pressure and temperature becomes stable. The vacuum pressure should become about 1×10^{-8} torr at the end of this cool down phase.

4.5.11 Feed-through board

The flex cables will bring signals from the pixel modules to connectors sitting inside the vacuum part of the feed-through boards. From there, the signals will go through copper traces inside the board, and will be taken to the part of the board which is outside the vacuum vessel. Connectors sitting on the part of the board outside the vacuum vessel will be used to bring the signals to external data cables. Because of complication in fabricating large size multilayer printed circuit boards, the complete FTB will consist of six (three top and three bottom) 17x27.5 inches boards. To make vacuum tight joints between the boards and to make the FTBs stiffer, aluminum plates will cover both sides of the board leaving free space for inner and outer connectors and other on-board components. Fig. 4.56 is an engineering drawing of the feed-through board assembly.

4.5.12 Actuators

Four actuators (two at the top and two at the bottom, see fig. 4.57) will be attached to each of the half-detectors. The bottom actuators will be attached to the cold blocks assembly and to the carbon fiber support structure. The top actuators will be attached to the cold block assembly, a third support of the support structure will be created by attaching to the cold block assembly (see Fig. 4.58. This detector supporting scheme is chosen for the following reason. Each cold block assembly has two inlets and two outlets for liquid nitrogen, with each inlet and outlet having bellows to accommodate movement of the detector in and

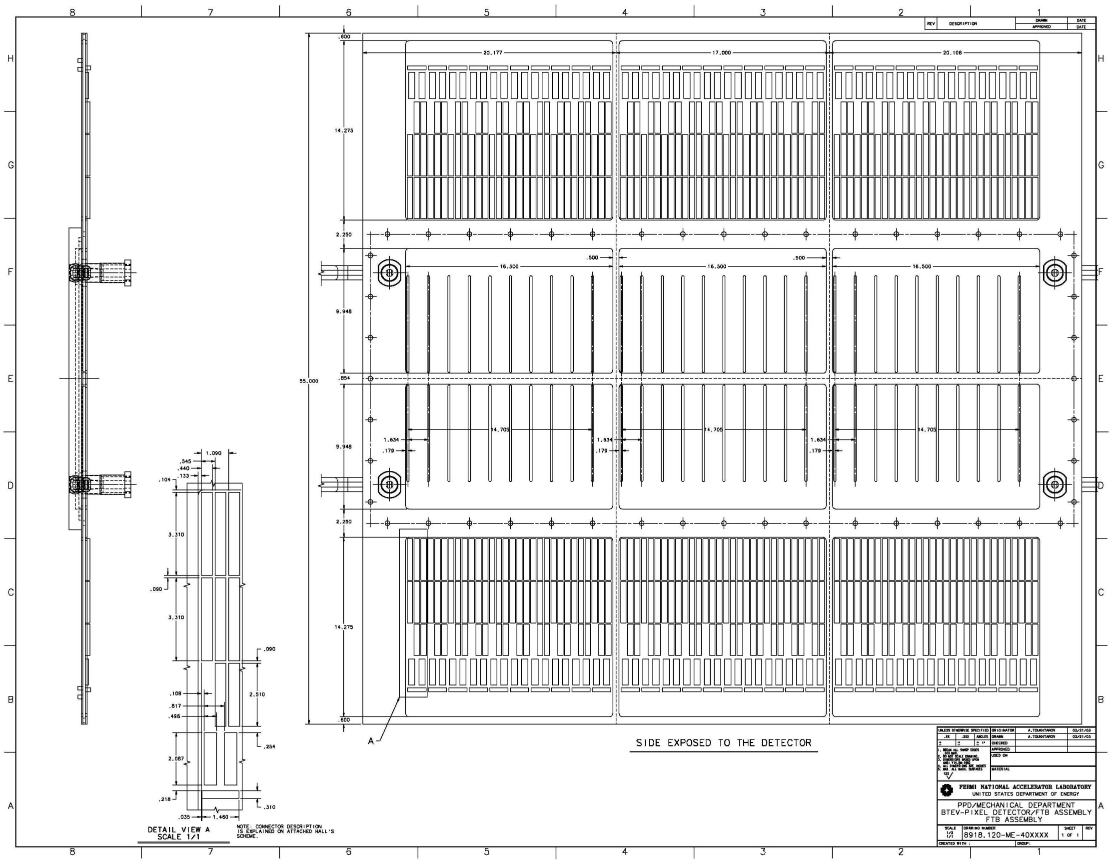

Figure 4.56: Engineering drawing of the complete feed-through board assembly. Signals are fed through the vacuum vessel via these printed circuit boards with high density connectors.

out of the beam. Any difference in the bellows behavior will create excessive forces. These forces, in the case of a three-actuators supporting scheme (e.g. two at the bottom and one on top) will create extra motion of the cold block with respect to the carbon support structure. This extra motion in the worst case scenario can be as large as 5 mm, which is more than acceptable. The solution to this problem is to attach four actuators to the cold block assembly in close proximity to the bellows. At the same time, we have to keep the carbon support structure attached to the actuators at only three points. In other words, we have to provide a kinematic supporting scheme. The actuators will be connected to an external drive system sitting outside the magnet via hydraulic lines.

Capacitive position sensors will be permanently attached to the inner surface of the vacuum vessel and the metallic targets will be attached to the half detectors. A couple of sensors will be installed on each measuring point, one for x and the other for y measurement. Special attention has been given to the choice of location where the sensors will be placed. Our current plan is to place four pairs of sensors per half detector. They will be mounted close to the end window openings. Final alignment and sensor calibration will be done after the detector halves have been installed inside the vessel and attached to the actuators. This design has quite a lot of redundancy (since only 5 sensors will be enough to define the detector position), but it is conservative and will reduce risk in case of sensor malfunctioning. With this scheme, any distortion in the pixel detector support structure will be detected.

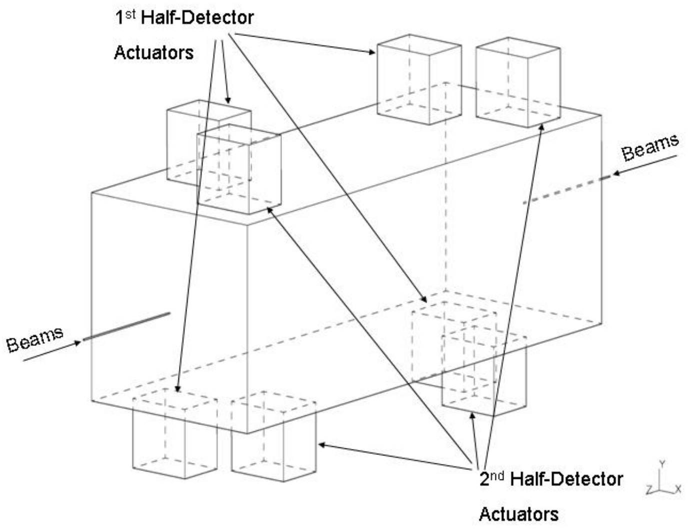

Figure 4.57: Schematic drawings showing the locations of the actuators

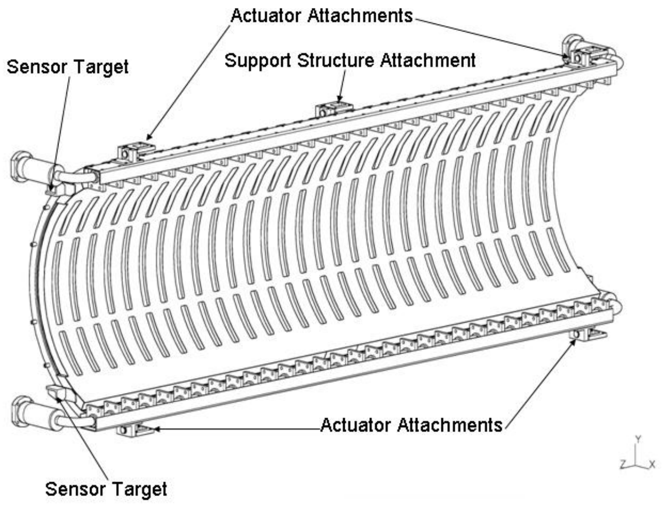

Figure 4.58: Locations of the actuator attachment and sensors on the pixel half-detector

4.5.13 RF shielding

The performance and readout of the pixel detector should not be unduly perturbed by the presence of the circulating beams. On the other hand, the presence of the detector must not affect the operation of the Tevatron or degrade the beam conditions at other IR's by parsitic coupling. An rf shield design is needed to suppress the wake-field and beam instabilities. We are currently exploring the use of a number of CuBe wires of 125 μm in diameter or four thin ($\sim 50\mu$m) but wide strips made out of stainless steel. In either case, the wires or strips will extend beyond the length of the vacuum vessel and the exit windows by as much as 4 meters on both ends. Their distance to the beam axis is adjustable between 20 mm (for injection) and 5 mm for data-taking. This can be done by either having a separate set of actuators or by coupling their radial movements to those of the pixel detector stations.

4.5.14 Power distribution

The power supplies to the pixel detector must provide:

- Low voltage for the electronics
- High voltage bias for the silicon sensors
- Power for the various accessories for the operation of the detector. These include position control system, cooling system, and the temperature control system.

We envision two options for the location of the power supplies: outside and inside the experimental hall. The first option simplifies the design and procurement of power supplies, but imposes restriction on the distribution cables. The cables can act as EM pick-up elements conducting noise into the detector or generating conductive paths between the different layers of the detector.

The second option imposes more challenges due to the need of locating DC-DC converters near the detector to break conductive paths and decrease the EM pick-up. The pixel detector will be subject to strong magnetic field, which does not allow any magnetic material in the design of such converters. Experience at CDF also showed that radiation effects would be significant inside the enclosure.

Our baseline design will have the HV power supplies installed in the catwalk that will be located just outside the experimental hall. The LV power supplies will be located inside the experimental hall, near the walls of the enclosure. A power distribution system will be developed, tested, and installed.

4.5.15 Control and Monitoring

The BTeV Pixel system requires continuous and careful monitoring in order to ensure safe and continuous operation during its long lifetime. It also needs a system which can be used to actively control the many inaccessible and complex pieces of hardware that make up the detector. Finally, a system to continuously record critical parameters is needed to watch for drifts in the many parameters so that problems can be diagnosed and corrected before they become critical.

The pixel monitoring needs can be divided into the following distinct groups:

- Cooling system
- Temperature control system
- Low and High Voltage power supply system
- Radiation Monitoring
- Vacuum system
- Actuators and position sensor
- Rack protection

These systems include the monitoring of a wide variety of parameters including pressures, temperatures, positions and flow rates. In addition, the complex vacuum system require active feedback and control of critical parameters. For less time critical monitoring appropriate limits will be set and an alarm will be issued should such limits be exceeded. In some cases, the alarm should automatically initiate a turn-off sequence to prevent any major damage to the system. For example, any signs of failure of the vacuum or cooling system should automatically trigger a mechanism to turn off all HV power and interface with the appropriate Tevatron alarm/interlock systems. Earlier this year, during the preparation for the pixel beam test at Fermilab, we implemented and tested a slow control and monitoring system based on APACs hardware and IFIX software. This is a system used by CDF and MINOS and is commonly found in American and European industry. We have successfully used the system to control the HV to the pixel sensors, LV to the readout chips, and monitor the temperature of the pixel detectors and coolant reservoir. We continuously monitor the current drawn by the sensors and the readout electronics and remotely control the position and angle of the mechanical box holding the detectors. This gives us valuable experience in testing the APACS hardware and IFIX software systems. In addition, this system is being expanded to include the BTeV RICH test beam monitoring system and will be further integrated with additional BTeV test setups as they are installed in the testbeam. Based upon these experiences, we will work together with the DAQ group and the relevant Fermilab departments to design and develop a system that is capable of meeting our needs and those of BTeV as a whole.

4.6 Ongoing Prototyping Efforts

Prototype substrates made out of TPG have already been received. A complete half-station is currently being assembled using mechanical grade silicon modules. This will give us experience in testing assembly of modules on the TPG using prototype fixtures. Once assembled, our plan is to test the thermal performance, check the thermal profile, and to study any thermal stresses and displacements at different operating temperatures.

One issue that still needs to be addressed is how to optimize the thermal connection of the heaters (which are needed for temperature control of the system) to the substrate, thus confirming the effective CTE of the assembly. Testing of a prototype control system will measure the time constant of the system. The time constant of the substrate temperature control system will be sufficiently short during the power failure. The temperature transient will not experience overshoot. The temperature change during the transient, in case of failure in the pixel power supply, will not exceed 15°C, as shown in a thermal modelling calculation[28]. This assumes that we will have uninterrupted power supply to feed the heater power in the pixel detector[29].

We have already made a full-size stainless steel cooling tube carrying LN2 with copper cold blocks brazed to it (see Fig. 4.59). Tests of the prototype cooling tube will begin soon. We will check the thermal profile at various places along the tube as a function of flow rate and applied heat load. The measurements will then be compared with our calculations. Possible vibration caused by the liquid nitrogen flow will also be studied. The design of the vacuum system is very advanced and we will test prototypes of the cryopumps this year.

Another critical area that needs to be addressed is the shielding from EMI effects due to the circulating beams. We have done first measurements using the rf shielding test setup to study the effect on the noise and threshold of a FPIX1-instrumented pixel detector. These measurements will continue with rf amplifiers of much high power to mimic the Tevatron beams.

We are ready to produce full-sized feed-through board prototypes. Once received, these boards will be tested both electrically and mechanically. Effects such as cross-talk, signal integrity, high voltage performance will be studied under normal and vacuum conditions. We will also study outgassing and check whether the boards are leak tight.

We have some conceptual ideas on the pixel data combiner board. These ideas will need to be turned into a specification and design. This is now one of our priority items that we would like to address during the next year.

We plan to do a series of beam tests using the MTEST facility at Fermilab. The goals of the tests are to study charge collection and efficiency of the p-spray sensors before and after irradiation. We will also study the performance of the 5-chip FPIX1 modules, and the performance of the new FPIX2-instrumented pixel detectors.

A moderate scale module assembly is also under way. We will assemble up to 50 FPIX2 modules of different types using a new HDI design. We hope that all the assembly and testing issues of the pixel modules will be fully understood after this round of prototypes and we can head into pre-production. Concurrently, a large scale wafer thinning program has started and we will work with industry to fully master the technique of thinning 8" wafers with bumps put on.

Lastly, we will continue to study system issues. From our test beam experience, as well as operational experience from other large experiments, systems issues such as power supply, grounding, cabling, and connectors are potentially the most problematic areas. A system demonstrator will be built to test the cooling system, the temperature control system, the vacuum system, the electronics readout system, and gain experience of operating the pixel detectors under conditions that will be close to the final BTeV experiment. The test will include one or more half-stations with working pixel modules fully assembled on it, a full size support structure, feed-through boards, control heaters, and the cold block assemblies. The gas load of the full sized model will be measured to better understand the total outgassing rate of the materials used in the detector assembly. Various operating conditions will be studied to test the temeprature control system. Figure 4.60 shows a sketch of the test setup. This demonstrator program will be carried out early in the construction phase of the project. Another critical issue that we will need to address is the effect on the pixel detector during unforseen beam incidents in which the pixel detectors may see a large particle flux in a very short time. We plan to study this with a few pixel modules in the Booster irradiation facility some time next year.

To understand and address more complicated system issues, we plan to assemble a 10% pixel system after the demonstrator test. With such a system, we can also carry out a thorough investigation of a complete electrical, mechanical and cooling system. This will also enable us to operate a small system in the real C0 environment. This system will be placed outside a normal beam pipe. Issues such as grounding, shielding, and fast readout coupled to a prototype trigger processor can be studied in detail there. At the same time, it will allow us to understand the yield at the various steps of production, as well as how to assemble reliably the full scale pixel system. We will use parts that are procured during the preproduction phase for this system test.

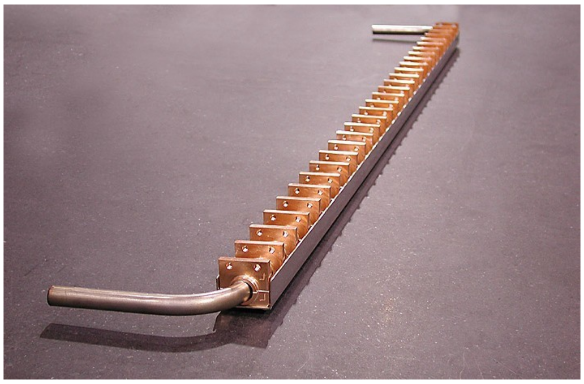

Figure 4.59: Prototype liquid nitrogen cooling line with copper tabs brazed to the stainless steel tube.

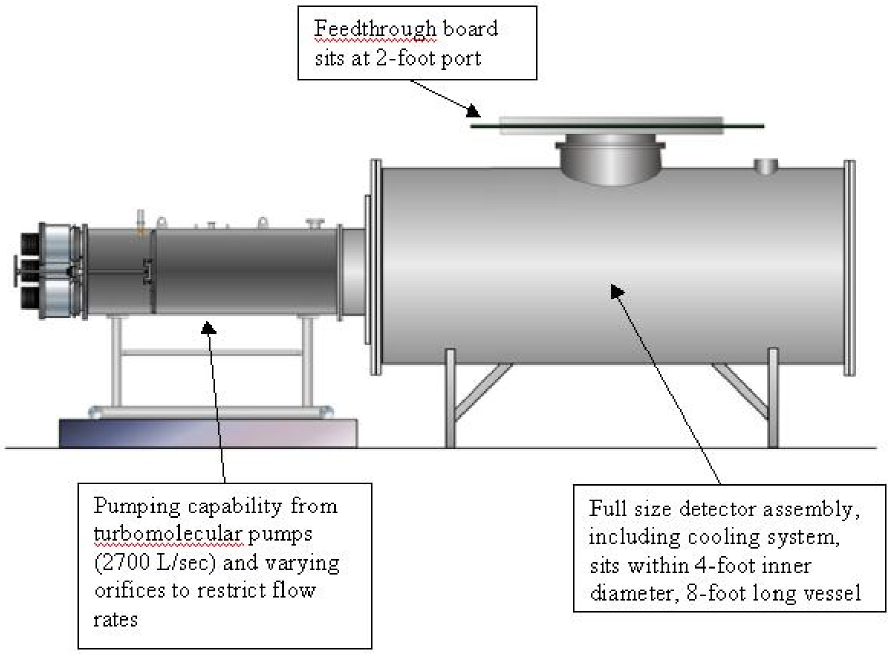

Figure 4.60: Schematic of the system demonstrator setup.

4.7 Production - QA and Testing

4.7.1 Overview

The key to keeping the project on schedule and on budget is the extensive testing and qualification of the components and of the product at each step of the assembly. The basic building block of the pixel detector is a module, which is composed of a pixel sensor bump-bonded to a number of pixel readout chips. Underneath the readout chips on the module, a high density flex cable (HDI) will be glued. The readout chips will be wire-bonded to the HDI and the latter will carry all the signal, control, and power lines from the pixel module to the DAQ system. The HDI will in turn be attached to a pixel interconnect flex cable (PIFC). All of these individual components will be tested before assembly. A few of the groups involved in the pixel project will be equipped with probe stations that can test the sensors, HDI, and flex cables. Furthermore, a common PCI-based test-stand will be used at all sites for hardware checks and software development and debugging. Databases will be used extensively so that all production and testing information will be readily accessible at all sites. We also do cross checks and calibration so that the same high quality testing procedure and standard can be maintained at all sites. Lastly, we intend to have specifications documents, detailed quality control planning, vigorous test procedures established with commercial vendors for critical components to ensure that only products that passed our acceptance criteria will be delivered. To ensure this, we intend to do a lot of testing at the vendor sites. We have already gained good experience with one sensor vendor during our latest submission. These quality control plans and procedures will be developed as the project moves to the construction phase.

The assembled pixel modules will undergo initial functionality tests followed by burn-in testing. The modules that pass the burn-in testing will then be mounted on a support substrate to form a pixel half-station. Next, all modules on a half-station will be fully tested for electrical and readout problems. Before assembly, each substrate will be tested for mechanical tolerances and thermal conductivity. A separate cooling test will be performed to insure that the pixel half-station achieves the designed operating temperature. During this process, all assembly and alignment parameters will be recorded in a database.

The pixel stations will next be mounted to a carbon support shell to form a half-detector. During this step, the position of each pixel half-station will be measured and the information will again be recorded in a database. Once the half-detector is fully assembled, each half-station will be tested and read out. This testing will be repeated after the half detector is inserted into the vacuum vessel at SIDET.

When both half-detectors are inserted and all cables and connections inside the vacuum vessel are properly installed, connected, and tested, the vacuum vessel will be closed. Before transporting the vessel from SIDET to C0, a number of additional tests will be performed. These include:

- **Vacuum test**: the vessel will be pumped down to check for possible leaks
- **Cooling test** - Leak tightness and temperature performance will be checked with the vessel under vacuum and then the modules fully powered.
- **Electrical test** - the modules will be powered up to check for continuity
- **Readout test** - all modules on a half station will be readout simultaneously
- **Actuator test** - the half detectors will be moved closer and further apart and the read-back sensors calibrated.

When the pixel detector has passed all these tests, it will be ready for installation.

4.7.2 Sensor Tests

To ensure high quality of the pixel sensors, we plan to have a series of quality assurance(QA) checks to be performed by the vendors and by the pixel group. Fermilab will serve as a central distribution and control center with dedicated testing and coordinating (with the vendors and other institutes) tasks. There will be one or more other testing sites set up and the QA program will be carried out in a consistent manner at all places.

The vendor is required to perform checks and tests to ensure the wafers will be selected and processed according to our specification and their design rules. Consistency of the processing will be checked by the vendor using Process Control Monitors (PCM) of their choice. Information on the consistency of the alignment and processing will be provided to us. I-V and C-V measurements are to be performed on the diodes, single chip devices, and the modules.

All the delivered sensor wafers will be tested at Fermilab and other testing sites. These include visual inspection, I-V measurement and C-V measurements on all modules and single chip devices. A subset of the wafers will also be subjected to additional tests. These include:

- Leakage current stability over time
- Flat band voltage measurements on MOS test structure
- Current measurement as function of gate and revserve bias for gate controlled diodes
- Sensor thickness and warping
- Irradiation test on selected single chip sensors and test structures

For consistency, cross-checks will be performed on some detectors and wafers to make sure that measurements at various sites agree with each other.

4.7.3 Pixel Readout chips

All the received wafers of the pixel readout chip will be probed at Fermilab. We have already acquired some experience of testing the first batch of FPIX2 wafers. These tests include powering sequence, checking of the voltage and current levels during quiet and operation mode, loading and reading back of a test pattern at high clock speeds using one to all of the serial lines. We may also do more detailed checks such as determining the noise and threshold performance of all pixels. The chips that pass the criteria will be marked and the known-good-die (KGD) map will be sent to the bump bonding vendors. One or more wafers will be diced up so that we can carry out characterization tests to check on functionalities and performance. Chips from these wafers will also be irradiated to check their performance after irradiation.

4.7.4 Bump Bonding

The tested sensors and readout chip wafers will be sent to one or more bump bonding companies to be flip-chip mated to produce the pixel detector modules. We would like to have the readout chips thinned down to 200 microns. Thinning will be done in another company. A database is necessary to keep track of all the shipment of the wafers. We are currently discussing with the prospective vendors on a detailed QA plan. Tests will be performed by the vendor to check on the quality of bump deposition and the strength of the bump-bonds. These tests include visual inspection, automatic checking of the bumps on the wafer using a profiler, and scanning electron microscopy. Pull tests will also be performed randomly on test structures to check the quality of the mating. After hybridization, the integrity of the mating will be checked by several means. Some of the modules will be X-rayed at Fermilab and a record of all the X-ray images will be kept. Some single chip detectors will also be made, and these detectors will be tested to study their performance. We also plan to do probing tests of all the modules. I-V and C-V measurements will be carried out on the sensor of each module to compare its behavior before and after bump bonding. These tests will be performed at Fermilab. The equipment needed will be the same as for probing the sensors. A small complication in the process flow is the issue of thinning. At this point, we assume that thinning will be done after the bumps have been put on the readout wafers. Note that the sensor wafers will be delivered to us at the thickness we specified, since the sensor fabrication uses a double-sided process. If needed, the inspection and testing of the bumped-readout-chip wafers after thinning will be done at Fermilab.

4.7.5 HDI and interconnect flex cable

The HDI will come in 5 different types, one type for each module type(size), with the ones for the 1x4 module having right and left-hand versions. All together, there will be 5 types of HDIs. Including factors due to production and assembly yield, extra quantities etc, we will need close to 2000 HDIs in total. Each HDI has to be tested for shorts, broken lines, open vias, and bad wire bond pads. Surface mounted components have to be assembled on the HDIs. Each HDI will need to be bonded to a Pixel Interconnect Flex cable. The joint technology to be used is still being evaluated. Options include wire bonding, small connectors, solder pads, and z-axis conductive adhesive. The bonding and the line integrity have to be rechecked afterwards. Tests will need an optical microscope and simple probe station (due to the fine line spacing and width). Tests and assembly of the HDIs will be done at Fermilab, Iowa, and Wayne State University. The PIFC will be used to connect the pixel module (the HDI) to the feed-through boards. The two cables, HDI and PIFC need to be joined together. Testing of the PIFC will be done at Fermilab, Iowa and possibly Wayne State University. The joining of the HDI to the PIFC may need a special fixture. This process will be done at Fermilab.

4.7.6 Data Combiner Board

The pixel data combiner board will be used to assemble the data from the pixel modules and sort them according to time-stamps. These time-stamped pixel hits will then be sent to the L1 trigger processors. One pixel data combiner board will be needed per pixel half-plane. Fermilab and Tennessee engineers will be responsible for the electrical testing of these boards.

4.7.7 Substrate

The pixel modules will be assembled on a TPG substrate. Each substrate will form the mechanical support for a half-plane. There will be 120 substrates in total. The substrate will need to be encapsulated before the placement of pixel modules on them . All substrates will be produced by industry. Encapsulation will be done at Fermilab. At the two ends of the substrate, a flexible part made from Pyrolytic Graphite Sheet (PGS) will be glued. The substrates will need to be checked after delivery. They will be visually inspected for any defects and non-uniformity. They have to be measured for flatness, dimensions, and be checked for thermal performance. The substrates will then be machined to the right size. Precision alignment pins or fiducial marks will be placed on the substrate. The testing and machining will be shared between FNAL and Iowa.

4.7.8 Substrate support structure

Fermilab will be responsible for the fabrication and testing of the substrate support structures. This structure will come in two halves. Pixel stations will be mounted to the substrate support structures using mounting brackets. Frascati will be responsible for checking the stability tests on the support strcture. They will also be responsible for performing a feasibility study on the in-situ checking of any long term deformation or creeping of the structure during operation.

4.7.9 Feed-through board

The feed-through board is a very complicated multilayer printed circuit. These boards are needed to bring the signal, control, and power cables from outside the vacuum vessel to the pixel modules inside the vessel. It will be manufactured and assembled by industry. The boards will be tested electrically by the manufacturer and only boards which pass the tests will be sent to us. At Fermilab, these boards will be tested mechanically for outgassing and vacuum leak-tightness. Electrical tests will be repeated under vacuum conditions. Six of these boards will then be glued together with aluminum support frames to form one side of the vacuum vessel. The glued joints will be checked for vacuum properties.

4.7.10 Database

The amount of information that we have to keep track of during the production and assembly of the BTeV pixel detector is enormous. This includes the various parameters from the large number of components that need to be tested, the assembly and alignment parameters, voltage and threshold settings, current limits, and various monitoring information such as temperature and pressure. Furthermore, there will be a number of vendors involved for the components and at various stages of the assembly. We will have to keep track of the inventory and the parts flow at each step of the process. Finally, a number of institutes will participate in the testing of the components and we need to maintain a stringent and uniform quality control for the testing of the components. For these reasons, we need a production and testing database to store all the information.

We will learn as much as we can from the experience of the Tevatron (CDF and D0) and LHC experiments (ALICE, ATLAS, and CMS). Together with the Fermilab Computing Division, we will design and develop a relational database to track and identify each piece of all the components. The database will consist of:

- Detector construction database: this keeps track of all the components and their detailed test results
- Electronics manufacturing database: this keeps track of the shipping of all the different wafers (readout chips, sensors) from on place to the other and the processing task that has been performed at different places (e.g. bumping, thinning, wafer probing)
- Detector Configuration database: this keeps track of all the alignment parameters of the pixel modules placement on the substrates, the pixel half stations and the pixel half detectors at different stages of the assembly process
- Detector calibration database: this keeps tracks of the calibration results using radioactive source, laser, and test pulses. Besides keeping a record of bad (dead or noisy) channels, detailed performance parameters such as noise, threshold, and ga in will be recorded for each pixel in the system. All information pertinent to the performance of the detector, such as voltage and current settings, limits, operating temperatures, vacuum conditions will also be kept.

4.8 Performance

4.8.1 Spatial Resolution

BTeV test beam studies, performed with prototype sensors and readout having pixel sizes of 50 μm by 400 μm, have demonstrated a spatial resolution between 5 and 9 μm in the narrow dimension, depending on the track angle of incidence (see Fig. 4.61). The solid line shows the resolution function (Gaussian) used for the Monte Carlo studies presented in the BTeV proposal. (The MC simulations also included non-Gaussian tails in the resolution distributions as measured in the test beam.) The figure shows both the resolution obtained using 8-bit charge information directly, and also the resolution obtained by degrading the pulse height to 2-bits of information. This result confirms the prediction of our simulations: that excellent resolution can be obtained using charge sharing, even with very coarse digitization. Based on these results, it has been decided that the BTeV readout chip will have a 3-bit FADC in each pixel cell. This will provide excellent spatial resolution. In addition, the actual pulse heights may be used to indicate the presence of δ-rays or γ conversions.

The single hit resolution is made possible by the choice of pixel size and a relatively low threshold for readout (approximately 2500 input electrons equivalent compared to about 24000 electrons for a minimum ionizing track at normal incidence for the devices tested). Relatively low dispersion of the thresholds across the chip and low noise in each pixel make

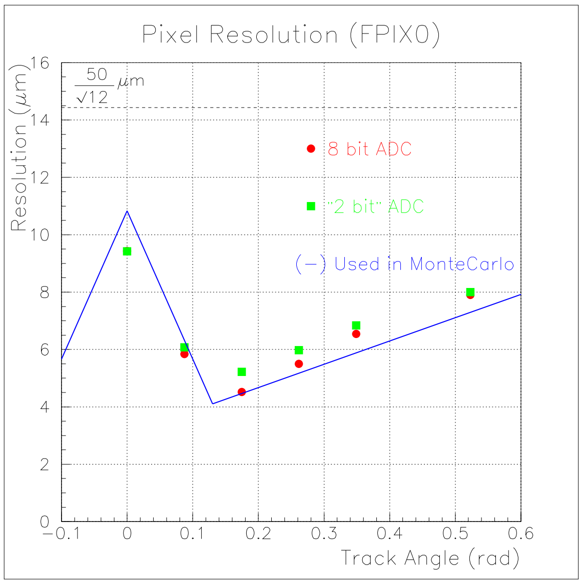

Figure 4.61: Resolution as a function of the angle of the incident beam for both 2-bit and 8-bit ADC readouts. The lines are piecewise linear fits to a simulation of the resolution.

the low readout threshold possible. Given the relatively long beam crossing interval of the Tevatron (compared with the 25ns at LHC), time slewing in the chips will not be a problem. Mounting stability and the necessary pixel alignment, using actual tracks in the final location, will be important to avoid serious degradation of this good resolution.

While single hit resolution is important, it is not the whole story. We have worked to minimize the multiple scattering due to the material in all the components of the system (see Table 4.4). The pixel detector will sit in a vacuum with only a set of wires or a few strips between the beam and the detectors. The very close proximity to the interaction region and the spacing between pixel planes is kept to a minimum to reduce the extrapolation distances to vertices, both primary and secondary. All these parameters have been optimized using detailed (MCFast and GEANT) simulations of our experiment and representative physics measurements.

4.8.2 Pattern Recognition Capability

The early choice of pixel technology for the BTeV vertex detector was based, in part, on the space point information that it provides which will help in pattern recognition. Fig. 4.62 comes from a beam test of BTeV prototype pixel detectors, and shows the power of space points in reconstructing high density tracks. There, an interaction in a carbon target a few mm upstream of the first pixel plane leads to seven tracks reconstructed in much less than 1 cm^2, a density an order of magnitude more than typical for BTeV.

The pattern recognition capability benefits enormously from the low occupancy, averaging slightly above 1 track per B event in the highest rate readout chip. In addition, the stretching

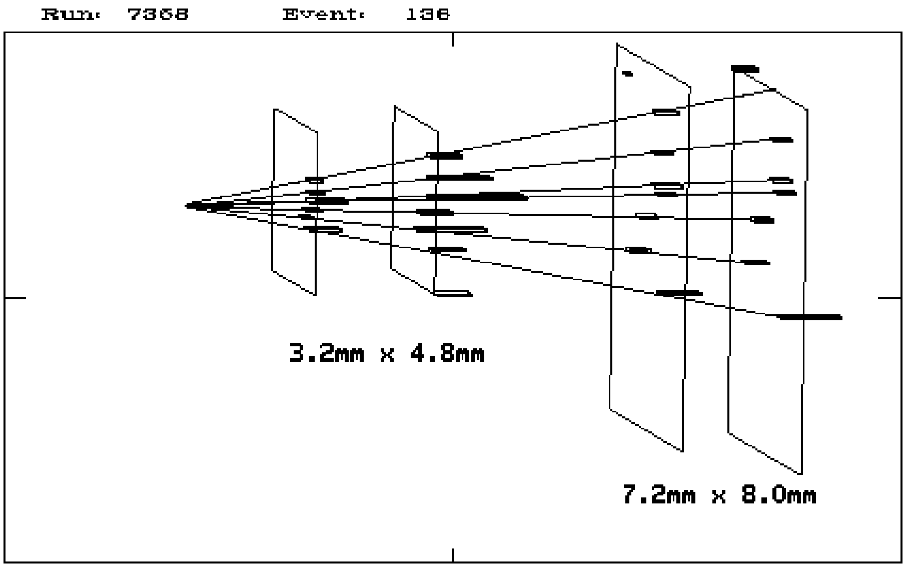

Figure 4.62: Multiparticle interaction observed in Fermilab beam test. The length of each hit is proportional to the pulse height. The straight lines represent fits to the outgoing tracks.

of edge pixels and the overlap of pixel modules mounted on opposite sides of the substrate provide complete coverage within the nominal plane acceptance. The regular spacing of planes along the beam also eases the job of the Level 1 trigger.

4.8.3 Radiation Hardness

We have done a detailed simulation of the expected radiation levels for the whole BTeV detector and the experimental area. The luminosity used in the simulation was 2×10^{32} $\mathrm{cm}^{-2}\ \mathrm{s}^{-1}$. The Pythia generator was used to generate minimum bias events which served as input particles for the MARS code. The full BTeV geometry file was used, including the location and amount of material in the various subsystems of the detectors, the dipole magnet, and the compensating dipoles. The charged hadron fluence distribution in the pixel region is plotted in Fig. 4.63. We have also looked at other particles such as neutrons, gammas, electrons, and muons. In the pixel active region, the fluences due to these latter particles are more than an order of magnitude less than that from the charged hadrons. As one can see from Fig. 4.63, it is expected that the innermost region of the pixel detector will receive a fluence of 1×10^{14} particles/cm^2/year.

The significant radiation environment in which we plan to operate our detector means that all components of the pixel system have to be radiation hard. Our irradiation studies showed that both the sensors and the readout chips are radiation hard enough to remain operational for at least 10 years of BTeV running.

These irradiation results will be augmented with charge collection and other tests in a test

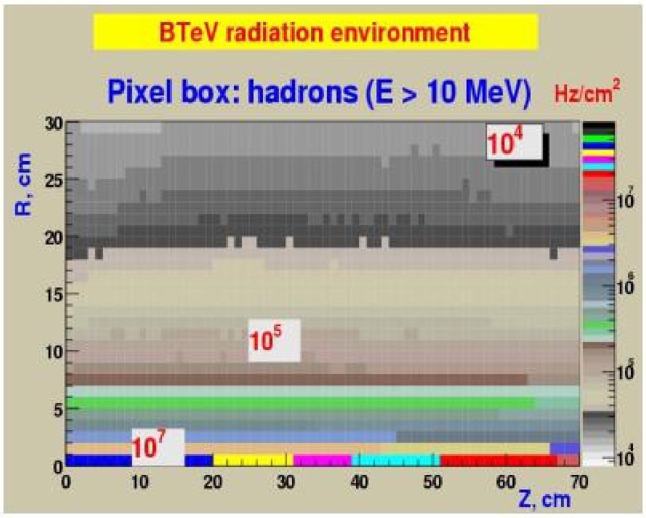

Figure 4.63: Charged particles distribution in the BTeV pixel detector

beam at the Fermilab Meson Test Beam Facility as soon as it is available. Finally, we have started and will continue to test all components (bump bonds, high density interconnects, adhesives, etc.) in high radiation environments before final certification for use in the pixel detector.

4.8.4 Material Thickness

In order to prevent multiple scattering from decreasing the utility of our precision spatial resolution, we are keeping the material budget as low as possible. Table 4.4 lists the various contributions to our material budget within the active area (10×10 cm^2) of the pixel detector. Note that the sensors and readout chips are thinned relative to what is typically used in high-energy physics today. The high-density interconnects have four Cu layers. Signal and power flex-cables are decoupled and the materials in each can be separately optimized. We are currently investigating the use of power cables using Al instead of Cu. For rf shield, we are still investigating the options of using four Al or stainless steel strips, each 5 mm wide by 50 microns thick or a set of Cu/Be wires of 125μm in diameter.

4.8.5 Readout Speed

Our pixel readout is data-driven. That is, the readout occurs as soon as data is ready on the readout chip. The token passing from row to row, which is an important part of the potential readout speed, is very fast (0.125 ns per row), and this starts in parallel in all

Table 4.4: Material budget of a BTeV pixel plane. The column labeled "coverage" shows the factor applied to account for overlaps of the sensors and readout chips, and for geometric coverage (e.g. area covered by bump bonds/total area).

Item	*Thickness(mm)*	$X_0(mm)$	*Coverage*	$X/X_0(\%)$
Sensor	0.25	93.6	1.06	0.28
Readout chip	0.20	93.6	1.27	0.27
Bumps and wire bond	0.02	10.0	0.02	0.004
HDI	0.22	82.45	1.55	0.40
Adhesive	0.10	376	1.41	0.04
Substrate	0.44	191.3	1	0.23
Total				1.22

columns. The readout rate allows us to move all the data off chip with negligible loss of data, even if the amount of data is three times that projected for our nominal luminosity of 2×10^{32} cm^{-2}s^{-1}. Data output is serialized, but uses a number of parallel readout paths selectable for each readout chip. The bandwidth of each serial path is 140 Mbps. The chips located closest to the beam are read out using 6 serial paths (840 Mbps total). Other chips are read out using 1, 2, or 4 serial paths. Most of the readout chips in the pixel system require only 1 serial output path. The readout bandwidth summed over the entire pixel detector is approximately 2 Tbps (terabits per second). The data coming off the chip is already highly sparsified, since only pixels above threshold are read out. Sorting out the data and assembling events is done external to the detector in large buffer memories.

4.8.6 Physics Capability

Figure 4.64 shows the momentum resolution as a function of track momentum using the pixel hits only. Figure 4.65 shows the distribution of L/σ(L), which is the normalized detachment between the primary vertex and the B decay vertex, for reconstructed decays $B_s \to D_s^- K^+$, where, $D_s^- \to \phi\pi^-$ and $\phi \to K^+K^-$. The mean value is 44 standard deviations! Figure 4.66 shows the L-resolution and the proper time resolution for the B_s decay. The resolution in proper time is 46 fs even for this complex multibody decay containing a tertiary vertex (the D_s^- decay). This can be compared with the B_s lifetime of $\sim$1500 fs or the B_s mixing period of $\sim$400 fs if x_s is about 25. It is clear that the BTeV vertex detector has abundant resolution to carry out detailed time-dependent analyses even if the B_s were to have a surprisingly high oscillation frequency.

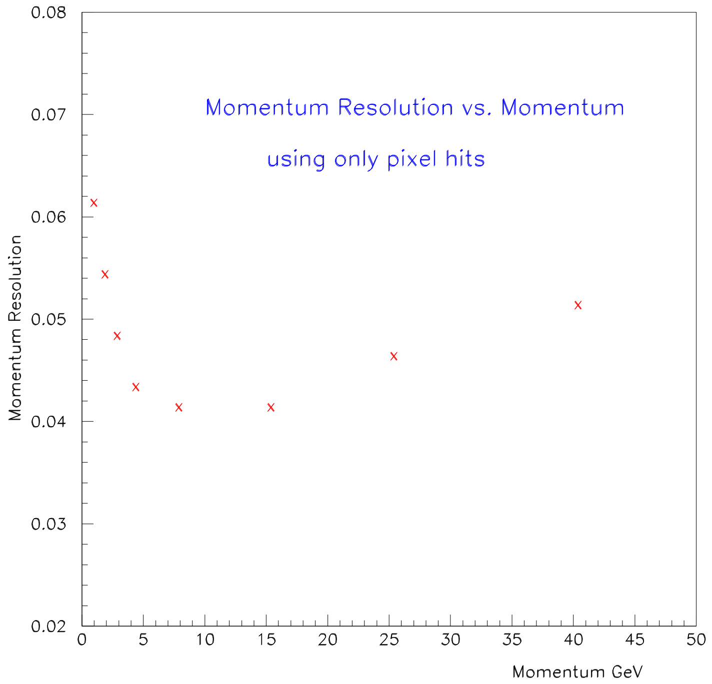

Figure 4.64: Momentum resolution as a function of track momentum using just the pixel hits

4.9 Cost, schedule and Risk analysis

4.9.1 Cost

The construction cost for the pixel detector is estimated to be \$15.5M with a contingency of \$6.2M to give a total cost of \$21.7M. These figures includes fringes and overheads. Most of the estimates are based on budgetary quotes from industry or recent requisitions of prototypes. A few are based on experiences with other projects on similar items (e.q. data cable used by CDF).

4.9.2 Schedule

The overall work schedule covers the whole construction period for the BTeV detector. This is based on a fully resource-loaded schedule. It is planned to ensure that the pixel detector is installed well before the start of the data-taking. A 10% detector is envisaged to be built and tested in CZERO using parts from the preproduction run and will be operational in 2007.

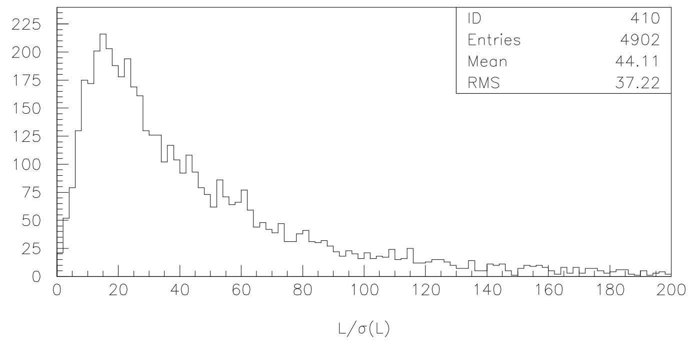

Figure 4.65: Normalized detachment, L/σ(L), between the primary vertex and the decay vertex for the decay $B_s \rightarrow D_s^- K^+$.

4.9.3 Production Risk Analysis

A risk is a situation that has the potential to cause a wanted or unwanted change in the project. Here, we focus on risks to the BTeV pixel detector that are unwanted. Risks can affect the schedule, cost, scope (what the project finally has in it) or technical success of the project.

A measure of the severity of risk is Severity (S) = Probability of occurence (P) $\times$ Impact (I) if it occurs. Following the guidance as outlined in [30], we have done an analysis of the pixel detector and identified the "risk events" as outlined below during the construction phase. Only events that have a Severity above 0.15 are listed. We also give our risk mitigation plan.

Sensor Currently, all vendors that we have contacted are using 4" technology. However, at some future dates, vendors may choose to move from 4" technology to 6" technology. Past experience showed that it would take a long time for the vendors to understand the process and improve the yield. The potential impact is on the schedule because the vendor may take a long while to ramp up the production capacity. We assign a severity factor of 0.15 to this based on a probability of 0.3 and an impact of 0.5. Our mitigation plan is to work with multiple vendors and keep in close contact with vendors to understand their future plans.

Bump bonding Our current bump bonding vendors may not be available to us in the future or have unacceptable yield. Since we need more or less state-of-the-art technology for this, there is not a lot of experience for the vendors with large scale production (P=0.5). The impact of this will be high (0.8) as it will lead to severe cost increase and project slippage.

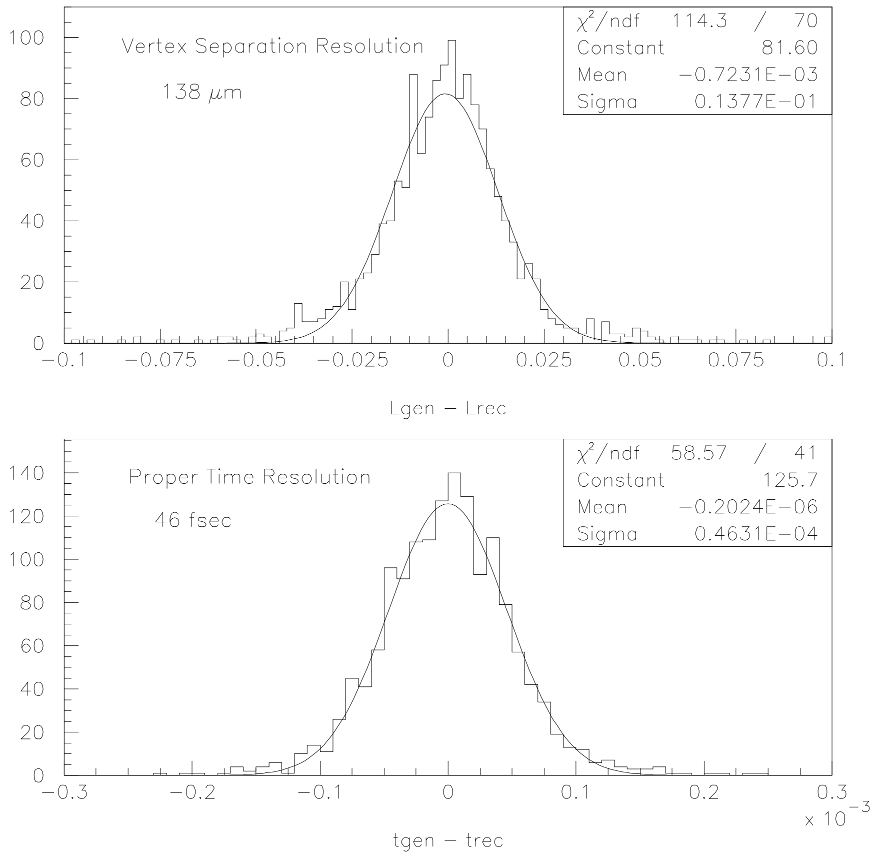

Figure 4.66: Top) The resolution in L, the separation between the primary and secondary vertex. The quantity plotted is the difference between the Monte Carlo generated separation L_{gen} and the reconstructed separation L_{rec}, for the $B_s \to D_s^- K^+$ decay. The X- axis is in cm. The L resolution is 138 μm; and bottom) resolution in proper time. The quantity plotted is the Monte Carlo generated proper time t_{gen} minus the reconstructed proper time, t_{rec} of the B_s decay. The X-axis is picoseconds (10^{-3} nanoseconds). The proper time resolution is 46 fs.

Our plan is to identify more vendors and to keep close contact with ALICE, ATLAS, and CMS about their schedules and vendors.

Readout chip The pixel readout chip is based on a 0.25 μm CMOS process. Since the trend in industry is a move towards processes with finer features, there is a probability (0.25) that the process would disappear before we go into production. The impact will be high

(0.8) as it will mean re-design of the chip using a different process. The best solution is to start production as soon as funding is available.

HDI The risk (0.3) is that none of the vendors can produce the multi-layer flex cables with acceptable yield; or the couple of vendors are too busy with orders from other HEP experiments. While minimal technical problems are expected, we do not know what the yield of large scale production will be. The impact (I=0.5) will be high as it will lead to overall project slippage and increase in cost. We need to identify other vendors and keep abreast with all the developments in electronic packaging. We have to follow the industrial trend but not lead it.

TPG substrate TPG substrate is a quite fragile material and has a very poor tensile strength and a very low elastic limit in the out of plane direction. Any excessive loads that come from improper handling, installation (like gluing pressure of module on TPG), or operation (thermal stresses due to thermal gradient and CTE mismatch) can make the TPG substrate yield or deform permanently. Probability of failure is moderate (0.3), and the impact factor is high(0.5). The best mitigations are to develop proper procedures to handle the TPG with great care, to conduct more tests to understand its behavior so that undesirable stresses will not be generated, and to go through a series of real module placement as early as possible to expose any troubles. We have recently made good progress on the encapsulation which has addressed a lot of the handling issues and concerns.

4.9.4 Operation Risk Analysis

The mechanical system of the BTeV pixel detector is a very complicated system which must be integrated to the Tevatron machine vacuum without excessive risk. We have carried out a preliminary risk analysis to address failure scenarios, and to provide a basis for further discussion and any design modifications that may be necessary. A number of precautionary measures to mitigate these risks have been looked into and these have been included in the baseline design of the BTeV pixel system.

The critical parts of the system which have been analysed include the vacuum, cooling, rf shield, actuators, and the magnet. The detailed risk analysis is presented in [29]. This preliminary analysis will be developed further as the project progresses to the construction phase. By working together with the relevant department at Fermilab and learn from the experience of CDF and D0, most of these failure scenarios could be mitigated. As an example, we will work together with the Acceleration Integration Department to understand machine-related radiation loads for beam accidents and also to study impact of BTeV operation on the machine. It should be borne in mind, however, that since the pixel detector is placed inside a vacuum vessel which in turn will be located inside the analysis magnet, it will be hard to access should any problem occur. Routine maintenance or repairing of the detector elements that are placed inside the vessel *in-situ* will not be possible. To remove the vessel out of the magnet for repair will require a downtime of the machine for at least one month.

This implies a robust system with minimum and long time in between maintenances. We have designed our system with this condition imposed as a boundary condition.

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