Model-Based Fault Detection and Identification for Power Electronics Systems

Jason Poon

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2015-238
http://www.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-238.html

December 15, 2015

Model-Based Fault Detection and Identification for Power Electronics Systems

by Jason Poon

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

Committee:

Seth R. Sanders
Research Advisor

Date

* * * * * *

Costas Spanos
Second Reader

Date

Model-Based Fault Detection and Identification for Power Electronics Systems

Abstract

Model-Based Fault Detection and Identification for Power Electronics Systems

by

Jason Poon

Master of Science in Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Seth R. Sanders, Chair

We present the analysis, design, and experimental implementation of a model-based fault detection and identification (FDI) method for switching power converters based on a linear-switched modeling approach. The proposed FDI approach is general in that it can be used to detect and identify arbitrary faults in components, sensors, and inputs in a broad class of switching power converters. More importantly, the modeling and implementation of the proposed FDI approach is flexible for both the converter topology and faults of interest; that is, one would require minimal effort to reconfigure an existing FDI implementation for a different converter topology or fault type. We show that the use of a linear-switched model, while introducing complexities in terms of modeling and real-time implementation, offer advantages over model-based FDI methods that rely on an averaged small signal model. Moreover, we show that the proposed FDI method can be integrated with the existing control system of the switching power converter, that is, no additional electrical or computation hardware is required. In essence, the FDI method enables a layer of intelligence on top of existing hardware protection such as fuses and circuit breakers.

In this thesis, we present experimental implementations and results for three different converter topologies, ranging from distributed AC grid-connected systems to distributed DC networked systems. The field-programmable gate array (FPGA) implementation enables fast fault detection and fault identification with speed on the order of application-specific implementations in literature, but with the advantage of being converter- and fault-agnostic in terms of modeling and implementation.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 The emergence of safety-critical power electronics systems

The reliability of power electronics systems is critically important in many applications; ranging from safety- and mission-critical systems in aerospace, automotive, ship and train propulsion; to information technology and communication systems, industrial automation, and converters for voltage and power flow control in electrical networks.

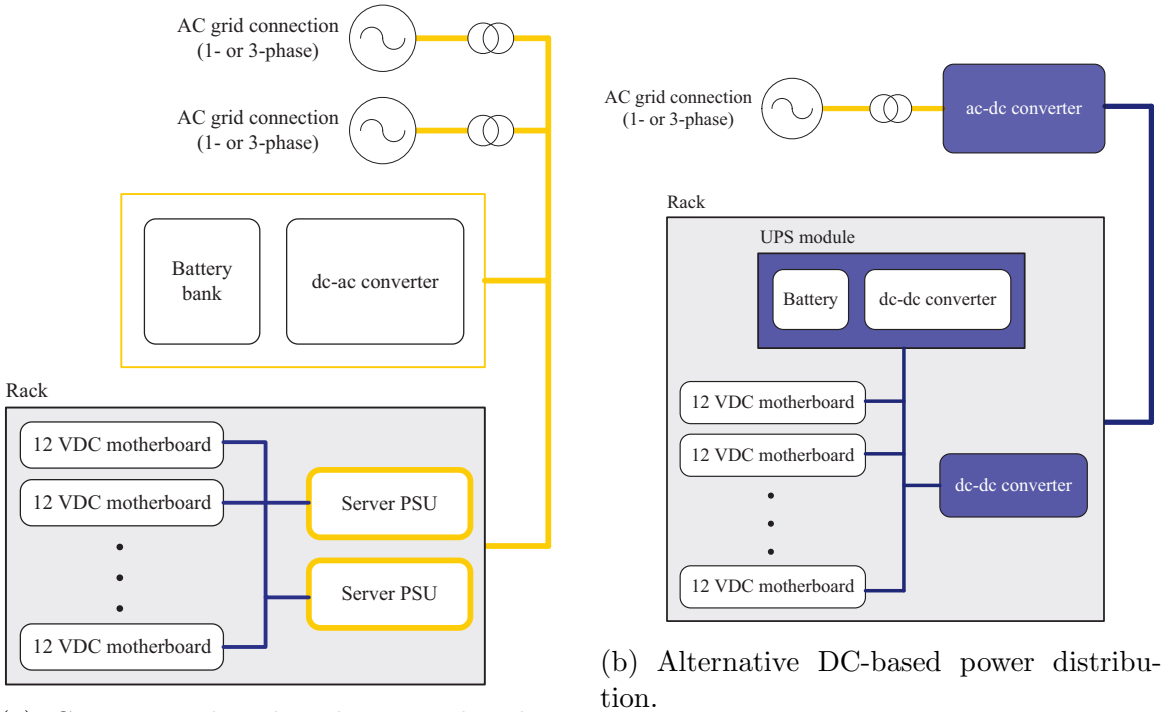
In general, in any engineered system, ensuring a high-level of reliability is usually achieved by incorporating mechanisms for *fault tolerance* into the system design. Fault tolerance is the ability of a system to adapt and compensate, in a systematic way, to random component, sensor, or input faults, while providing completely or partially its intended functionality [18]. There are three key elements to any fault-tolerant system design–component redundancy, a fault detection and identification system, and a remediation or reconfiguration system that, once a fault has been detected and identified, substitutes the faulty component with a redundant one, or reconfigures the control to compensate for the fault.

Here, we will discuss four technologies that fundamentally rely on one or multiple safety-critical power electronics systems, characterized by the need for high reliability, minimal down-time, and high fault tolerance and reconfigurability.

Data center power distribution networks

Data centers around the world enable an abundance of cloud and information technology services. In recent years, demand for these types of services has grown tremendously; in 2010, data centers accounted for 1.3 percent of the entire global energy usage [17].

The reliability and fault tolerance of the power distribution in a data center is an utmost priority and often takes precedence over other design choices such as cost or energy efficiency. Many data centers achieve this reliability by redundancy and over-provisioning, as shown in



(a) Conventional ac-based power distribution.

(b) Alternative DC-based power distribution.

Figure 1.1: Architectures for power distribution in a data center.

Fig. 1.1a. The drawback of this design is under-utilization of the infrastructure and excessive energy required to power redundant components.

In recent years, there have been renewed efforts towards realizing more efficient and less redundant data center power distribution systems, while still maintaining high reliability and fault tolerance. Fig. 1.1b shows an alternative DC-based power distribution network for a data center. In general, a DC-based design can be less redundant, and can achieve similar levels of fault tolerance by the addition of power electronics converters at the rack-level.

A DC microgrid architecture for rural electrification

There are currently 1.3 billion people in rural developing regions without access to electricity [10]. This number is projected to increase despite increased grid-tied generation since there is still a significant power deficit in urban areas [10, 35, 27]. Microgrids have been viewed as a viable option to provide electricity for rural areas where the cost of grid extension is prohibitive [9, 20]. In recent years, the falling cost of solar energy has sparked increasing interest in developing renewable methods for rural electrification [5, 34, 22]. However, battery costs have not declined at the same rate as solar photovoltaic (PV) panels. Since the predominant residential usage is during night-time hours [33], the cost of stored electricity

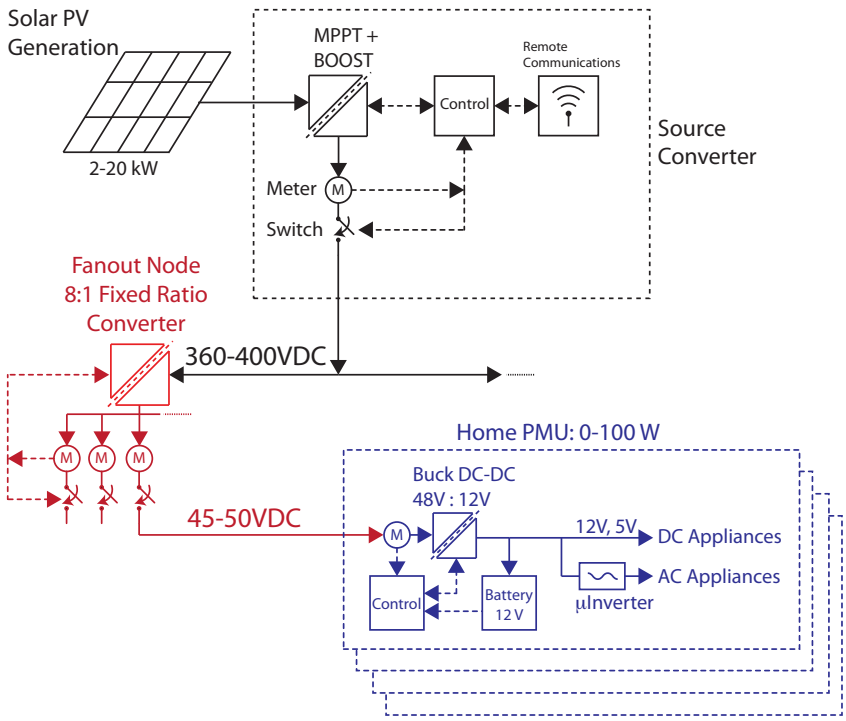
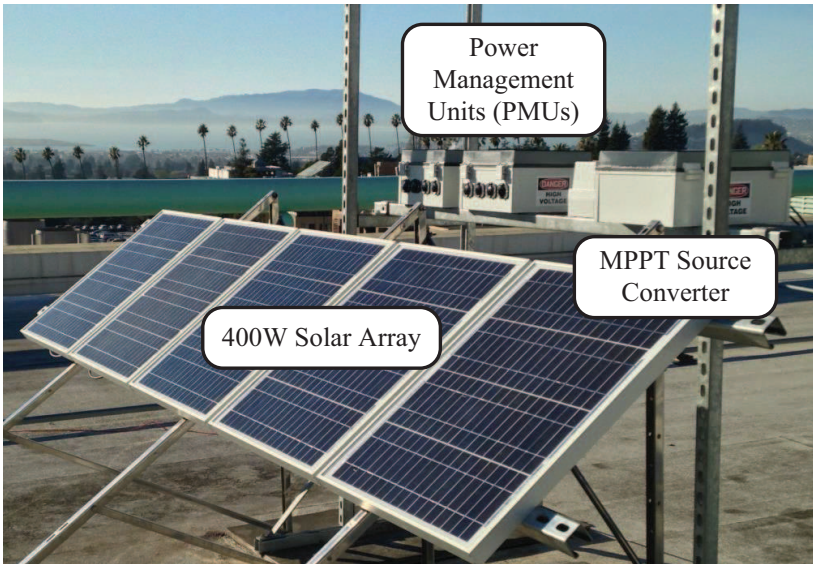


Figure 1.2: An architectural overview of a proposed DC microgrid system in [23].

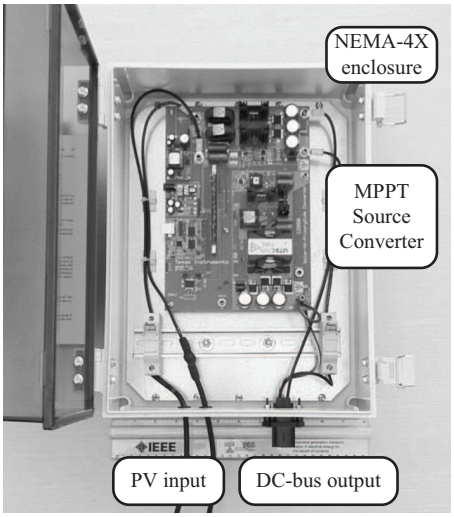
use is a key figure of merit. In this regard, DC microgrids have demonstrated promise as a viable method of enabling improved efficiency and scalability for off-grid systems [22, 33, 6, 13, 41, 40].

In [23], the authors demonstrate a DC microgrid architecture that provides a scalable solution for rural electrification. An overview of the DC microgrid architecture is shown in Fig. 1.2. The key components of the system are 1) the maximum power point tracking (MPPT) *source converter*, 2) the *fanout nodes*, and 3) the *household power management units (PMUs)*. The converter designs and enclosures are shown in Fig. 1.3. The MPPT source converter (Fig. 1.3b) consists of a 2-phase interleaved boost converter, fuse protection, and connectors for PV input and bus output. The fanout node is implemented using a commercially available 8:1 fixed ratio 300 W DC converter which converts from 360-400 V to 45-50 V. The household PMU (Fig. 1.3c) consists of a 100 W synchronous buck converter, fuse protection, 100 W-hrs of battery storage, and connectors for 45-50 V bus input and 12 V DC output.

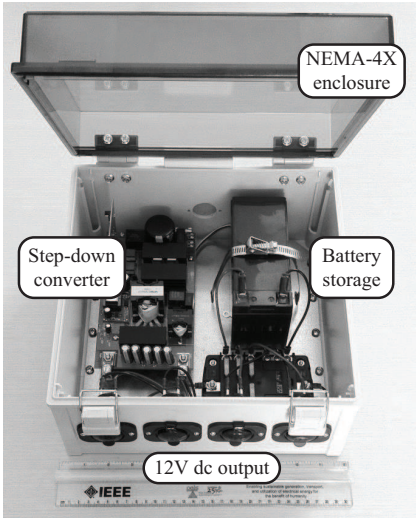
There are two key elements which motivate the need for fault tolerance in the proposed DC microgrid architecture. First, the architecture relies on intermittent energy sources, with no grid connection, and thus, reliability and fault tolerance are crucial in order to maintain grid uptime and to power critical loads. Moreover, the increased number of power electronics in the architecture, at both the distribution and household level, introduce additional points of failure that require additional robustness and resiliency.



(a) A scaled-down DC microgrid prototype.



(b) MPPT source converter.



(c) Power management unit (PMU).

Figure 1.3: Photographs of DC microgrid prototype setup and components from [23].

Grid-connected AC-DC converters for ancillary services

The proliferation of grid-connected storage and renewable resources, such as batteries, mechanical flywheels, photovoltaics, and wind, have introduced a large number of highly uncertain and intermittent energy sources and loads in the grid. Power electronics converters are essential for enabling the integration of these devices by providing grid ancillary services such as last-mile voltage regulation, power factor correction, and harmonic mitigation.

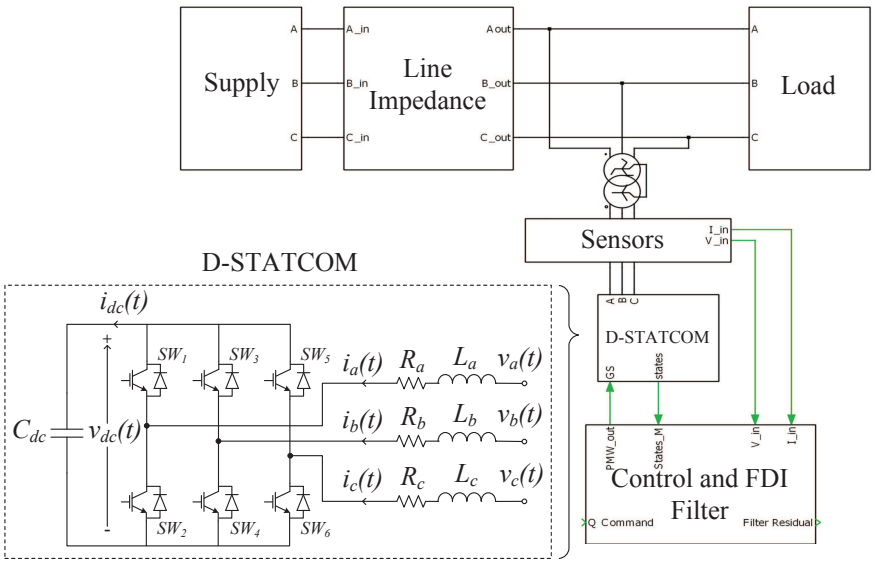


Figure 1.4: A D-STATCOM converter topology.

One example of such a converter is a distributed static compensator (D-STATCOM). A D-STATCOM is a distribution-level converter that is often tied to highly nonlinear loads to reduce their disturbance to the grid, or to loads that require very strict power quality control [26, 31]. The most basic D-STATCOM consists of a voltage source converter tied to a capacitor on the DC end, and tied to a filter on the ac end, as shown in Fig. 1.4.

Next-generation smart building nanogrids

Commercial buildings consume nearly one-fifth of the primary energy in the United States. In recent years, the concept of a 'smart building' has emerged as an important academic and industrial effort towards realizing significant improvements in building efficiency, comfort, and intelligence. Integral to the concept of a smart building is its power distribution network, which can be viewed as a nanogrid, as shown in Fig. 1.5. As opposed to buildings that purely consume energy, these nanogrids can contain on-site energy resources, such as rooftop photovoltaics or wind turbines. Energy storage buffers, such as batteries or mechanical flywheels, store excess generated energy, which can be used for building power or to provide grid services to the utility. Moreover, electrical loads can be scheduled based on dynamic energy pricing, enabling demand response. Indeed, smart building nanogrids introduce a new paradigm of how buildings consume, generate, and store energy.

However, the confluence of power electronics systems and buildings in these nanogrids has introduced new challenges, particularly with respect to reliability and fault tolerance. Switching power converters introduce new failure points in a power distribution network. Additionally, the interaction between converters and the propagation or cascade effect of faults through a nanogrid remain open research questions.

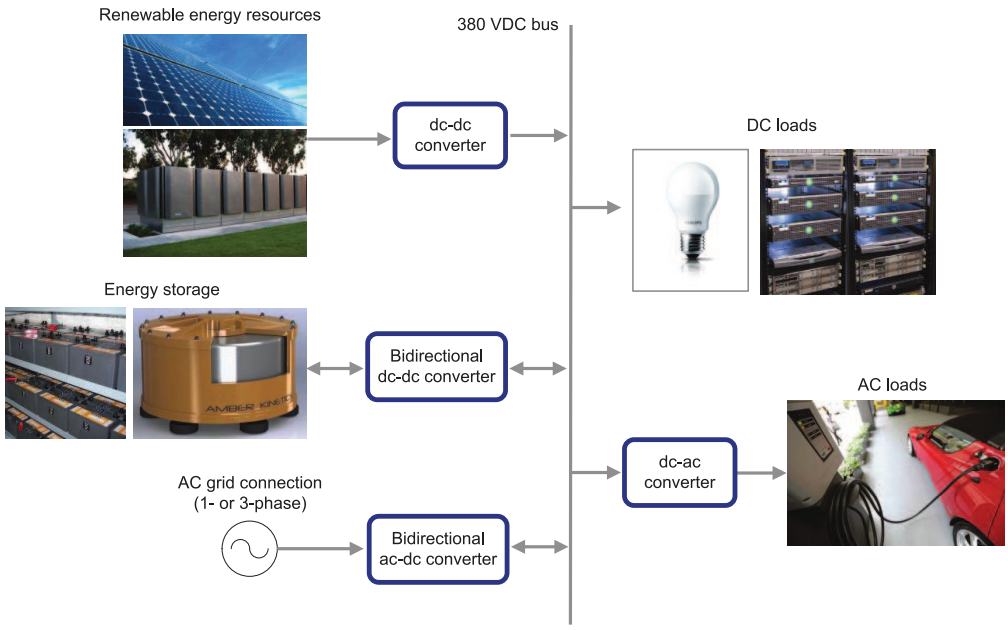


Figure 1.5: A prototype nanogrid for power distribution in a smart building.

1.2 Motivation for fault tolerance

Fault tolerance is an essential property that needs to be built into the safety-critical power electronics systems. At the converter-level, there are three classes of faults that can occur: (1) component faults, (2) sensor faults, and (3) input or actuator faults.

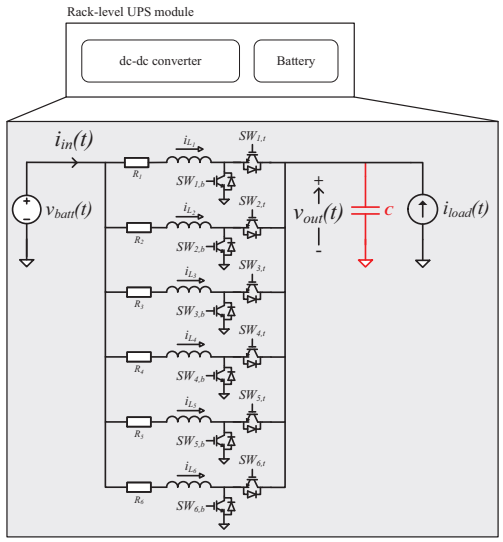
Here, we will explain and motivate the need for fault tolerance at the level of single switching power converter by considering specific faults in a data center rack-level uninterruptable power supply (UPS) module. The topology of the UPS module is a 6-phase interleaved boost converter.

Component fault

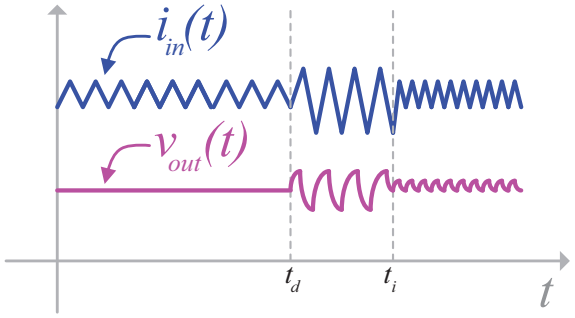
Consider a degraded capacitor C in the converter shown in Fig. 1.6a that reduces the effective capacitance at the output of the converter. The effect of this fault will result in an increase the ripple in both the input current and output voltage waveforms, as shown in the sketch in Fig. 1.6b.

A fault tolerant converter should:

1. Detect and identify the change in capacitance C, and
2. If appropriate, remediate the fault by reconfiguring the converter control (e.g. by increasing switching frequency), which will enable operation in degraded state.



(a) Rack-level UPS module converter topology with a component fault in C.



(b) Sketch of input current and output voltage waveforms. Time of fault detection t_d and time of fault identification t_i are shown.

Figure 1.6: Component fault in C.

3. If appropriate, automatically take the converter offline, and re-route power through parallel path converters.

Sensor fault

Consider a fault in the output voltage sensor in the converter shown in Fig. 1.7a. The effect of this fault will cause the measured output voltage to be zero, while the actual converter state remains unchanged, as shown in Fig 1.7b.

A fault tolerant converter should:

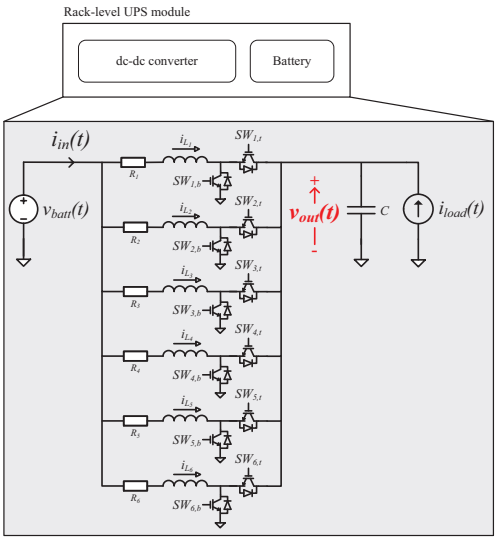
1. Detect and identify the voltage sensor fault,
2. Enable continued operation by using an estimate value for the output voltage $\hat{v}_{out}$, and
3. Notify an operator for sensor or converter replacement.

Input (actuator) fault

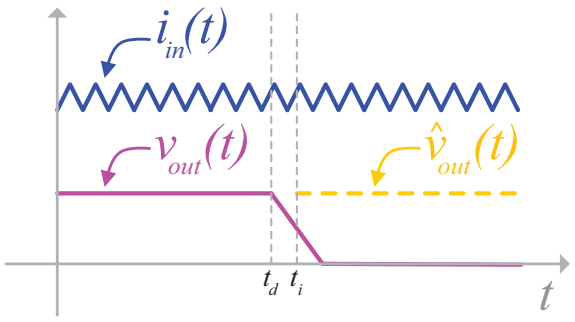
Consider a hard switch failure to short in $SW_{3,b}$ in the converter shown in Fig. 1.8a. The effect of this fault will cause a large spike in current, and force the input current and output voltage waveforms to zerpo, as shown in the sketch in Fig. 1.8b.

A fault tolerant converter should:

1. Detect and identify the hard switch failure in $SW_{3,b}$,



(a) Rack-level UPS module converter topology with a sensor fault in the output voltage sensor.



(b) Sketch of input current and output voltage waveforms. Time of fault detection t_d and time of fault identification t_i are shown.

Figure 1.7: Sensor fault in the output voltage sensor.

2. Take action to isolate converter from system (e.g. by stopping PWM signals and actuating external contactors), and

3. Notify an operator for converter replacement.

1.3 Requirements for fault detection and identification

As mentioned in the preceding section, fault tolerance can be achieved through some combination of the following:

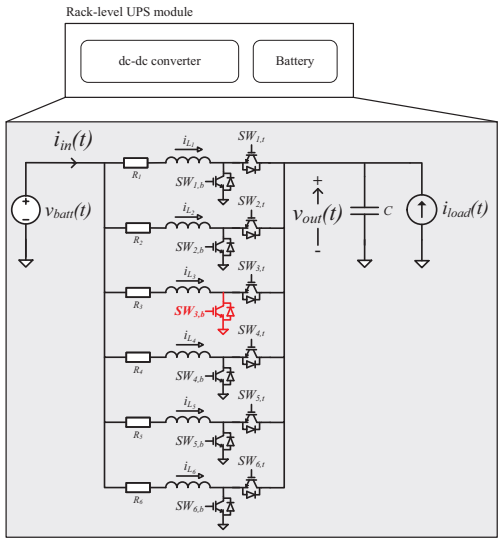
1. Component redundancy,

2. A fault detection and identification (FDI) system, and

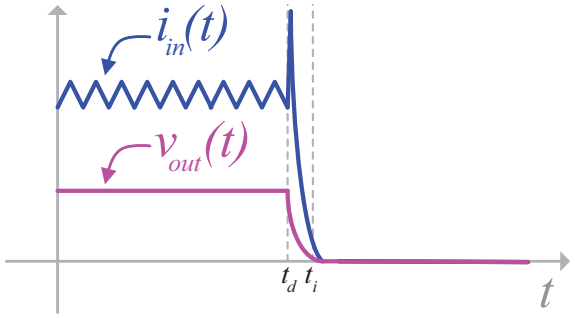
3. A remediation system.

Many traditional approaches to fault tolerance have focused on component redundancy. However, this typically results in systems with (1) increased cost, (2) increased system complexity, and (3) increased energy losses due to device under-utilization.

The question then becomes—how can we achieve fault tolerance while minimizing the amount of component redundancy in a system?



(a) Rack-level UPS module converter topology with an input fault in $SW_{3,b}$.



(b) Sketch of input current and output voltage waveforms. Time of fault detection t_d and time of fault identification t_i are shown.

Figure 1.8: Input fault in $SW_{3,b}$.

One approach—the approach explored in this thesis—is to improve the fault detection identification system.

An FDI system (see, e.g., [28]) executes two tasks: (1) detection, which makes a binary decision whether or not a fault has occurred, and (2) identification, which determines the location of the faulty component. Methods for FDI in power electronics applications can be broadly classified into three different classes: i) model-based, uses knowledge of the system model (including the effect of faults) to design residual generators that can point to specific faults (see, e.g., [39, 19, 29, 38, 4]); ii) artificial intelligence-based, uses neural networks and fuzzy logic to develop expert systems that once trained can point to specific faults (see, e.g., [1, 16, 1]); and iii) signal processing-based, uses spectral analysis to identify unique fault signatures (see, e.g., [7, 37]).

In power electronics systems, the dynamic time constants are typically much faster than most aerospace and industrial systems for which the majority of FDI literature focuses on. Moreover, in general, fault detection and identification should occur within one or two switching cycles of the fault occurrence. This creates computational challenges, particularly for artificial intelligence-based and signal processing-based approaches, which can require significant computational resources, particularly for real-time implementations.

1.4 Summary of results

The salient contributions of this thesis are as follows:

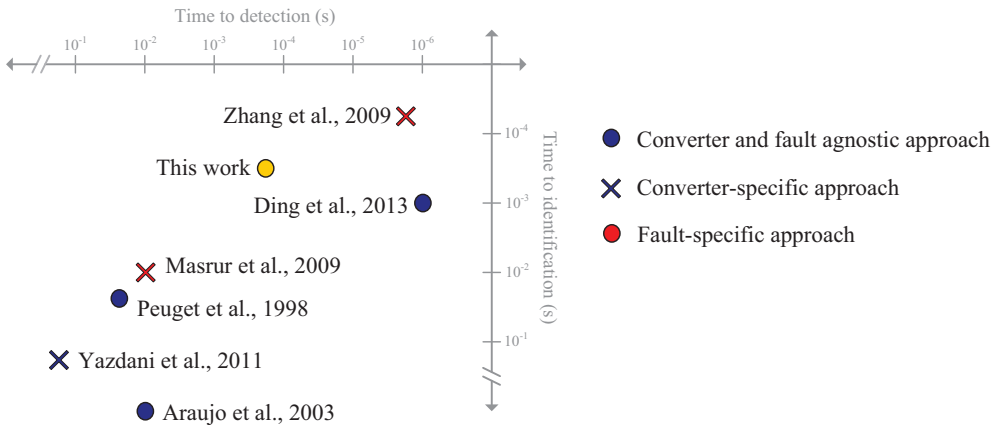


Figure 1.9: A comparison of the speed and flexibility of the proposed FDI approach with existing approaches discussed in literature.

1. We present a model-based fault detection and identification method for switching power converters based on a linear-switched modeling approach. We show that the use of a linear-switched model, while introducing complexities in terms of modeling and real-time implementation, offers advantages over model-based FDI methods that rely on an averaged small signal model.

2. The proposed FDI approach is general in that it can be used to detect and identify arbitrary faults in components, sensors, and inputs in a broad class of switching power converters. More importantly, the modeling and implementation of the proposed FDI approach is flexible for both the converter topology and faults of interest; that is, one would require minimal effort to reconfigure an existing FDI implementation for a different converter topology or fault type.

3. The field-programmable gate array (FPGA) based implementation enables fast fault detection and fault identification. Fig. 1.9 shows a comparison of the speed and flexibility of the proposed FDI approach with existing approaches discussed in literature. Indeed, our experimental results indicate the proposed FDI approach demonstrates speed on the order of application-specific implementations in literature, but the modeling and implementation is converter and fault agnostic.

4. We present experimental implementation and results for three different converter topologies, ranging from distributed AC grid-connected systems to distributed DC networked systems.

5. Finally, we show that the proposed FDI method can be integrated with an existing control system of the switching power converter, that is, no additional electrical or computation hardware is required in order to implement this FDI. In essence, the FDI

method enables a layer of intelligence on top of existing hardware protection such as fuses and circuit breakers.

1.5 Thesis plan

The remainder of the thesis is organized as follows. Chapter 2 presents the proposed methodology for fault detection and identification. We discuss the modeling approach, and also the design and implementation of the fault detection logic and the fault identification logic. Chapter 3 presents an experimental implementation and verification of the proposed FDI approach for a class of distributed AC grid-connected systems. Specifically, we consider (1) a three-phase inverter with an RL load, and (2) a distributed static compensator (D-STATCOM). Chapter 4 presents an experimental implementation and verification for a class of distributed DC networked systems. Specifically, we present a case study for a rack-level UPS DC-DC converter in a data center DC power distribution network. Chapter 5 concludes the thesis by comparing the performance of this work with other approaches in literature. Moreover, we propose opportunities for future work and research directions.

Chapter 2

Methodology

In this chapter, we will discuss the proposed methodology for fault detection and identification. We present the design and implementation of the real-time model based estimator, the fault detection logic, fault signature library, and the fault identification logic. The methodology (and results, thereafter) presented in this thesis extends and unifies the author's previous work in [8] and [30].

2.1 Overview of approach to fault detection and identification

The basic principles of operation for fault detection and identification method are illustrated in Fig. 2.1. Moreover, the testbed used to experimentally demonstrate the proposed methodology is shown in Fig. 2.2. Fundamentally, the FDI system accepts the same input $u(t)$ as the converter (e.g. PWM signals, input voltages, load currents) and outputs (1) a binary decision dependent upon whether a fault has occurred, and (2) if a fault has occurred, an index that identifies the particular fault from a fault signature library.

As shown in Fig. 2.1, there are four distinct stages of the proposed FDI methodology:

1. Real-time model-based estimator
2. Fault detection logic
3. Fault signature library
4. Fault identification logic

First, given a switching power converter, we construct a ***real-time model-based estimation*** that captures the large-signal dynamics of the converter.

The ***fault detection logic*** consists of a model-based estimator or observer for the switching power converter, which generates an error residual vector of the difference between the measured outputs of the converter and the estimated outputs.

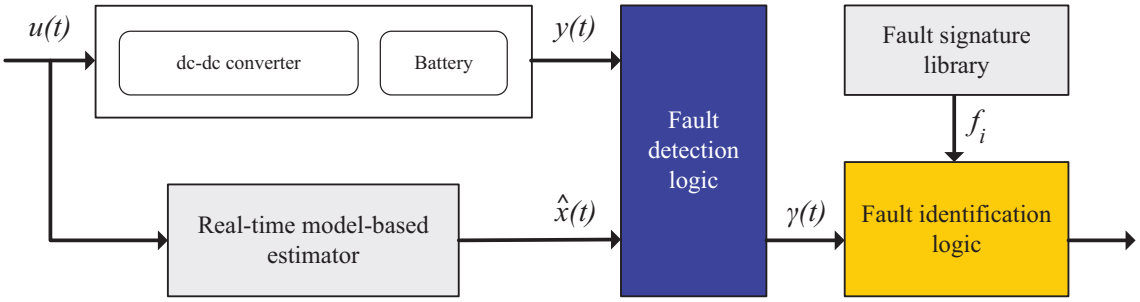


Figure 2.1: A block diagram of the proposed methodology for fault detection and identification.

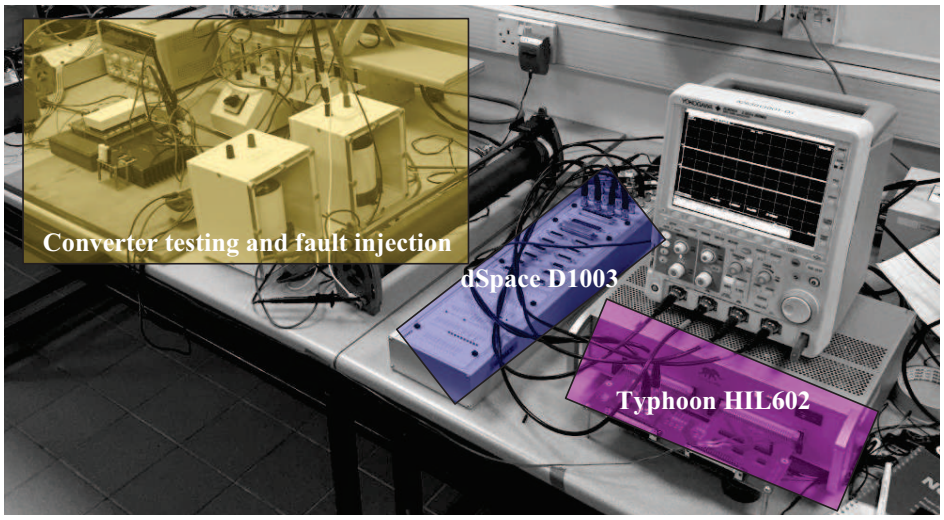


Figure 2.2: A photograph of the testbed used to experimentally demonstrate the proposed methodology for fault detection and identification.

Next, we identify faults of interest in the components and sensors. The dynamics of each of these faults can be uniquely modeled by a scalar *fault magnitude function* and a vector *fault signature*, and are collected in the ***fault signature library***.

In the presence of a particular fault, the error residual will evolve according to the dynamics of the fault magnitude function and fault signature. Since these dynamics are calculated a priori, the ***fault identification logic*** can identify the fault by computing the sliding window L^2-inner product between the error residual vector and the set of fault signatures.

In the subsequent sections, we will discuss the design and implementation of each of these four stages.

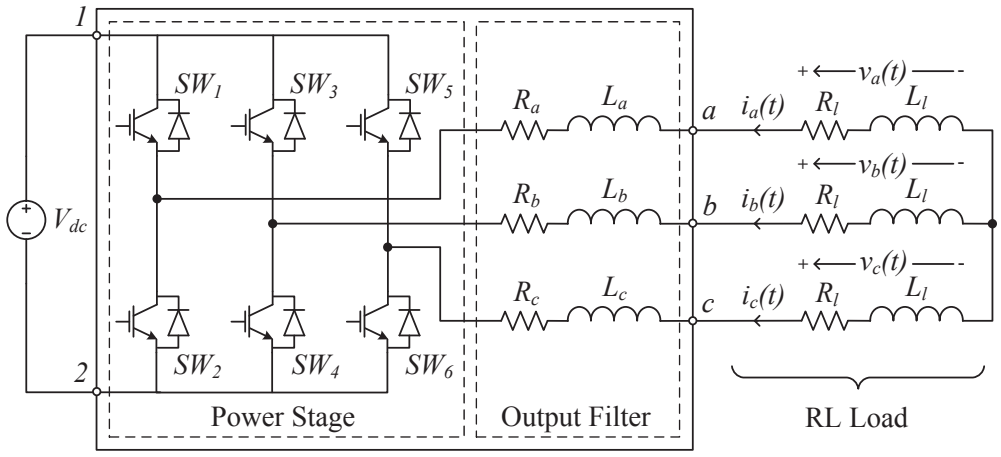


Figure 2.3: Inverter with RL load system.

2.2 Real-time model based estimator

In this section, we develop the linear-switched system modeling framework adopted throughout the thesis and introduce relevant notation and terminology. In order to build the intuition behind the ideas put forward, we start off with the three-phase AC-DC power electronics system in Fig. 2.3. Then, we generalize the framework to a larger class of switching power electronics converters.

Motivation for linear-switched modeling approach

In power electronics systems, which are fundamentally non-linear and time-varying, it is common to use small-signal (linearized) average system models to design the controls (see, e.g., [15, 24]). The use of linearized average models together with observer-based linear filters appears to be a feasible solution to tackle the FDI problem in power electronics; however, linearized average models cannot properly capture the effect of a fault on the systems dynamics. This can be easily illustrated in a simple buck converter when there is a fault that causes a change in the capacitance value of the output filter capacitor [19]. While this fault causes an increase in the output voltage ripple that could degrade system performance, this ripple does not manifest in the standard averaged model; therefore a linear FDI filter that relies on the standard averaged model cannot detect the presence of this fault. To overcome the limitations of linearized averaged models when designing FDI filters for power electronics systems, we use a large-signal model of the system; specifically a linear-switched state-space model to develop a piecewise linear FDI filter with a similar structure to that of a piecewise linear observer [2].

Table 2.1: Possible open/close switch positions for the converter in Fig. 2.3: $s_i = 1$ ($\overline{s}_i = 1 - s_i = 0$) if SW_i is closed and $s_i = 0$ ($\overline{s}_i = 1 - s_i = 1$) if SW_i is open

p	1	2	3	4	5	6	7	8
$s_1/\overline{s}_2$	0	0	0	0	1	1	1	1
$s_3/\overline{s}_4$	0	0	1	1	0	0	1	1
$s_5/\overline{s}_6$	0	1	0	1	0	1	0	1

Three-Phase Inverter with RL Load

Consider the three-phase AC-DC power electronics system in Fig. 2.3, comprised of i) a power stage, and ii) an output filter. The DC voltage source and the RL load, although interconnected to both ends of the system, are not considered part of it, i.e., they are what we refer to as *external elements*.

The large-signal dynamics of this AC-DC power electronics system can be accurately represented by *switched system*[*] modeling formalisms.

In particular, a switched system can be described by a collection of continuous time state-space models—referred to as *modes*—together with a *switching signal*,[†] the role of which is to specify, at each time instant, the active mode [21]. In the system of Fig. 2.3, each mode can be obtained by applying Kirchhoff's laws to each of the circuits that results from the possible open/closed switch combinations. The switching signal is defined by the specifics of the control system that determines the switch open/close positions.

Nominal (Pre-Fault) System Model

For the system of Fig. 2.3, there are six switches, which means that there are 64 possible combinations; however, during normal operation, on each phase, there is exactly one switch closed at any given time, which results in only eight feasible modes. Let $\mathcal{P} = \{1, 2, \ldots, 8\}$ be the set indexing the feasible modes, and let s_i, $i = 1, 2, \ldots, 6$, denote an indicator variable that, at time t, takes value 0 whenever switch i (denoted by SW_i) is open, and value 1 whenever it is closed. Then, as defined in Table 2.1, each $p \in \mathcal{P}$ is uniquely defined by an open/closed switch combination $\{s_1, s_2, \ldots, s_6\}$; therefore, the active mode at time t can be indicated by a function $\sigma : [0, \infty) \to \mathcal{P}$ (the switching signal). Now, by defining $x(t) = [i_a(t), i_b(t), i_c(t)]^T$ and $u(t) = [V_{dc}, v_a(t), v_b(t), v_c(t)]^T$, the system dynamics can be

[*] A dynamical system that can be described by the interaction of some continuous and discrete dynamic behavior is referred to as a *hybrid system*. A *switched system* is a continuous-time system with (isolated) discrete switching events. A switched system can be obtained from a hybrid system by neglecting the details of the discrete behavior [21].

[†] A switching signal is a piecewise constant function with a finite number of discontinuities—the *switching times*—on every bounded time interval, taking a constant value on every interval between two consecutive switching times.

described by a linear-switched state-space model of the form

$$E_{\sigma(t)}\frac{dx(t)}{dt} = F_{\sigma(t)}x(t) + G_{\sigma(t)}u(t), \tag{2.1}$$

with

$$E_{\sigma(t)} = \begin{bmatrix} L_a & -L_b & 0 \\ 0 & L_b & -L_c \\ 1 & 1 & 1 \end{bmatrix},$$

$$F_{\sigma(t)} = \begin{bmatrix} -R_a & R_b & 0 \\ 0 & -R_b & R_c \\ 0 & 0 & 0 \end{bmatrix},$$

$$G_{\sigma(t)} = \begin{bmatrix} -\frac{(s_1-s_2)-(s_3-s_4)}{2} & 1 & -1 & 0 \\ -\frac{(s_3-s_4)-(s_5-s_6)}{2} & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

To complete the above description, we can add

$$y(t) = Hx(t), \tag{2.2}$$

$$z(t) = Du(t), \tag{2.3}$$

where H is a full-rank matrix describing the states (or linear combinations thereof), the measurements of which are available; and D is a full-rank matrix relating the actual value of the system inputs $u(t)$ and the available measurements $z(t)$. The observation equation in (2.2) describes the state measurements available for feedback control, while (2.3) describes the state measurements available for feedforward control; both sets of measurements are key in our FDI filters.

In (2.1), we multiply on both sides by $E^{-1}_{\sigma(t)}$ to obtain:

$$\frac{dx(t)}{dt} = A_{\sigma(t)}x(t) + B_{\sigma(t)}u(t), \tag{2.4}$$

where $A_{\sigma(t)} = E^{-1}_{\sigma(t)}F_{\sigma(t)}$ and $B_{\sigma(t)} = E^{-1}_{\sigma(t)}G_{\sigma(t)}$. In order to ease the notation in subsequent developments, and without loss of generality, we assume that the three phases are symmetric and identical, i.e., $L_a = L_b = L_c = L$, and $R_a = R_b = R_c = R$. Then, the resulting matrices $A_{\sigma(t)}$ and $B_{\sigma(t)}$ are

$$A_{\sigma(t)} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix},$$

$$B_{\sigma(t)} = \begin{bmatrix} k_1(t) & \frac{2}{3L} & -\frac{1}{3L} & -\frac{1}{3L} \\ k_2(t) & -\frac{1}{3L} & \frac{2}{3L} & -\frac{1}{3L} \\ k_3(t) & -\frac{1}{3L} & -\frac{1}{3L} & \frac{2}{3L} \end{bmatrix}, \tag{2.5}$$

where

$$k_1(t) = \frac{-2(s_1 - s_2) + (s_3 - s_4) + (s_5 - s_6)}{6L},$$
$$k_2(t) = \frac{(s_1 - s_2) - 2(s_3 - s_4) + (s_5 - s_6)}{6L},$$
$$k_3(t) = \frac{(s_1 - s_2) + (s_3 - s_4) - 2(s_5 - s_6)}{6L}. \tag{2.6}$$

Post-Fault System Model

Now, in the system of Fig. 2.3, assume the occurrence of a fault that causes the matrices $A_{\sigma(t)}$ and $B_{\sigma(t)}$ to change. For example (and without loss of generality), consider a fault in phase a that causes the resistance value R_a to change over time; this could be a gradual increase in resistance, i.e., a *soft fault*; or a sudden fault causing an open-circuit, i.e., a *hard fault*. Thus, to capture this class of faults, the value that the phase a resistance takes over time can be described by $R_a(t) = R + \Delta R_a(t)$, where R is the pre-fault (nominal) phase a resistance, and $\Delta R_a(t)$ describes the magnitude of the fault as time evolves. Then, after this fault, the system dynamics can be described by

$$\frac{dx}{dt} = \tilde{A}_{\sigma(t)}x(t) + \tilde{B}_{\sigma(t)}u(t), \tag{2.7}$$

where $\tilde{B}_{\sigma(t)} = B_{\sigma(t)}$, $\forall t$, and

$$\tilde{A}_{\sigma(t)} = \begin{bmatrix} -\frac{R}{L} - \frac{2\Delta R_a(t)}{3L} & 0 & 0 \\ \frac{\Delta R_a(t)}{3L} & -\frac{R}{L} & 0 \\ \frac{\Delta R_a(t)}{3L} & 0 & -\frac{R}{L} \end{bmatrix}.$$

It can be shown (see, e.g., [36]) that (2.7) can be written as the pre-fault dynamics in (2.1) plus an additional term that captures the effect of the fault on the pre-fault system dynamics:

$$\frac{dx(t)}{dt} = A_{\sigma(t)}x + B_{\sigma(t)}u(t) + \phi(t)f, \tag{2.8}$$

where $f = [-2, 1, 1]^T$ is referred to as the *fault signature*, and $\phi(t) = \frac{\Delta R_a(t)}{3L} i_a(t)$ is referred to as the *fault magnitude function*. In this case, although the fault magnitude is not a function of the switching signal, in general it is.

A similar development follows for the case when there is a fault that affects the observation equations in (2.2)–(2.3), i.e., we can write the post-fault observation equation as the pre-fault observation equations plus an additional term that captures the effect of the fault. Thus

$$y(t) = Hx(t) + \theta(t)g, \tag{2.9}$$
$$z(t) = Du(t) + \rho(t)h, \tag{2.10}$$

where $\theta(t)g$ and $\rho(t)h$ capture the effect of faults.

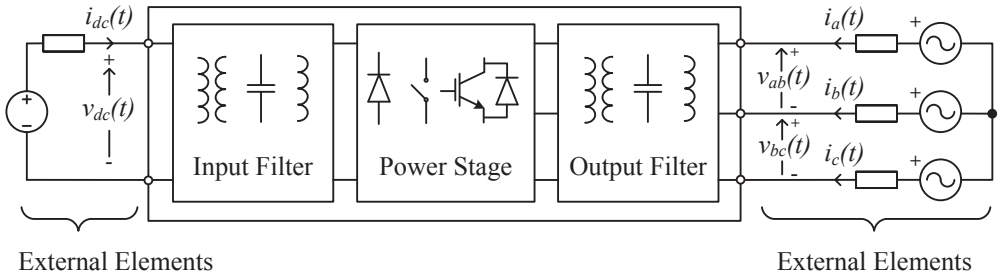


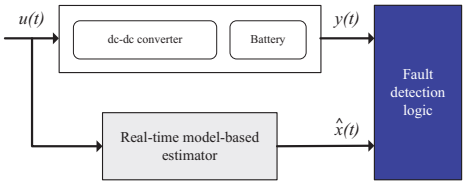
Figure 2.4: AC-DC power electronics system building blocks.

Generalized Model for Arbitrary Switching Power Electronics Systems

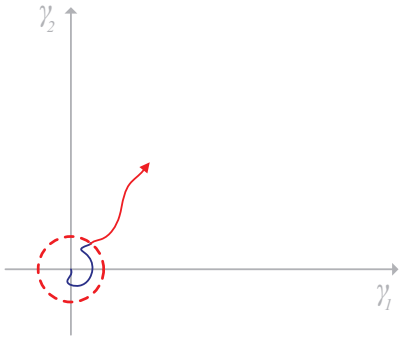
In this section, we generalize the modeling ideas introduced thus far to any switching power electronics system of the form in Fig. 2.4 that can obtained by a cascade interconnection of: i) an input filter comprised of storage elements, ii) a power stage comprised of switching devices, and iii) an output filter also comprised of storage elements. The *external elements* connected to the DC and AC ends are not considered part of the system and as such we are not concerned with detecting faults in these elements (we assume they have their own FDI mechanisms as appropriate). However, we assume that some of the interface variables that these external elements share with the power electronics system can be measured (e.g., line-to-line voltages or phase currents on the ac end, and voltage across the terminals of the dc end). This essentially decouples the detection of faults within the power electronics system from events affecting the external elements.

Let $x(t) \in \mathbb{R}^n$ denote the state vector, $u(t) \in \mathbb{R}^m$ the input vector, $y(t) \in \mathbb{R}^n$ the state measurements, $u(t) \in \mathbb{R}^m$ the input measurements, and $\sigma(t)$ the switching signal. Consider s different possible component faults, the j^{th} of which is described by a real-valued function $\phi_j(t)$—the fault magnitude function—, and a vector f_j—the fault signature. Similarly, we also assume that the state-measurement [input-measurement] sensors are subject to r [q] faults, each of which is captured by an additive perturbation of the form $\theta_j(t)g_j$ [$\rho_j(t)h_j$], where $\theta_j(t)$ [$\rho_j(t)$] is the fault magnitude function and g_j [h_j] is the fault signature. Then, the dynamics of an AC-DC power electronics system of the form in Fig. 2.4 (including the behavior in the presence of faults) can be generally described by

$$\begin{aligned}
\frac{dx(t)}{dt} &= A_{\sigma(t)}x(t) + B_{\sigma(t)}u(t) + \sum_{j=1}^{s}\phi_j(t)f_j, \\
y(t) &= Hx(t) + \sum_{j=1}^{r}\theta_j(t)g_j, \\
z(t) &= Du(t) + \sum_{j=1}^{q}\rho_j(t)h_j,
\end{aligned} \tag{2.11}$$



(a) A block diagram of the fault detection process.



(b) A sketch of the evolution of $\gamma(t)$. The red dotted line indicates the fault detection threshold.

Figure 2.5: The fault detection stage.

where we impose the matrix $H \in \mathbb{R}^{n\times n}$ to be full rank, i.e., all the states (or linear combinations thereof) can be measured. This automatically ensures that the pairs $\{A_p, H\},\ p \in \mathcal{P}$, are observable, which is necessary in the development of our FDI filters. Similarly, we impose $D \in \mathbb{R}^{m\times m}$ to be also full rank.

2.3 Fault detection logic

In this section, we will discuss the fault detection logic stage, as shown in Fig. 2.5a. We present the design and implementation of two approaches to the fault detection logic stage. The first is an estimator (parity equation) based approach, and the second is an Luenberger observer based approach. In both approaches, fault detection is achieved by generating a time-varying filter residual $\gamma(t)$, which becomes non-zero in the presence of a fault. When the magnitude of $\gamma(t)$ exceeds a predefined threshold, the fault detection logic indicates a binary flag that a fault has occurred.

Estimator (parity equation) approach

To achieve the desired fault detection properties, we first propose a linear-switched estimator of the following form:

$$\frac{d\hat{x}(t)}{dt} = A_{\sigma(t)}\hat{x}(t) + B_{\sigma(t)}u(t) \tag{2.12}$$

$$\gamma(t) = y(t) - H\hat{x}(t) \tag{2.13}$$

where $\hat{x}(t)$ is the estimated state vector, $\gamma(t)$ is the error residual vector, $u(t)$, $y(t)$, and $\sigma(t)$ are obtained via measurement, and $A_{\sigma(t)}$, $B_{\sigma(t)}$, and H are as in (2.4) and (2.2).

The open loop error dynamics are stable, that is, that the trajectories $\hat{x}(t)$ and $x(t)$ cannot diverge.[‡] Moreover, due to lossiness in the converter and the corresponding model, we can show that $x(t) - \hat{x}(t)$ asymptotically converges to zero in steady state [14].

In the nominal operating state, the dynamics of the error residual vector $\gamma(t)$ are as follows:

$$\frac{de(t)}{dt} = A_{\sigma(t)}e(t) \tag{2.14}$$

$$\gamma(t) = He(t) \tag{2.15}$$

where $e(t) := x(t) - \hat{x}(t)$. Since $e(t)$ asymptotically converges to zero, $\gamma(t)$ will converge to zero in the fault-free state, as desired.

Component faults manifest as changes in $A_{\sigma(t)}$ and $B_{\sigma(t)}$. Consider the i^{th} component fault. The dynamics of the error residual vector $\gamma(t)$ in the presence of this fault are as follows:

$$\frac{de(t)}{dt} = A_{\sigma(t)}e(t) + \phi_{i,\sigma(t)}f_i \tag{2.16}$$

$$\gamma(t) = He(t) \tag{2.17}$$

The non-zero magnitude of the component fault magnitude function $\phi_{i,\sigma(t)}(t, x(t), u(t))$ causes $\gamma(t) \neq 0$, which enables fault detection.

Sensor faults manifest as changes in H. Consider the j^{th} sensor fault. The dynamics of the error residual vector $\gamma(t)$ in the presence of this fault are as follows:

$$\frac{de(t)}{dt} = A_{\sigma(t)}e(t) \tag{2.18}$$

$$\gamma(t) = He(t) + \theta_{j,\sigma(t)}g_j \tag{2.19}$$

Again, $e(t)$ will asymptotically converge to zero. Thus, $\gamma(t)$ will asymptotically converge to the sensor fault magnitude function and fault signature $\theta_{j,\sigma(t)}g_j$, which enables fault detection since $\gamma(t) \neq 0$.

Luenberger observer approach

Next, we propose a piecewise linear FDI observer, which is comprised of a collection of linear state-space models (subsystems), each of which has the same structure of a Luenberger observer, including the corresponding gain matrix. The transitions between the subsystems are determined by the same rules that govern the switching in the actual system. A challenge is to design the individual gain matrices so that i) the detection filter residual exhibits

[‡]One can construct a natural Lyapunov function $V(\gamma)$ corresponding to the energy in the increment of the switching converter. Results from [32] prove that $\dot{V}(\gamma) \leq 0$ for a lossy switching converter containing linear passive reactive elements, switching elements, and time-varying sources.

certain geometric characteristics for each particular fault, and ii) the observer is stable. With respect to ii), it is well-known that choosing the individual gains such that each subsystem is stable is not sufficient for ensuring stability (see, e.g., [21]). Thus, as part of the FDI filter design procedure outlined here, we provide sufficient conditions that ensure the choice of gain matrices renders the filter stable.

In order to solve the FDI observer design problem, we propose a causal filter of the form

$$\begin{aligned} \frac{d\hat{x}(t)}{dt} &= A_{\sigma(t)}\hat{x} + B_{\sigma(t)}D^{-1}z(t) + L_{\sigma(t)}\gamma(t), \\ \gamma(t) &= y(t) - H\hat{x}(t). \end{aligned} \tag{2.20}$$

where $\sigma(t)$, $A_{\sigma(t)}$, $B_{\sigma(t)}$, $p \in \mathcal{P}$ and H as in (2.11); and

$$L_{\sigma(t)} = \left[\mu I_n + A_{\sigma(t)}\right] H^{-1}, \ \forall t, \tag{2.21}$$

for some $\mu > 0$ (I_n denotes the $n \times n$ identity matrix). Next, we establish that with the choice of $L_{\sigma(t)}$'s in (2.21), the FDI filter in (2.20) is stable and satisfies properties for fault detection.

In this case, for all $t > 0$, in (2.11) we have that $\phi_j(t)f_j = 0, \ \forall j$. Let $e(t) := x(t) - \hat{x}(t)$, then by subtracting (2.20) from (2.11), we obtain that

$$\frac{de(t)}{dt} = \left[A - L_{\sigma(t)}H\right] e(t),$$

but with the choice of $L_{\sigma(t)}$ in (2.21), we have that

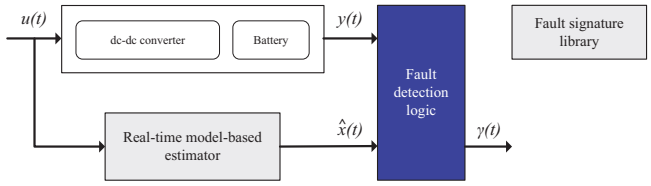
$$\begin{aligned} \frac{de(t)}{dt} &= -\mu e(t), \\ \gamma(t) &= Ce(t), \end{aligned}$$

for some $\mu > 0$, from where we obtain that $\lim_{t\to\infty} \gamma(t) = 0$, thus we have that $\gamma(t)$ approaches zero in the absence of faults. We will subsequently show that $\gamma(t) \neq 0$ in the presence of faults, which enables fault detection.

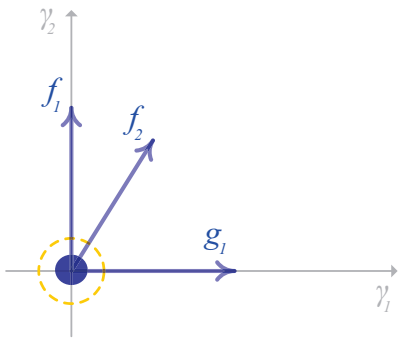
2.4 Fault signature library

In this section, we discuss the design and implementation of the fault signature library. Fig. 2.6 illustrates a block diagram and sketch of the basic concept. Fundamentally, the fault signature library defines a set of time-varying directional unit vectors that predicts the evolution of $\gamma(t)$ based on the converter model. The fault signature vectors can be derived from the model of the switching power converter, and can be used to describe a broad class of component, sensor, and input faults.

The derivation of the fault signature library for the estimator (parity equation) approach and for the Luenberger observer approach differ slightly, and are discussed here.



(a) A block diagram of the fault signature library process.



(b) A sketch of the elements of the fault signature library. The blue vectors indicate a particular component, sensor, or input fault signature vector.

Figure 2.6: The fault signature library.

Fault signature library for the estimator (parity equation) fault detection approach

For the estimator (parity equation) fault detection approach, we will derive the fault signature vectors for faults affecting $\{A_{\sigma(t)}, B_{\sigma(t)}\}$ and H.

Fault signature vectors for faults affecting $\{A_{\sigma(t)}, B_{\sigma(t)}\}$

Component faults manifest as changes in $A_{\sigma(t)}$ and $B_{\sigma(t)}$. Consider the i^{th} component fault. The dynamics of the error residual vector $\gamma(t)$ in the presence of this fault are as follows:

$$\frac{de(t)}{dt} = A_{\sigma(t)}e(t) + \phi_{i,\sigma(t)}f_i \tag{2.22}$$

$$\gamma(t) = He(t) \tag{2.23}$$

The non-zero magnitude of the component fault magnitude function $\phi_{i,\sigma(t)}(t, x(t), u(t))$ causes $\gamma(t) \neq 0$, which enables fault detection. Moreover, $\gamma(t)$ will evolve in the direction of Hf_i. Thus, by computing the L^2-inner product $\langle \gamma(t), \overline{Hf_i} \rangle_{L^2}$ on an interval $[t-W, t]$, where $\overline{Hf_i}$ denotes the normalized fault signature vector Hf_i, we can identify the fault signature that $\gamma(t)$ most closely aligns with, and thus, achieve fault identification.

Fault signature vectors for faults affecting H

Sensor faults manifest as changes in H. Consider the j^{th} sensor fault. The dynamics of the error residual vector $\gamma(t)$ in the presence of this fault are as follows:

$$\frac{de(t)}{dt} = A_{\sigma(t)}e(t) \tag{2.24}$$

$$\gamma(t) = He(t) + \theta_{j,\sigma(t)}g_j \tag{2.25}$$

Again, $e(t)$ will asymptotically converge to zero. Thus, $\gamma(t)$ will asymptotically converge to the sensor fault magnitude function and fault signature $\theta_{j,\sigma(t)}g_j$, which enables fault detection since $\gamma(t) \neq 0$. Moreover, we can compute the L^2-inner product $\langle \gamma(t), \overline{g_j} \rangle_{L^2}$ on an interval $[t - W, t]$, where $\overline{g_j}$ denotes the normalized fault signature vector g_j, to identify the appropriate sensor fault.

Fault signature library for the Luenberger observer fault detection approach

For the Luenberger observer fault detection approach, we will derive the fault signature vectors for faults affecting $\{A_{\sigma(t)}, B_{\sigma(t)}\}$, H, and D.

Fault signature vectors for faults affecting $\{A_\sigma(t), B_\sigma(t)\}$

In this case, we assume that for some $t = t_f$, the j^{th} fault affecting $A_{\sigma(t)}$ and/or $B_{\sigma(t)}$ manifests, i.e., $\phi_j(t)f_j \neq 0,\ \forall t \geq t_f$. By subtracting (2.20) from (2.11), we obtain that

$$\frac{de(t)}{dt} = -\mu e(t) + \phi_j(t)f_j,$$
$$\gamma(t) = He(t),$$

thus,

$$\gamma(t) = He^{-\mu t}e(0) + \alpha_j(t)Hf_j, \tag{2.26}$$

with

$$\alpha_j(t) = \int_0^t e^{-\mu(t-\tau)}\phi_j(\tau)d\tau. \tag{2.27}$$

Now, since $\alpha_j(t)$ is a scalar, and the first term on the right-hand side of (2.26) vanishes as $t \to \infty$, it follows that, the filter residual $\gamma(t)$ will align with the fault signature vector Hf_j as $t \to \infty$.

Fault signature vectors for faults affecting H

In this case, for some $t = t_f$, the j^{th} fault affecting H manifests, i.e., $\theta_j(t)g_j = 0,\ \forall t \geq t_f$. By subtracting (2.20) from (2.11), we obtain that

$$\begin{aligned} \frac{de(t)}{dt} &= -\mu e(t) - \theta_j(t)(A_{\sigma(t)} + \mu I)g_j, \\ \gamma(t) &= He(t). \end{aligned}$$

Let $\{t_k\},\ k = 1, 2, \ldots, n$, with $t_1 \geq 0$ and $t_n \leq t$, be the sequence of switching instants in $[0, t)$, then

$$\gamma(t) = He^{-\mu t}e(0) + \sum_{i=0}^{n} \beta_j(t_i)H(A_{\sigma(t_i)} + \mu I)g_j, \tag{2.28}$$

where

$$\beta_j(t_i) = -\int_{t_i}^{t_{i+1}} e^{-\mu(t-\tau)}\theta_j(t)d\tau, \tag{2.29}$$

with $t_0 = 0$ and $t_{n+1} = t$. Let $\{t_{k_p}\}$ denote a subsequence of $\{t_k\}$ that corresponds to the times when mode $p \in \mathcal{P}$ is activated. Then, we can rearrange the summation term in (2.28) to obtain

$$\gamma(t) = He^{-\mu t}e(0) + \sum_{p\in\mathcal{P}} \sum_{l\in\{t_{k_p}\}} \beta_j(l)H(A_p + \mu I)g_j, \tag{2.30}$$

Now, since the $\beta_j(l)$'s are scalars and the first term on the right-hand side of (2.28) vanishes as $t \to \infty$, it follows that, as $t \to \infty$, the filter residual $\gamma(t)$ will be a linear combination of the fault signature vectors in $\{H(A_p + \mu I)g\},\ p \in \mathcal{P}$.

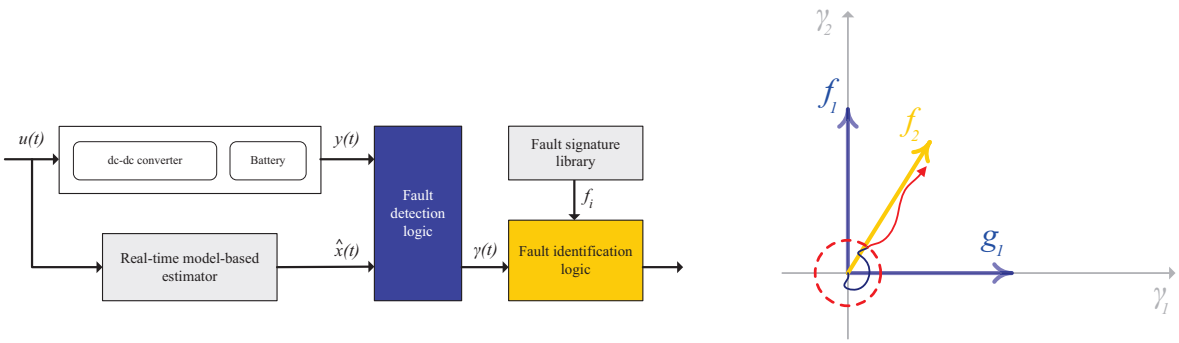
Fault signature vectors for faults affecting D

For some $t = t_f$, the j^{th} affecting D manifests, i.e., $\rho_j(t)h_j,\ \forall t \geq t_f$. By subtracting (2.20) from (2.11), we obtain

$$\begin{aligned} \frac{de(t)}{dt} &= -\mu e(t) - \rho_j(t)B_{\sigma(t)}D^{-1}h_j, \\ \gamma(t) &= He(t). \end{aligned}$$

From a similar development to that in (2.28)–(2.30), we obtain

$$\gamma(t) = He^{-\mu t}e(0) + \sum_{i=0}^{n} \kappa_j(t_i)HB_{\sigma(t)}D^{-1}h_j,$$



(a) A block diagram of the fault identification process.

(b) A sketch of the fault identification process. The residual $\gamma(t)$ closely aligns with the f_2 element of the fault signature library.

Figure 2.7: The fault identification stage.

with

$$\kappa_j(t_i) = -\int_{t_i}^{t_{i+1}} e^{-\mu(t-\tau)}\rho_j(t)d\tau, \tag{2.31}$$

and where $\{t_k\}$, $k = 1, 2, \ldots, n$, with $t_1 \geq 0$ and $t_n \leq t$, is the sequence of switching instants in $[0, t)$. Then,

$$\gamma(t) = He^{-\mu t}e(0) + \sum_{p\in\mathcal{P}}\sum_{l\in\{t_{k_p}\}} \kappa_j(l)HB_pD^{-1}h_j, \tag{2.32}$$

where $\{t_{k_p}\}$ is the subsequence of $\{t_k\}$ that corresponds to the time instants when mode $p \in \mathcal{P}$ is activated. Since the $\kappa_j(l)$'s are scalars, it follows that, as $t \to \infty$, the first term on the right-hand side of (2.32) vanishes, and thus $\gamma(t)$ will be a linear combination of the fault signature vectors in $\{HB_pD^{-1}\}$, $p \in \mathcal{P}$.

2.5 Fault identification logic

Lastly, in this section, we discuss the design and implementation of the fault identification logic. Fig. 2.6 illustrates a block diagram and sketch of the basic concept.

Fault identification is achieved by computing an L^2-inner product calculation, which determines the fault signature vector that $\gamma(t)$ most closely aligns with.

For component faults, $\gamma(t)$ will evolve in the direction of Hf_i. Thus, by computing the L^2-inner product $\langle\gamma(t), \overline{Hf_i}\rangle_{L^2}$ on an interval $[t - W, t]$, where $\overline{Hf_i}$ denotes the normalized Hf_i, we can identify the fault signature that $\gamma(t)$ most closely aligns with, and thus, achieve

fault identification.

$$\langle \gamma(t), \overline{Hf_i} \rangle_{L^2} = \int_{t-W}^{t} \gamma^T(\tau) \overline{Hf_i}(\tau) \, \mathrm{d}\tau \tag{2.33}$$

For sensor faults, we can compute the L^2-inner product $\langle \gamma(t), \overline{g_j} \rangle_{L^2}$ on an interval $[t-W, t]$, where $\overline{g_j}$ denotes the normalized g_j, to identify the appropriate sensor fault.

$$\langle \gamma(t), \overline{g_j} \rangle_{L^2} = \int_{t-W}^{t} \gamma^T(\tau) \overline{g_j}(\tau) \, \mathrm{d}\tau \tag{2.34}$$

Chapter 3

Applications for Distributed AC Grid-Connected Systems *

In this chapter, we present the design, implementation, and experimental validation of the proposed fault detection and identification methodology for distributed AC grid-connected systems. The systems considered in this chapter are (1) a three-phase inverter with an RL load, and (2) a distributed static compensator (D-STATCOM).

3.1 Three-phase inverter with RL load system

We develop the FDI approach for the three-phase inverter with RL load system shown in Fig 2.3. We first provide analytical expressions for all component fault signatures and associated fault magnitude functions, and, for certain faults, we also provide analytical expressions for the filter residual dynamics. We demonstrate the performance of the FDI filter via computer simulations and hardware experiments.

Fault Detection and Identification Filter

Consider again the three-phase inverter with RL load system of Fig. 2.3, and, as before, assume that the three phases are symmetric, i.e., $L_a = L_b = L_c = L$, and $R_a = R_b = R_c = R$. Then, the pre-fault system dynamics are described by the linear-switched state space model in (2.2)–(2.4). Assume that all the system states and inputs are directly measurable, i.e., $C = I_3$ in (2.2), and $D = I_4$ in (2.3). Then following the notation in (2.20) and (2.21), an FDI filter for this system is given by

$$\begin{aligned} \frac{d\hat{x}(t)}{dt} &= A_{\sigma(t)}\hat{x} + B_{\sigma(t)}u(t) + L_{\sigma(t)}\gamma(t), \\ \gamma(t) &= y(t) - \hat{x}(t), \end{aligned} \tag{3.1}$$

*Portions of this chapter are adapted from reference [8].

Table 3.1: Inverter with RL load: model parameters

V_{dc}	R	L	R_l	L_l	μ
230 V	0.5 Ω	12 mH	47 Ω	650 μH	500 s^{-1}

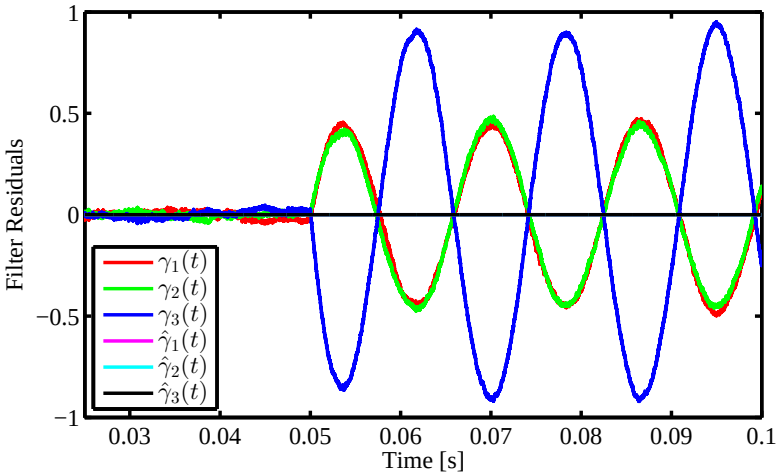


Figure 3.1: Inverter with RL load: simulation of filter response for a fault causing phase c resistance to increase by 4.5 Ω.

with $y(t) = x(t) = [i_a(t), i_b(t), i_c(t)]^T$, $z(t) = u(t) = [V_{dc}, v_a(t), v_b(t), v_c(t)]^T$; $A_{\sigma(t)}$ and $B_{\sigma(t)}$ as given in (2.5); and

$$L_{\sigma(t)} = \begin{bmatrix} -\frac{R}{L} + \mu & 0 & 0 \\ 0 & -\frac{R}{L} + \mu & 0 \\ 0 & 0 & -\frac{R}{L} + \mu \end{bmatrix},$$

for some $\mu > 0$. In this case, it is important to note that $A_{\sigma(t)}$ and $L_{\sigma(t)}$ are constant, which simplifies the filter residual expressions.

Analytical and Simulation Results

Next, we analyze the filter residual dynamics for different types of faults, providing numerical simulation results for the parameter values in Table 3.1. The simulations are performed in the MATLAB/Simulink environment using the Piece-wise Linear Electrical Circuit Simulation (PLECS) toolbox [3]. In all simulations, we implement an open-loop controller that generates sine-triangle PWM gate signals with a carrier frequency of 16 kHz.

Change in output filter phase resistance

The system dynamics for a fault causing a change in the resistance value of the output filter phase a was already derived in Section 2.2 by assuming that $R_a(t) = R + \Delta R_a(t)$, where R

Table 3.2: Inverter with RL load: fault magnitude function and signature for faults causing changes in the output filter phase resistance

i	$\phi_i(\mathrm{t})$	f_i
1	$\frac{\Delta R_a(t)}{3L} i_a(t)$	$[-2,1,1]^T$
2	$\frac{\Delta R_b(t)}{3L} i_b(t)$	$[1,-2,1]^T$
3	$\frac{\Delta R_c(t)}{3L} i_c(t)$	$[1,1,-2]^T$

is the pre-fault output filter resistance, and $\Delta R_a(t)$ describes the fault magnitude as time evolves. A similar procedure can be followed to derive the system dynamics for this type of fault in phases b and c. The resulting fault magnitude functions and fault signatures are summarized in Table 3.2.

Now, following the notation in (2.26), the filter residual dynamics for a fault affecting phase c resistance is given by

$$\gamma(t) = e^{-\mu t} e(0) + \left[\int_0^t e^{-\mu(t-\tau)} \frac{\Delta R_c(t)}{3L} i_a(t) \tau \right] f_3, \tag{3.2}$$

with $f_3 = [1,1,-2]^T$. Now, consider that at time t_f a fault occurs causing the phase c resistance to increase by $\Delta R > 0$, i.e., $\Delta R_c(t) = \Delta R$, for all $t > t_f$. While the phase currents are not perfectly sinusoidal, the filtering effect provided by the output filter ensures that $i_c(t) \approx I \sin(\omega t)$ for some $I > 0$, then, as $t \to \infty$, it follows from (3.2) that

$$\gamma(t) \approx \hat{\gamma}(t) := \frac{I \Delta R}{3L} \frac{\mu \sin(\omega t) - \omega \cos(\omega t)}{\omega^2 + \mu^2} f_3. \tag{3.3}$$

In the simulation environment, a fault causing the phase c resistance to change according to $\Delta_{R_c}(t) = \Delta R = 4.5\ \Omega$ was injected at $t = t_f = 0.05$ s. The filter residual response $\gamma(t) = [\gamma_1(t), \gamma_2(t), \gamma_3(t)]^T$ is shown in Fig. 3.1, where we can see that for all $t > 0.05$ s, $\gamma(t) \neq 0$ and almost immediately after the fault occurs, the filter residual settles to a solution where $\gamma_1(t) = \gamma_2(t)$ and $\gamma_3(t) = -2\gamma_2(t)$. i.e., $\gamma(t)$ aligns with $f_3 = [1,1,-2]^T$, as expected from the analytical results in Table 3.2. In the same figure, we also plot $\hat{\gamma}(t) = [\hat{\gamma}_1(t), \hat{\gamma}_2(t), \hat{\gamma}_3(t)]^T$ as defined in (3.3). As we discuss later, the fact that the filter residual response is almost sinusoidal will play a key role in isolating this fault, i.e., distinguishing it apart from other faults with the same fault signature.

Output filter phase open-circuit fault

This fault can be modeled by increasing the value of the output filter phase resistance by several orders of magnitude. In this regard, on one hand, by examining $\phi_3(t) = \frac{\Delta R_c(t)}{L} i_c(t)$, which corresponds to a fault in phase c, we observe that this type of fault would result

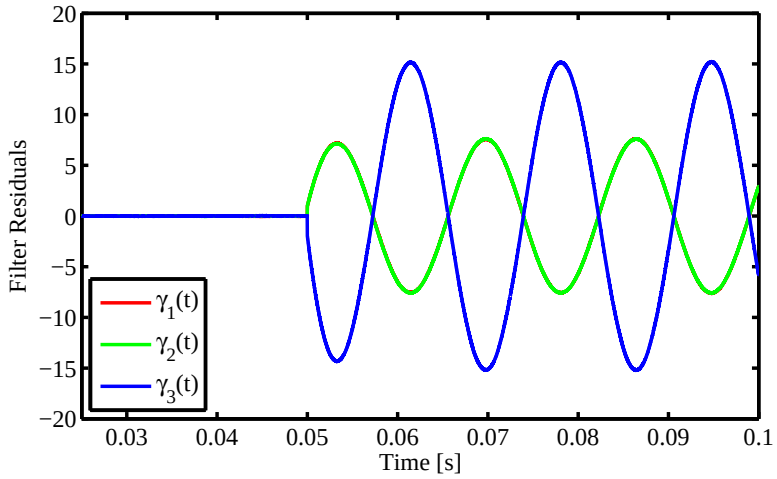


Figure 3.2: Inverter with RL load: simulation of filter response for an open-circuit fault in phase c.

Table 3.3: Inverter with RL load: fault magnitude function and signature for faults causing changes in the output filter phase inductance

i	$\phi_i(\mathrm{t})$	f_i
4	$\frac{\lambda_a \Delta L_a(t) V_{dc} - 3\left(R\Delta L_a(t) - L\frac{d\Delta L_a(t)}{dt}\right) i_a(t)}{3L(3L+2\Delta L_a(t))}$	$[-2,1,1]^T$
5	$\frac{\lambda_b \Delta L_b(t) V_{dc} - 3\left(R\Delta L_b(t) - L\frac{d\Delta L_b(t)}{dt}\right) i_b(t)}{3L(3L+2\Delta L_b(t))}$	$[1,-2,1]^T$
6	$\frac{\lambda_c \Delta L_c(t) V_{dc} - 3\left(R\Delta L_c(t) - L\frac{d\Delta L_c(t)}{dt}\right) i_c(t)}{3L(3L+2\Delta L_c(t))}$	$[1,1,-2]^T$

$\sigma(t)$	1	2	3	4	5	6	7	8
λ_a	0	1	1	2	-2	-1	-1	0
λ_b	0	1	-2	-1	1	2	-1	0
λ_c	0	-2	1	-1	1	-1	2	0

in a very large $\Delta R_c(t)$, possibly resulting in a large $\phi_3(t)$; on the other hand, $i_c(t)$ should decrease significantly, counteracting the large increase in $\Delta R_c(t)$, which would hopefully result in a reasonably small value for $\phi_3(t)$. This is indeed the case as shown in Fig. 3.2 by setting $\Delta R_c(t) = \Delta R = 1$ MΩ, $\forall t > 0.05$ s; where not only we see that the amplitude of the filter residual $\gamma(t)$ is similar to the one shown in Fig. 3.1, but also we see that, after the transient vanishes, the residual aligns with $f_3 = [1,1,-2]^T$. While this fault has the same fault signature as a fault causing a change in the phase resistance, the filter response is different, thus these two faults can be easily distinguished apart. In particular, by inspecting Figs. 3.1 and 3.2, we observe that the residual amplitude for the open-circuit fault is about 15 times greater than the amplitude for the resistance fault.

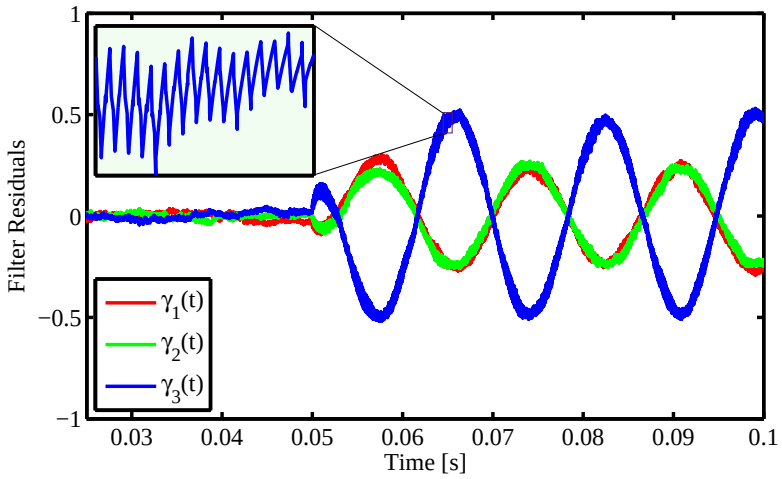


Figure 3.3: Inverter with RL load: simulation of filter response for a fault causing phase c inductance to decrease by 6 mH.

Change in output filter phase inductance

As with the output filter phase c resistance fault, this fault can be modeled by describing the phase inductance as $L_c(t) = L + \Delta L_c(t)$, where L is the pre-fault phase c inductance, and $\Delta L_c(t)$ describes the fault magnitude as time evolves. Deriving the post-fault dynamics for this case is more involved than for the resistance case as we need to manipulate terms of the form $\frac{d}{dt}\left[(L + \Delta L_c(t))i_c(t)\right]$; we omit this derivation, but provide the details of a similar one in the D-STATCOM case study presented in Section 3.2. For all three phases, Table 3.3 presents the resulting fault magnitude functions and fault signatures.

Figure 3.3 shows the filter residual response $\gamma(t)$ for a fault injected at $t = t_f = 0.05$ s that causes the phase c inductance to change as $\Delta_{L_c}(t) = \Delta L = -6$ mH. Almost immediately after the fault occurs, the filter residual aligns with $f_6 = [1, 1, -2]^T$ (see Table 3.3); however this prevents fault identification as f_6 is equal to f_3, which corresponds to the signature of a fault that causes the output filter phase c resistance to change (see Table 3.2). Although we do not include the analysis results, the fault signatures of an open-circuit fault in SW_5 and SW_6 also coincide with fault signatures f_3 and f_6.

Fault identification

From the analysis above, it is obvious that once the fault occurs, it can be detected as the filter residual is no longer zero. However, the fault signatures of all the components in each phase are the same, e.g., for phase c, the resistance, inductance and switches SW_5 and SW_6 (not analyzed above) have the same fault signature $[1, 1, -2]^T$, therefore by just analyzing the direction of the filter residual we can not distinguish these faults apart. A closer look at Figs. 3.1 and 3.3, corresponding to the filter residual response for faults causing, respectively, a change in phase c resistance and inductance, reveals that the fault magnitude function of

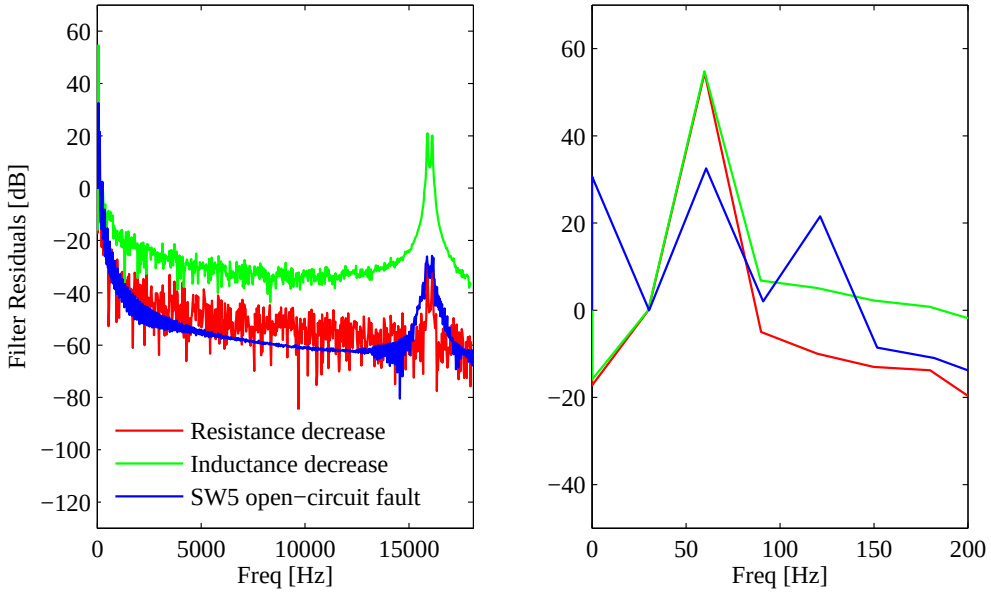


Figure 3.4: Inverter with RL load: frequency analysis of the filter residual magnitude for faults phase in c.

these faults (see Tables 3.2 and 3.3) yield significantly different responses. In particular, the filter residual response for the resistance fault is a 60-Hz sinusoid, whereas the residual response for the inductance fault also contains higher order harmonics. Thus, a spectral analysis of the residual magnitude provides additional information to distinguish these faults apart.

Figure 3.4 shows the spectral analysis of the individual filter residual magnitude functions for faults in phase c causing i) the output filter resistance to decrease, ii) the output filter inductance to decrease, and iii) an open-circuit in SW_5. For the resistance fault, the spectrum is concentrated mostly around 60 Hz, with a small double peak around the switching frequency. The spectrum for the inductor shares some features with the spectrum of the resistor fault; however, the peak near the switching frequency is much larger ($\sim$ 30 dB) than for the resistance fault due to the dependence of the filter residual on the switching signal. Thus, this peak near the switching frequency can be used to distinguish this fault apart from the resistance fault. For an open-circuit in SW_5, the 60-Hz component and the peak around the switching frequency are similar to the ones for the inductance fault, but there are two additional components at 0 Hz and 120 Hz. Thus, these two additional frequency components can be used to distinguish apart inductance and switch open-circuit faults.

Current sensor fault

Consider the current sensor of phase c; a fault in this sensor can be modeled by describing the corresponding observation equation as $y_3 = [1 + \Delta G_c(t)]x_3(t) + \Delta B_c(t)$, where $x_3(t) = i_c(t)$

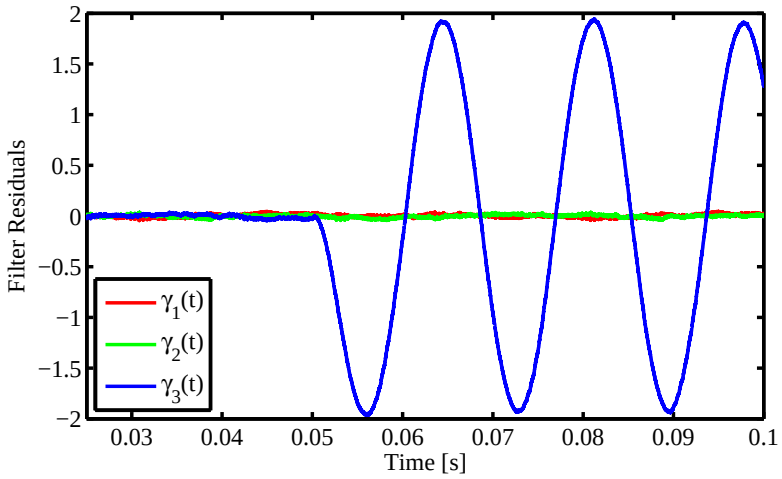


Figure 3.5: Inverter with RL load: simulation of filter response for a omission fault in phase c current sensor.

Table 3.4: Inverter with RL load: fault magnitude function and signature for faults in current sensors

i	$\theta_i(t)$	g_i
1	$\left(-\frac{R}{L}+\mu\right)\Delta G_a(t)\left(i_a(t)+\Delta B_a(t)\right)$	$[1,0,0]^T$
2	$\left(-\frac{R}{L}+\mu\right)\Delta G_b(t)\left(i_b(t)+\Delta B_b(t)\right)$	$[0,1,0]^T$
3	$\left(-\frac{R}{L}+\mu\right)\Delta G_c(t)\left(i_c(t)+\Delta B_c(t)\right)$	$[0,0,1]^T$

and $\Delta G_c(t)$, $\Delta B_c(t)$, respectively, describe the effect of a fault that causes a change in the sensor gain and a measurement bias. Table 3.4 presents the resulting fault magnitude function and fault signature (it also collects the corresponding counterparts for faults in the current sensors of the other two phases).

As stated in property P4, when a fault in the phase c current sensor occurs, as $t \to \infty$, the filter residual should lie in the subspace spanned spanned by $\{C(A_p + \mu I)g_3\}, p \in \mathcal{P}$. However, for this particular system, the filter residual aligns with $g_3 = [0,0,1]^T$; this is the case because $C = I_3$ and $A_{\sigma(t)}$ is diagonal. Figure 3.5 shows the filter residual response $\gamma(t)$ for a so-called omission fault in the current sensor of phase c, i.e., $\Delta G(t) = -1$, for all $t > t_f$, where $t_f = 0.05$ s, and $\Delta B(t) = 0,\ \forall t$. As expected, almost immediately after the fault, the residual aligns with $g_3 = [0,0,1]^T$.

Experimental Results

In order to experimentally demonstrate the feasibility of the proposed filter for FDI in the system of Fig. 2.3, we developed the experimental testbed shown in Fig. 3.6. All three phase currents and voltages are measured and passed to the FDI filter residual generator, which

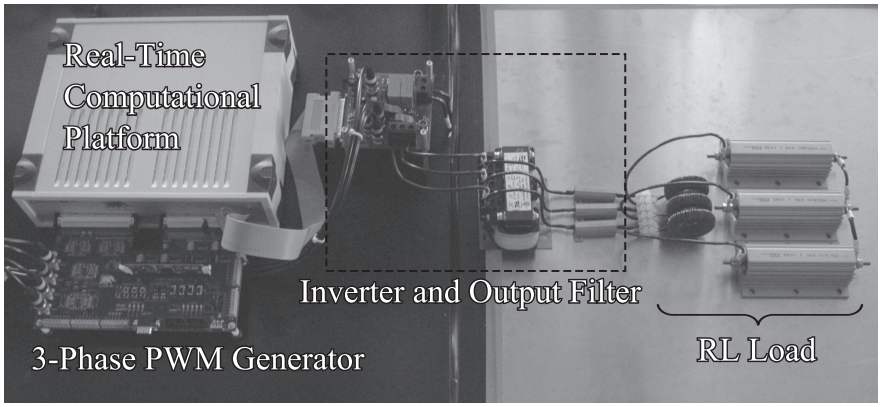


Figure 3.6: Experimental testbed main building blocks.

Table 3.5: Experimental testbed: specifications of main building blocks

DC power supply ratings	300 V, 16 A, 5 kW
Inverter module ratings	20 A, 600 V
Output filter	
Resistance, per phase	0.5 Ω
Inductance, per phase	12 mH
RL load	
Resistance, per phase	23.5 Ω, 47 Ω (nominal), 67 Ω, 94 Ω
Inductance, per phase	650 μH
Current sensors bandwidth	200 kHz
PWM generator	
Switching frequency	4 kHz
Dead time	1 μs
Volts / freq. scalar	3.83
Real-time platform	
FPGA device	Xilinx Virtex-5 ML506
Clock speed	100 MHz
ADC sapling rate	1 MSPS
DAC sampling rate	1 MSPS

is implemented in a FPGA-based platform, running on a real-time processor in lockstep with the physical system. Additionally, we have a mechanism to artificially inject certain faults into the physical system; for each of these faults, we compare the resulting filter residual response with that obtained with the simulation-based model. Table 3.5 provides the specifications of the main building blocks that comprise the experimental testbed.

FDI filter implementation

As time evolves, to execute the FDI filter in lockstep with the physical system, we use the generalized automaton modeling approach described in [25], which, among other things, enables the implementation of the linear-switched state-space model in (2.20)–(2.21) that

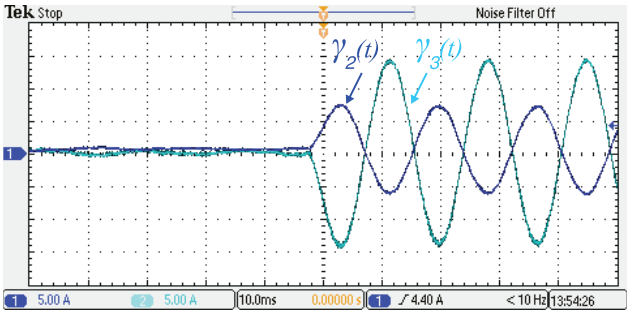


Figure 3.7: Inverter with RL load: experimental filter response for an open-circuit fault in phase c.

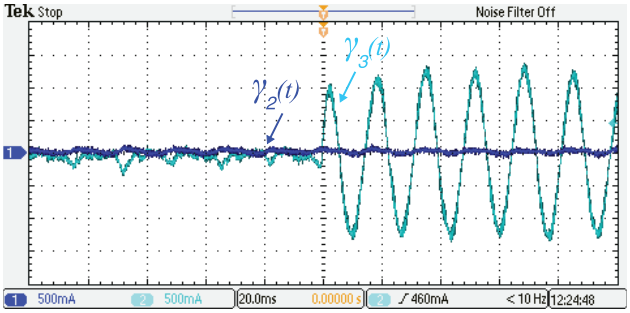
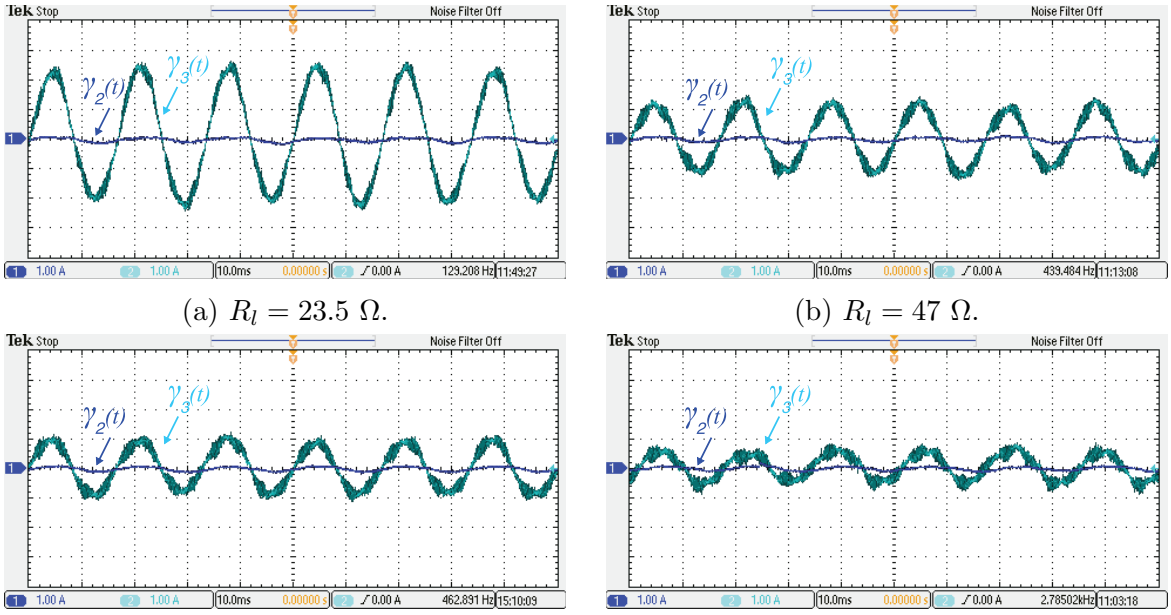


Figure 3.8: Inverter with RL load: experimental filter response for an omission fault in phase c current sensor.

defines the FDI filter. During real-time execution, a direct memory indexing technique controls the selection of the active mode based on the system input $u(t)$ and boundary conditions defined by $\hat{y}(t) = C\hat{x}$. A linear solver computes the state vector $\hat{x}(t)$ and the corresponding estimated output vector $\hat{y}(t)$, and filter residual $\gamma(t)$. An internal signal generator and external analog and digital input ports provide the input vector $u(t)$ to the state-space solver. The state vector $\hat{x}(t)$ and the output vector $\hat{y}(t)$ are accessible in real-time through low-latency analog output ports. The processor architecture, which is implemented in an FPGA, guarantees the execution time for each time interval to be shorter than the fixed simulation time step. Furthermore, the loop-back latency is minimized with custom designed input-output hardware, and has been characterized to be on the order of 1 μs [25].

Phase open-circuit fault

Figure 3.7 shows the real-time FDI filter residual response before and after phase c of the RL load is disconnected (so as to mimic the effect of an open-circuit fault in this phase). In this figure, we can see that after the transient vanishes, the filter residual is proportional to the vector $[1, 1, -2]^T$, which matches the fault signature f_3 analytically derived for this type of fault (see Table 3.2). Also, the filter residual exhibits a sinusoidal behavior, matching the simulation results in Fig. 3.2.



(a) $R_l = 23.5\ \Omega$. (b) $R_l = 47\ \Omega$.

(c) $R_l = 67\ \Omega$. (d) $R_l = 94\ \Omega$.

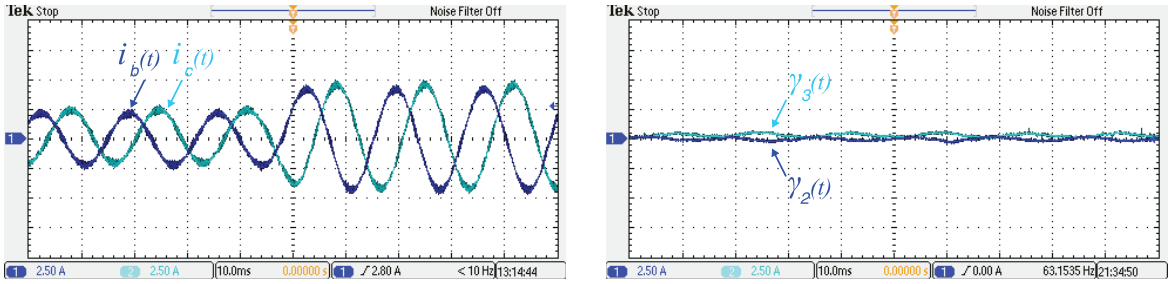
Figure 3.9: Inverter with RL load: filter response for different values of R_l and a fault in phase c current sensor. [Scope settings are 1 A/div and 10 ms/div.]

Current sensor fault

Figure 3.8 displays the real-time response of the FDI filter after the current sensor of phase c is disconnected. The filter residual matches the simulation results shown in Fig. 3.5. As in the simulations, after the transient vanishes, the filter residual aligns with the vector $[0, 0, 1]^T$, which matches the fault signature g_3 analytically derived for this fault (see Table 3.4). This provides with sufficient information to unequivocally determine that the faulty component is the current sensor of phase c.

Effect of different load parameter values

For the same fault in the current sensor of phase c discussed above, Fig. 3.9 displays the FDI filter response when the load resistance takes the following values: $R_l = 23.5\ \Omega$, $R_l = 47\ \Omega$ (nominal), $R_l = 67\ \Omega$, and $R_l = 94\ \Omega$. As it can be seen in this figure, the filter residual magnitude depends on the value that R_l takes and, in general, the larger R_l is, the smaller the residual magnitude is. However, it is important to note that, independently of the value of R_l, the filter residual aligns with the vector $[0, 0, 1]^T$; this provides with enough information to conclude that the faulty component is the current sensor of phase c.



(a) Phase currents. (b) Filter residual response.

Figure 3.10: Inverter with RL load: experimental filter response for a load variation that results in R_l to decrease by 50% of its nominal value.

Effect of load variations

Finally, we discuss the effect of load variations on the filter performance. As discussed in Section 2.2, the RL load is considered an external element to the system being monitored (in this case, comprised of a power stage and an output filter). Thus, events that affect this external element should not be flagged by the FDI filter. To illustrate this, consider a load variation that results in the load resistance changing from $R_l = 47\ \Omega$ to $R_l = 23.5\ \Omega$. Figure 3.10a shows the sudden change in phase currents when the load changes. Figure 3.10b displays the corresponding filter residual evolution; as expected, this event is not flagged as a fault.

3.2 Distributed static compensator (D-STATCOM)

In this section, we develop an FDI filter for a D-STATCOM [Distributed Static Compensator]. A D-STATCOM is a distribution-level controller that is often tied to highly nonlinear loads to reduce their disturbance to the grid, or to loads that require very strict power quality control [26, 31]. The most basic D-STATCOM consists of a voltage source converter tied to a capacitor on the dc end, and tied to a filter on the ac end (see Fig. 3.11).

Pre-Fault Dynamics and FDI Filter

Consider the circuit at the bottom left of Fig. 3.11, and assume that $L_a = L_b = L_c = L$, and $R_a = R_b = R_c = R$. Let $s_i(t)$, $i = 1, 2, \ldots, 6$, be an indicator variable that, at time t, takes value 0 whenever SW_i is open, and 1 whenever is closed. Then, the pre-fault circuit dynamics are described by

$$\begin{aligned} \frac{d}{dt}x(t) &= A_{\sigma(t)}x(t) + B_{\sigma(t)}u(t), \\ y(t) &= Hx(t), \end{aligned} \tag{3.4}$$

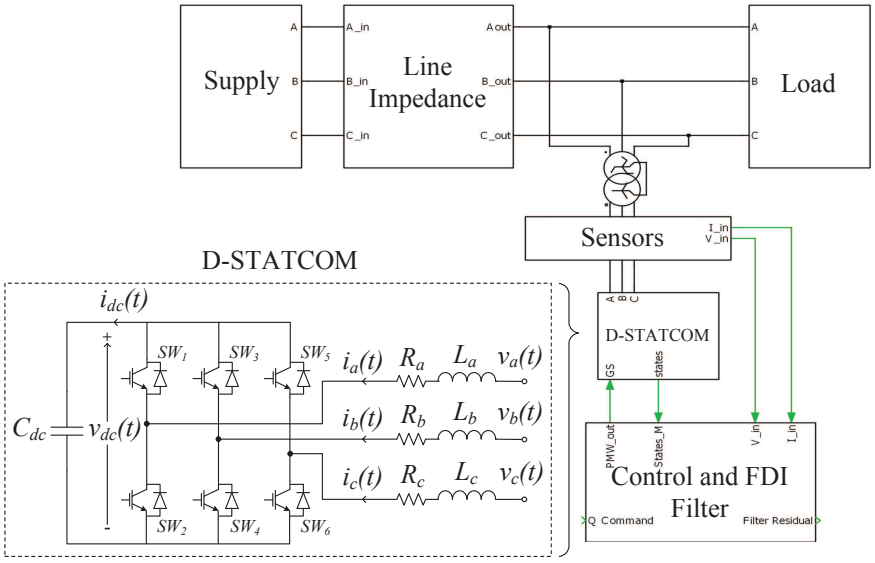


Figure 3.11: D-STATCOM Simulation Block Diagram.

where $x(t) = [i_a(t), i_b(t), i_c(t), v_{dc}(t)]^T$, $u(t) = [v_a(t), v_b(t), v_c(t)]^T$, $C = I_4$, $D = I_3$, and

$$A_{\sigma(t)} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & k_{1(t)} \\ 0 & -\frac{R}{L} & 0 & k_2(t) \\ 0 & 0 & -\frac{R}{L} & k_3(t) \\ k_4(t) & k_5(t) & k_6(t) & k_7(t) \end{bmatrix},$$

$$B_{\sigma(t)} = \begin{bmatrix} \frac{2}{3L} & -\frac{1}{3L} & -\frac{1}{3L} \\ -\frac{1}{3L} & \frac{2}{3L} & -\frac{1}{3L} \\ -\frac{1}{3L} & -\frac{1}{3L} & \frac{2}{3L} \\ 0 & 0 & 0 \end{bmatrix}, \tag{3.5}$$

with

$$\begin{aligned} k_1(t) &= \frac{-2(s_1 - s_2) + (s_3 - s_4) + (s_5 - s_6)}{6L}, \\ k_2(t) &= \frac{(s_1 - s_2) - 2(s_3 - s_4) + (s_5 - s_6)}{6L}, \\ k_3(t) &= \frac{(s_1 - s_2) + (s_3 - s_4) - 2(s_5 - s_6)}{6L}, \\ k_4(t) &= \frac{s_1 - s_2}{C_{dc}}, \quad k_5(t) = \frac{s_3 - s_4}{C_{dc}}, \\ k_6(t) &= \frac{s_5 - s_6}{C_{dc}}, \quad k_7(t) = 0, \end{aligned} \tag{3.6}$$

where the possible open/closed switch combination are the same as for the inverter with RL load system (see Table 2.1).

Now, following the same notation as in (2.20) and (2.21), an FDI filter for this system is given by

$$\begin{aligned} \frac{d\hat{x}(t)}{dt} &= A_{\sigma(t)}\hat{x} + B_{\sigma(t)}u(t) + L_{\sigma(t)}\gamma(t), \\ \gamma(t) &= y(t) - \hat{x}(t), \end{aligned} \tag{3.7}$$

with $y(t) = x(t)$, $z(t) = u(t)$; $A_{\sigma(t)}$ and $B_{\sigma(t)}$ as in (3.5); and

$$L_{\sigma(t)} = \begin{bmatrix} -\frac{R}{L} + \mu & 0 & 0 & k_{1(t)} \\ 0 & -\frac{R}{L} + \mu & 0 & k_2(t) \\ 0 & 0 & -\frac{R}{L} + \mu & k_3(t) \\ k_4(t) & k_5(t) & k_6(t) & \mu \end{bmatrix},$$

for some $\mu > 0$. In this case, it is important to note that, unlike in the inverter with RL load system, the matrices $A_{\sigma(t)}$ and $L_{\sigma(t)}$ depend on the switching signal, which complicates the detection and identification of faults affecting C. On the other hand, since $B_{\sigma(t)}$ is constant, the detection of faults affecting D simplifies significantly.

Analytical and Simulation Results

Next, we analyze the filter residual dynamics for different types of faults, providing numerical simulation results for the parameter values in Table 3.6; the simulations are performed in MATLAB/Simulink/PLECS. Figure 3.11 provides a block diagram of the simulation model; the *supply* block is comprised of a three-phase ideal voltage source, the *line impedance* block is a series-connection of inductors and resistors, whereas the *load* block is comprised of inductive reactances. The controller is adapted from the voltage-mode controller in [12]. This controller includes a phase-lock loop that generates sine-triangle PWM gate signals with a carrier frequency of 5 kHz.

Change in dc end capacitance

In order to capture the effect of this fault, we describe the capacitance as $C_{dc}(t) = C_{dc} + \Delta C_{dc}(t)$, where C_{dc} is the pre-fault capacitance value and $\Delta C_{dc}(t)$ describes the change in

Table 3.6: D-STATCOM model parameters

V_{ac}	R	L	C_{dc}	μ
480 V	0.1 Ω	10 mH	2 mF	500 s^{-1}

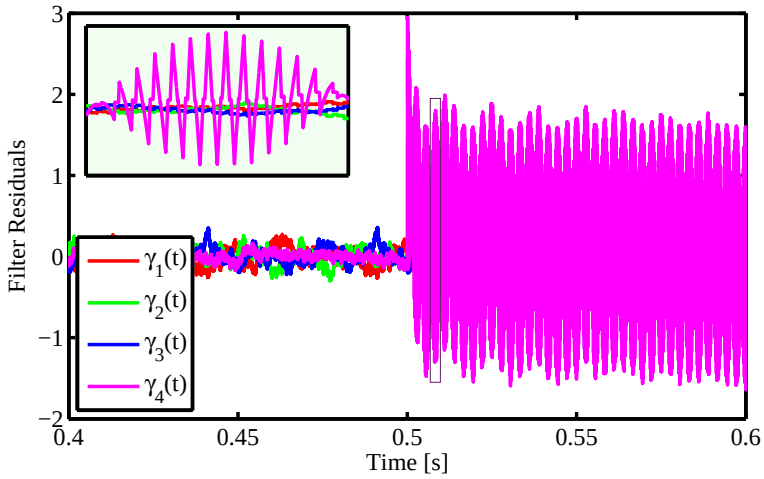


Figure 3.12: D-STATCOM: simulation of filter response for 50% decrease in dc end capacitance.

Table 3.7: D-STATCOM: fault magnitude function and signature for faults in dc end capacitor

$\phi_1(t)$	f_1
$\lambda\frac{\Delta C_{dc}(t)i_{dc}-C\frac{d\Delta C_{dc}(t)}{dt}v_{dc}}{C_{dc}[C_{dc}+\Delta C_{dc}(t)]}$	$[0,0,0,1]^T$

$\sigma(t)$	1	2	3	4	5	6	7	8
i_{dc}	0	i_c	i_b	i_a	i_a	i_b	i_c	0
λ	0	-1	-1	1	-1	1	1	0

capacitance due to the fault. Thus, the relation between the dc end voltage and current is given by $\frac{d}{dt}[C_{dc}+\Delta C_{dc}(t)]v_{dc}=i_{dc}(t)$, from where it follows that

$$\frac{dv_{dc}(t)}{dt}=\frac{1}{C_{dc}+\Delta C_{dc}(t)}\left(i_{dc}(t)-\frac{d\Delta C_{dc}(t)}{dt}v_{dc}(t)\right);$$

therefore, the post fault dynamics can be described by

$$\frac{dx(t)}{dt}=\tilde{A}_{\sigma(t)}x(t)+\tilde{B}_{\sigma(t)}u(t), \tag{3.8}$$

with $\tilde{B}_{\sigma(t)}=B_{\sigma(t)}$, and

$$\tilde{A}_{\sigma(t)}=\begin{bmatrix}-\frac{R}{L} & 0 & 0 & k_1(t)\\ 0 & -\frac{R}{L} & 0 & k_2(t)\\ 0 & 0 & -\frac{R}{L} & k_3(t)\\ \tilde{k}_4(t) & \tilde{k}_5(t) & \tilde{k}_6(t) & \tilde{k}_7(t)\end{bmatrix}, \tag{3.9}$$

where $k_1(t)$–$k_3(t)$ are the same as in (3.6), and

$$\tilde{k}_4(t) = \frac{s_1 - s_2}{C_{dc} + \Delta C_{dc}(t)},$$
$$\tilde{k}_5(t) = \frac{s_3 - s_4}{C_{dc} + \Delta C_{dc}(t)},$$
$$\tilde{k}_6(t) = \frac{s_5 - s_6}{C_{dc} + \Delta C_{dc}(t)},$$
$$\tilde{k}_7(t) = -\frac{\frac{d}{dt}\Delta C_{dc}(t)}{C_{dc} + \Delta C_{dc}(t)}. \tag{3.10}$$

Now, by rearranging (3.9) as in (2.8), we obtain the fault signature f_1, and the fault magnitude function $\phi_1(t)$, both of which are given in Table 3.7.

Figure 3.12 shows the filter residual response for a fault injected at $t_f = 0.5$ s causing a decrease of 50% in the dc end capacitance. As expected, after the initial transient vanishes, the filter residual aligns with $f_1 = [0, 0, 0, 1]^T$.

Change in output filter phase resistance

For this type of fault, it is clear from (3.5) that only the equations for the phase currents will be altered; in fact the derivation of the post-fault model is very similar to the one for the inverter with RL load model derived in Section 2.2; thus, we omit it. Therefore, the fault magnitude functions $\phi_i(t)$, $i = 2, 3, 4$, are the same as the corresponding ones in Table 3.2; however the fault signatures are 4-dimensional vectors, respectively denoted by f_2, f_3, f_4, instead of 3-dimensional ones. In particular the first three entries of each f_i, $i = 2, 3, 4$, coincide with the entries of the corresponding fault signature vectors in Table 3.2; while the fourth entry is equal to zero for all f_i's, e.g., $f_2 = [-2, 1, 1, 0]^T$. In the simulation environment, a fault causing the resistance of phase c to change from 0.1 Ω to 0.5 Ω is injected at $t_f = 0.5$ s; Fig. 3.13 shows the evolution of the filter residual. After the transient vanishes, the filter residual aligns with $f_4 = [1, 1, -2, 0]^T$, as expected.

Change in output filter phase inductance

Similarly as for faults causing changes in phase resistance, from (3.5), it is easy to see that a fault causing the phase inductance to change will only affect the current equations, with a post-fault model similar to the one for the inverter with RL load system. Then, the fault magnitude functions for phase a, b, and c inductors, denoted respectively by $\phi_5(t)$, $\phi_6(t)$, and $\phi_7(t)$ are the same as those for the inverter with RL system given in Table 3.3. The corresponding fault signature vectors, respectively denoted by f_5, f_6, f_7, are 4-dimensional. Specifically, the first three entries of each f_i are equal to the entries of the corresponding fault signature vectors in Table 3.3, while the fourth entry is equal to zero, e.g., $f_5 = [-2, 1, 1, 0]^T$. Figure 3.14 shows the filter residual evolution for a fault that causes the inductance of phase

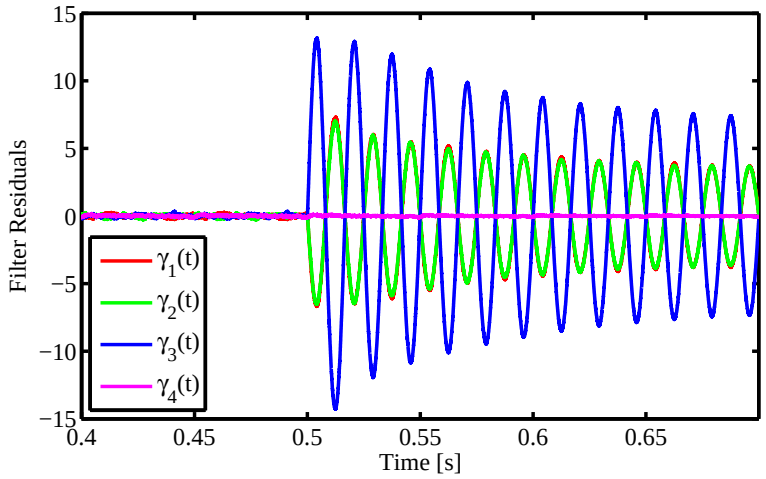


Figure 3.13: D-STATCOM: simulation of filter response for a fault causing phase c resistance to change from 0.1 Ω to 0.5 Ω.

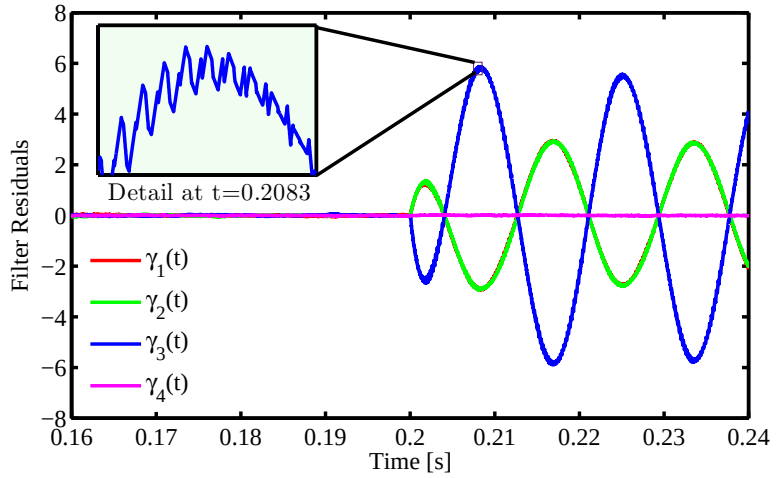


Figure 3.14: D-STATCOM: simulation of filter response for a fault causing the output filter phase c inductance to change from 10 mH to 5 mH.

c to change from 10 mH to 5 mH; as expected, when the filter residual reaches steady state, it aligns with $f_7 = [1, 1, -2, 0]^T$.

Other faults

Table 3.8 shows the fault magnitude functions and fault signatures for switch open-circuit faults; the ones for sensor faults are similar to the corresponding ones for the inverter with RL load system and are therefore omitted.

As with the inverter with RL load system, the fault signatures for all the components

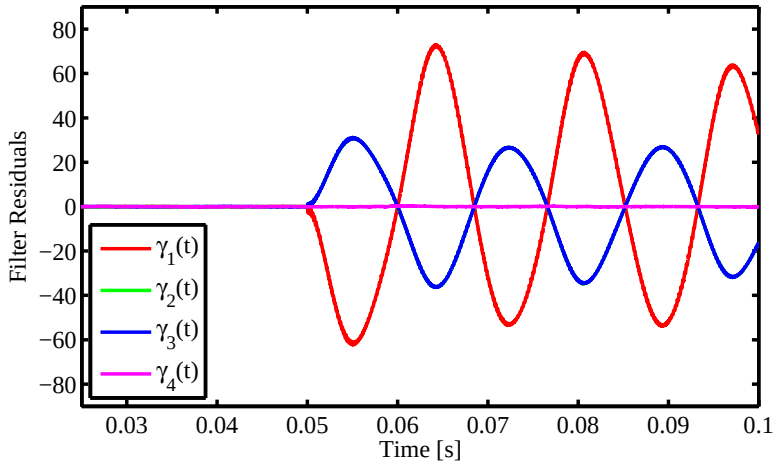


Figure 3.15: D-STATCOM: simulation of filter response for a short-circuit fault between the node connecting switches SW_1 and SW_2 and ground.

Table 3.8: D-STATCOM: fault magnitude function and signature for switch open-circuit faults

Fault	$\phi_i(\mathrm{t})$	f_i
SW_1 $(i=8)$	$\frac{-v_{dc}(t)(s_4+s_6)-3Ri_a(t)}{6}$	$[-2,1,1,0]^T$
SW_2 $(i=9)$	$\frac{v_{dc}(t)(s_3+s_5)-3Ri_a(t)}{6}$	$[-2,1,1,0]^T$
SW_3 $(i=10)$	$\frac{-v_{dc}(t)(s_2+s_6)-3Ri_b(t)}{6}$	$[1,-2,1,0]^T$
SW_4 $(i=11)$	$\frac{v_{dc}(t)(s_1+s_5)-3Ri_b(t)}{6}$	$[1,-2,1,0]^T$
SW_5 $(i=12)$	$\frac{-v_{dc}(t)(s_2+s_4)-3Ri_c(t)}{6}$	$[1,1,-2,0]^T$
SW_6 $(i=13)$	$\frac{v_{dc}(t)(s_1+s_3)-3Ri_c(t)}{6}$	$[1,1,-2,0]^T$

in the same phase are identical; these include, e.g., phase-to-ground faults. For instance, a fault causing a short circuit between the node connecting switches SW_1 and SW_2 and the (grounded) neutral point of the transformer winding on the D-STATCOM side is equivalent to both phase a resistance and inductance values suddenly dropping to zero; this is consistent with the simulation results in Fig. 3.15 that show the evolution of the filter residual for such a phase-to-ground fault. Thus, to distinguish such a fault from other faults that affect phase a, e.g., a slight increase in phase a resistance, it is necessary to analyze the residual magnitude frequency spectrum, which yields similar results to those reported in Section 3.1. Similarly, faults affecting both switches in the same leg, SW_1 and SW_2, SW_3 and SW_4, or SW_5 and SW_6 are equivalent to faults that cause the dc end capacitance to drop to zero suddenly.

Next, we discuss the performance of the filter residual for a phase-to-phase fault; in particular, we analyze a short-circuit fault between the node connecting $SW1$ and $SW2$, and the node connecting $SW3$ and $SW4$. Figure 3.16 displays the corresponding filter

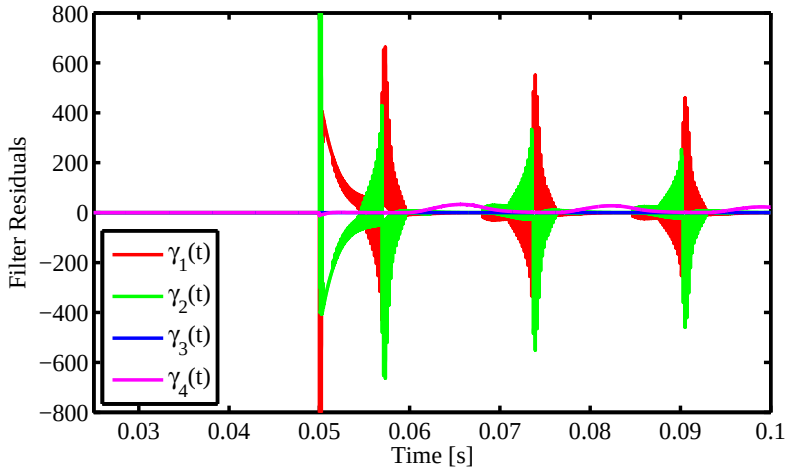
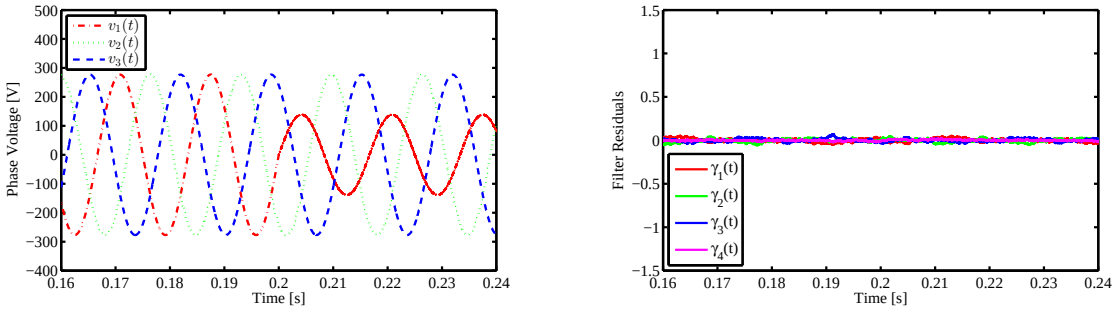


Figure 3.16: D-STATCOM: simulation of filter response for a short-circuit fault between the nodes connecting SW_1 and SW_2, and SW_3 and SW_4.



(a) Supply phase voltages.

(b) Filter residual.

Figure 3.17: D-STATCOM: filter response for a voltage sag on phase a.

residual response, where we can see that $\gamma_1(t) = -\gamma_2(t)$ for all t after the fault occurrence, i.e., for all $t > 0.05$ s. Additionally, even if not identically equal to zero, the maximum values that $\gamma_3(t)$ and $\gamma_4(t)$ take after the fault occurrence are very small relative to those that $\gamma_1(t)$ and $\gamma_2(t)$ take. These features of the residual response, which are substantially different from those of faults previously analyzed, enable distinguishing the occurrence of this type of fault from the occurrence of all other types analyzed earlier.

Faults in external elements

Finally, we discuss the effect of disturbance events affecting elements external to the D-STATCOM; in the block diagram of Fig. 3.11, these external elements are the supply, the line impedance, and the load. Detection of faults in these elements is important from the point of view of ensuring a reliable energy delivery to the load; however, the focus here is to

monitor the occurrence of faults in the components of the D-STATCOM. As such, the FDI filter should not flag as a fault any disturbance that may affect these external elements—these elements should have their own dedicated FDI mechanisms. With respect to this, we consider a voltage sag in phase a of the supply occurring at $t = 0.2$ s (see Fig. 3.17a); the corresponding filter residual evolution is displayed in Fig. 3.17b. As expected, the filter residual does not change after this event occurs because this event does not correspond to a component fault within the D-STATCOM, and therefore it is not flagged as such.

3.3 Discussion and comparison with state-of-the-art

In this section, we compare the time to detection and identification that can be achieved with this FDI approach, and the time to detection and identification that can be achieved with other FDI methods in the literature for which data is available (see Table 3.9 for details). The authors in [39] proposed a fault detection method to prevent shoot through faults in paralleled voltage source inverters; by focusing on this specific fault and converter topology, fault detection can be achieved in 3 μs, while fault identification can be achieved in 200 μs. The authors in [29, 38, 4] proposed different model-based FDI methods with detection and identification times ranging between 10 ms and 100 ms. Finally, the authors in [1] proposed a neural-network based FDI system; the time to detection and identification that can be accomplished with this system is on the order of 10 ms.

With the proposed FDI filter based on the Luenberger observer, in theory, the instant a fault occurs, the filter residual is no longer zero, and thus detecting the presence of a fault should be instantaneous. In practice, it takes about 1 μs as this is the integration step of the computational platform in [25], which is the one we use in the experimental setup described in Section 3.1. However, rather than just detecting the presence of a fault, we also want to isolate it, i.e., determine the location of the faulty component.

As stated earlier, fault identification can be accomplished through analysis of i) the filter residual direction, and ii) the residual magnitude frequency spectrum. For example, in (2.11), consider two different faults affecting $\{A_\sigma(t), B_\sigma(t)\}$, and denote them by l and m. Respectively, denote by f_l and f_m their fault signatures, and by $\phi_l(t)$ $\phi_m(t)$ their fault magnitudes. Then, assuming that H is the identity matrix, as discussed earlier, as $t \to \infty$, which happens exponentially fast at a rate μ, the filter residual aligns with f_l whenever fault l occurs, and with f_m whenever fault m occurs. Then, for $\tau_f \in (3/\mu, 5/\mu)$ s, the residual is within $1 - 5\%$ of its steady-state value, and thus we can pick the time to identification to be $t_{FDI} = \tau_f$. On the other hand, if $f_l = f_m$, the information contained in the frequency spectrum of $\alpha_l(t)$ and $\alpha_m(t)$, as defined in (2.27), can be used to distinguish the two faults apart. Thus $t_{FDI} = \tau_f + \tau_s$, where τ_s is the time it takes for the processor to perform the frequency analysis of $\alpha_l(t)$ and $\alpha_m(t)$ by using, e.g., a Fast Fourier Transform algorithm.

We have shown experimentally and through simulation that, we can choose $\mu = 500$ s^{-1} without compromising the dynamic performance of the filter. This results in an fault identification time within 6 and 10 ms, which outperforms all the methods in Table 3.9, except for

Table 3.9: Comparison of time to detection and identification for different methods proposed in the literature.

Reference	Detection Time [s]	Identification Time [s]
Zhang et al., 2009 [39]	$3 \cdot 10^{-6}$	$0.2 \cdot 10^{-3}$
Peuget et al., 1998 [29]	$21.7 \cdot 10^{-3}$	$21.7 \cdot 10^{-3}$
Yazdani et al., 2011 [38]	0.3	0.3
Araujo et al., 2003 [4]	$12.4 \cdot 10^{-3}$	None
Masrur et al., 2009 [1]	$19.5 \cdot 10^{-3}$	$19.5 \cdot 10^{-3}$
Proposed FDI filter	10^{-6}	$3/\mu$ to $5/\mu$ $(+ \tau_s)$

[39]. Note, however, that the method in [39] is for a very specific type of fault and converter topology, while our FDI filters provide flexibility to cover a wide ranges of topologies and faults.

Chapter 4

Applications for Distributed DC Networked Systems *

In this chapter, we present the design, implementation, and experimental validation of the proposed fault detection and identification methodology for distributed DC networked system. Specifically, we present a case study for a rack-level UPS DC-DC converter shown in Figure 4.1. The complete specifications for this converter are presented in Table 4.1.

First, we derive the converter model using the approach described in Section 2.2. Next, we analyze a set of component and sensor faults, and derive a set of fault signature vectors. Finally, we present simulation and experimental results that validate the proposed FDI approach for the converter.

4.1 Converter modeling

We construct a linear-time varying model of the DC-DC converter operating in continuous conduction mode. We assume that the switches $SW_{n,t}$ and $SW_{n,b}$ for $n = 1...6$ are ideal, and are controlled by an ideal complementary switching signal vector $k(t)$, where $k_n(t) = 1$ indicates that $SW_{n,t}$ is 'on' and $SW_{n,b}$ is 'off', while $k_n(t) = 0$ indicates that $SW_{n,t}$ is 'off' and $SW_{n,b}$ is 'on'. Thus, the dynamical model of the converter is:

$$\frac{dx(t)}{dt} = A(t)x(t) + Bu(t), \tag{4.1}$$

$$y(t) = Hx(t), \tag{4.2}$$

*Portions of this chapter are adapted from reference [30].

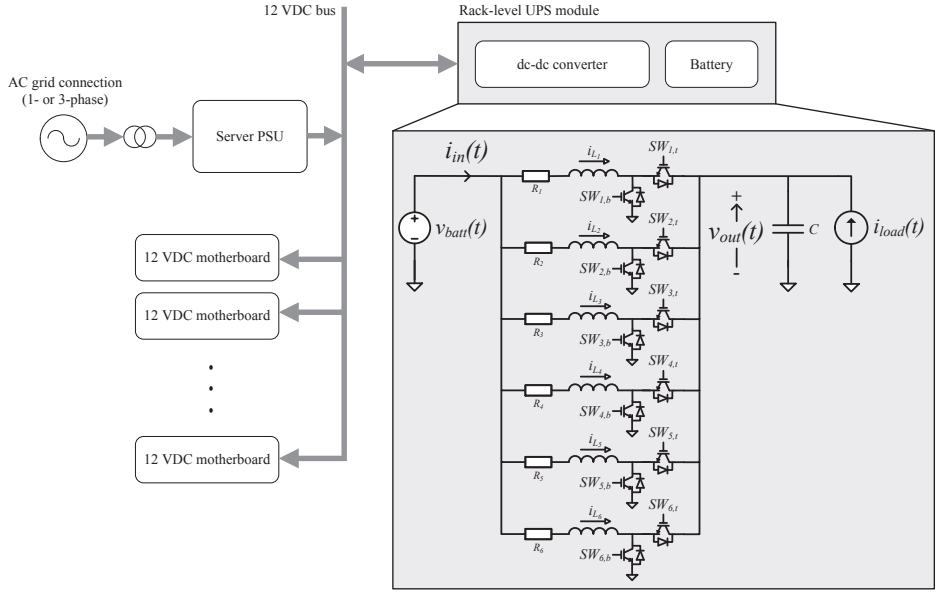


Figure 4.1: A data center power distribution network configuration. The converter topology of the rack-level UPS module is shown.

Table 4.1: Specifications for conveter experimental testbed.

Switching power converter	
Topology	6-phase boost converter
Rated output voltage	11.8 V
Rated output current	100 A
R_n	0.1 Ω
L_n	0.1 mH
C	400 μF
Battery pack	
Battery cell	K2 Energy LFP26650EV
Nominal v_{batt}	9.6 V
Pack capacity	25.6 A-h
Real-time computation platform	
FPGA device	Xilinx Virtex-6 ML605
Estimator solver time step	500 ns
Analog input sampling rate	1 MHz
PWM switching frequency	50 kHz

where

$$x(t) = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_3} \\ i_{L_4} \\ i_{L_5} \\ i_{L_6} \\ v_C \end{bmatrix}, u(t) = \begin{bmatrix} v_{batt}(t) \\ i_{load}(t) \end{bmatrix}, y(t) = \begin{bmatrix} i_{in}(t) \\ v_{out}(t) \end{bmatrix}$$

Table 4.2: Component fault in L_n causing ΔL change in inductance.

Component	ϕ_i	f_i
L_1	$\frac{R\Delta Li_{L_1}(t)+k_1(t)\Delta Lv_C(t)-\Delta Lv_{batt}(t)}{L(L+\Delta L)}$	$[1,0,0,0,0,0,0]^T$
L_2	$\frac{R\Delta Li_{L_2}(t)+k_2(t)\Delta Lv_C(t)-\Delta Lv_{batt}(t)}{L(L+\Delta L)}$	$[0,1,0,0,0,0,0]^T$
L_3	$\frac{R\Delta Li_{L_3}(t)+k_3(t)\Delta Lv_C(t)-\Delta Lv_{batt}(t)}{L(L+\Delta L)}$	$[0,0,1,0,0,0,0]^T$
L_4	$\frac{R\Delta Li_{L_4}(t)+k_4(t)\Delta Lv_C(t)-\Delta Lv_{batt}(t)}{L(L+\Delta L)}$	$[0,0,0,1,0,0,0]^T$
L_5	$\frac{R\Delta Li_{L_5}(t)+k_5(t)\Delta Lv_C(t)-\Delta Lv_{batt}(t)}{L(L+\Delta L)}$	$[0,0,0,0,1,0,0]^T$
L_6	$\frac{R\Delta Li_{L_6}(t)+k_6(t)\Delta Lv_C(t)-\Delta Lv_{batt}(t)}{L(L+\Delta L)}$	$[0,0,0,0,0,1,0]^T$

Table 4.3: Component fault in C causing ΔC change in capacitance.

Component	ϕ_i	f_i
C	$-\frac{\Delta C}{C(C+\Delta C)}i_{load}(t)-\sum_{n=1}^{6}\frac{\Delta Ck_n(t)}{C(C+\Delta C)}i_{L_n}(t)$	$[0,0,0,0,0,0,1]^T$

$$A(t)=\begin{bmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 & -\frac{k_1(t)}{L} \\ 0 & -\frac{R}{L} & 0 & 0 & 0 & 0 & -\frac{k_2(t)}{L} \\ 0 & 0 & -\frac{R}{L} & 0 & 0 & 0 & -\frac{k_3(t)}{L} \\ 0 & 0 & 0 & -\frac{R}{L} & 0 & 0 & -\frac{k_4(t)}{L} \\ 0 & 0 & 0 & 0 & -\frac{R}{L} & 0 & -\frac{k_5(t)}{L} \\ 0 & 0 & 0 & 0 & 0 & -\frac{R}{L} & -\frac{k_6(t)}{L} \\ \frac{k_1(t)}{C} & \frac{k_2(t)}{C} & \frac{k_3(t)}{C} & \frac{k_4(t)}{C} & \frac{k_5(t)}{C} & \frac{k_6(t)}{C} & 0 \end{bmatrix},$$

$$B=\begin{bmatrix} \frac{1}{L} & 0 \\ \frac{1}{L} & 0 \\ \frac{1}{L} & 0 \\ \frac{1}{L} & 0 \\ \frac{1}{L} & 0 \\ \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix},\ H=\begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

4.2 Fault modeling

Next, we model the dynamics of the system under faulted conditions. Consider a fault in the inductor L_n of the n^{th} phase of the converter that causes the value of the inductance to

change by a quantity ΔL. The fault manifests as an additive term ΔA and ΔB in $A(t)$ and B, respectively. Thus, the dynamics of the converter in the presence of this fault are:

$$\frac{dx(t)}{dt} = (A(t) + \Delta A)x(t) + (B + \Delta B)u(t) \tag{4.3}$$

With simple algebraic manipulation, we can rewrite (4.3) as the sum of (4.1) and the product of a scalar component fault magnitude function ϕ_i and a vector component fault signature f_i, that is:

$$\frac{dx(t)}{dt} = A(t)x(t) + Bu(t) + \phi_i f_i, \tag{4.4}$$

where, in the case $n = 1$,

$$\phi_i = \frac{R\Delta L i_{L_1}(t) + k_1(t)\Delta L v_C(t) - \Delta L v_{batt}(t)}{L(L + \Delta L)},$$
$$f_i = [1, 0, 0, 0, 0, 0, 0]^T$$

We can calculate ϕ_i and f_i for $n = 1...6$, as shown in Table 4.2. Similarly, we can use the same process to determine ϕ_i and f_i for faults that affect the capacitance of the output capacitor C and for faults in a switch pair that force $SW_{n,t} \rightarrow$ 'off' and $SW_{n,b} \rightarrow$ 'on'. The results of these derivations are shown in Tables 4.3 and 4.4.

Sensor faults manifest differently in the system dynamics than component faults. For example, consider the effect of a fault in the input current (i_{in}) sensor that causes a perturbation in the sensor gain ΔG_1 and in the sensor offset ΔE_1. The fault manifests as an additive term ΔH and ΔE_j in the output readout map as follows:

$$y(t) = (H + \Delta H)x(t) + \Delta E_j \tag{4.5}$$

We can rewrite (4.5) as the sum of (4.2) and the product of a scalar sensor fault magnitude function θ_j and a vector sensor fault signature g_j, that is:

$$y(t) = Hx(t) + \theta_j g_j \tag{4.6}$$

where

$$\theta_j = \Delta G_1(t) i_{in}(t) + \Delta E_1(t),$$
$$g_j = [1, 0]^T$$

We can use the same process to determine θ_j and g_j for faults in the output voltage sensor (v_{out}) as shown in Table 4.5.

Table 4.4: Fault in switch pair forcing $SW_{n,t} \rightarrow$ 'off' and $SW_{n,b} \rightarrow$ 'on'.

Component	ϕ_i	f_i
$SW_{1,t/b}$	$k_1(t)$	$[\frac{1}{L}v_C, 0, 0, 0, 0, 0, -\frac{1}{C}i_{L_1}]^T$
$SW_{2,t/b}$	$k_2(t)$	$[0, \frac{1}{L}v_C, 0, 0, 0, 0, -\frac{1}{C}i_{L_2}]^T$
$SW_{3,t/b}$	$k_3(t)$	$[0, 0, \frac{1}{L}v_C, 0, 0, 0, -\frac{1}{C}i_{L_3}]^T$
$SW_{4,t/b}$	$k_4(t)$	$[0, 0, 0, \frac{1}{L}v_C, 0, 0, -\frac{1}{C}i_{L_4}]^T$
$SW_{5,t/b}$	$k_5(t)$	$[0, 0, 0, 0, \frac{1}{L}v_C, 0, -\frac{1}{C}i_{L_5}]^T$
$SW_{6,t/b}$	$k_6(t)$	$[0, 0, 0, 0, 0, \frac{1}{L}v_C, -\frac{1}{C}i_{L_6}]^T$

Table 4.5: Fault in sensor affecting sensor gain and offset.

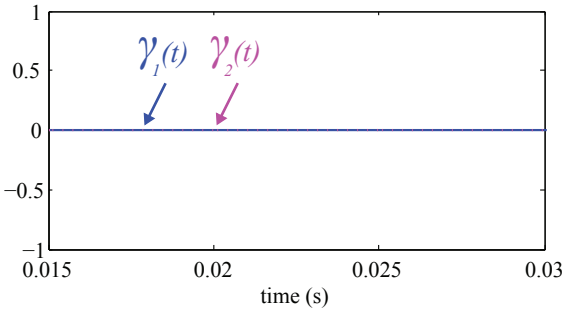
Sensor	θ_j	g_j
i_{in}	$\Delta G_1(t)i_{in}(t) + \Delta E_1(t)$	$[1, 0]^T$
v_{out}	$\Delta G_2(t)v_{out}(t) + \Delta E_2(t)$	$[0, 1]^T$

Table 4.6: Normalized fault signatures for component and sensor faults (note that $\xi = (\frac{v_C(t)^2}{L^2} + \frac{i_{L_n}(t)^2}{C^2})^{-\frac{1}{2}}$).

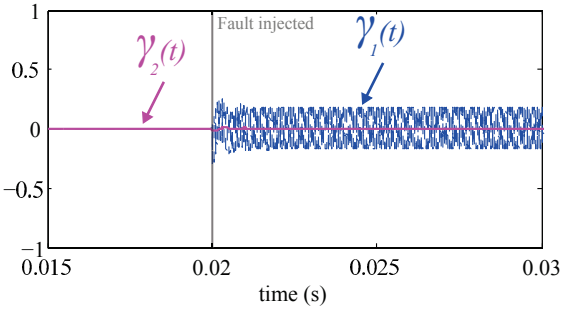
Faulted component	$\overline{Hf_i}$
L_n	$[1, 0]^T$
C	$[0, 1]^T$
$SW_{n,t/b}$	$\xi[\frac{v_C(t)}{L}, -\frac{i_{L_n}(t)}{C}]^T$
Faulted sensor	$\overline{g_j}$
i_{in}	$[1, 0]^T$
v_{out}	$[0, 1]^T$

4.3 Estimator design and implementation

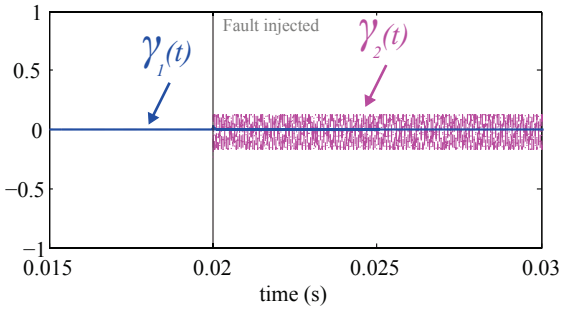
From Section 4.2, we see that the state space dynamics of the switching power converter contain valuable information, particularly the fault magnitude function and fault signature, that can be used to detect and identify faults. Thus, we propose a model-based estimator to extract these components from the measured outputs of the converter. Consider a switched



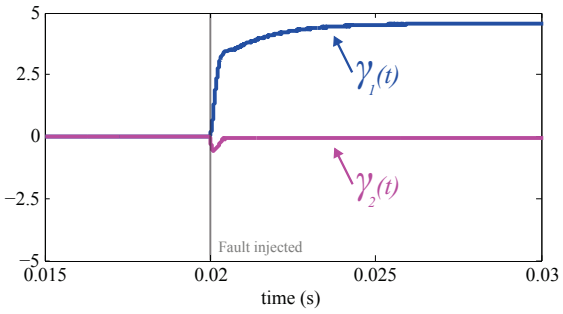
(a) Nominal (fault-free) response.



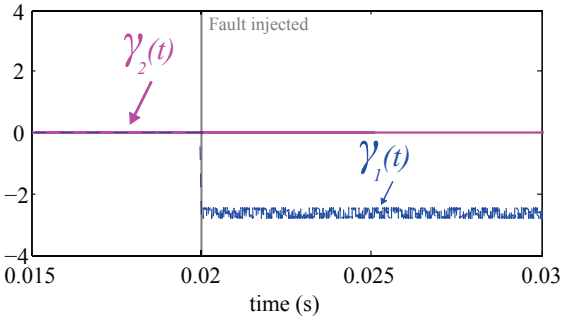
(b) Component fault causing 50 percent reduction of inductance L_6.



(c) Component fault causing 50 percent reduction of capacitance C.



(d) Fault in switch pair forcing $SW_{6,t}$ to 'off' and $SW_{6,b}$ to 'on'.



(e) Fault forcing sensor gain of i_{in} to zero.

Figure 4.2: Simulation of estimator response in nominal and component and sensor fault states.

linear estimator of the following form:

$$\frac{d\hat{x}(t)}{dt} = A(t)\hat{x}(t) + Bu(t) \tag{4.7}$$

$$\gamma(t) = y(t) - H\hat{x}(t) \tag{4.8}$$

where $\hat{x}(t)$ is an estimate of the state vector $x(t)$, $\gamma(t)$ is the error residual vector, and $A(t)$, B, and H are the state space matrices that describe the ideal converter dynamics. In some applications, one might use output injection to compensate for parameter uncertainty

and non-linearities that occur in $A(t)$, B, and H. However, in this case, we deliberately eschew this approach, and will demonstrate that these discrepancies naturally manifest as components of the fault magnitude function and fault signature.

The DC-DC converter and model-based estimator are simulated in MATLAB/Simulink using the Piecewise Linear Electrical Circuit Simulation (PLECS) toolbox [3].

Fig. 4.2a shows the nominal (fault-free) response of the error residual vector. Due to the modeled lossiness in the estimator and the natural lossiness in the converter, we have that the error residual vector is zero in steady state.

Next, we introduce faults in the converter and analyze the dynamics of the error residual vector. Using the analysis of the faulted response of the converter presented in Section 4.2, we can construct a *normalized fault signature*, which is the normalized vector function of Hf_i and g_j. The normalized fault signature, denoted as $\overline{Hf_i}$ for component faults and $\overline{g_j}$ for sensor faults, is an element of the output readout vector function space, as shown in Table 4.6. We take the L^2-inner product between the error residual vector and the set of all normalized fault signatures on an interval $[t-W, t]$, where W is the duration of the interval. We select W to be roughly ten switching cycles of the converter, which enables the inner product calculation to reach steady state in around 1 ms. For components faults, the inner product is:

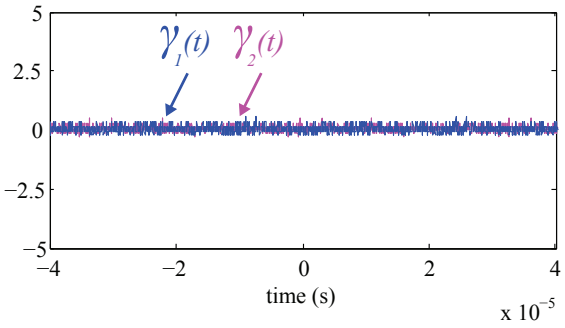
$$\langle \gamma(t), \overline{Hf_i} \rangle_{L^2} = \int_{t-W}^{t} \gamma^T(\tau) \overline{Hf_i}(\tau) \, \mathrm{d}\tau \tag{4.9}$$

Similarly for sensor faults, we have $\langle \gamma(t), \overline{g_j} \rangle_{L^2}$ on an interval $[t-W, t]$. In the presence of a fault, the result of the L^2-inner product will reveal the fault signature that $\gamma(t)$ most closely aligns with, and thus, enable fault identification.

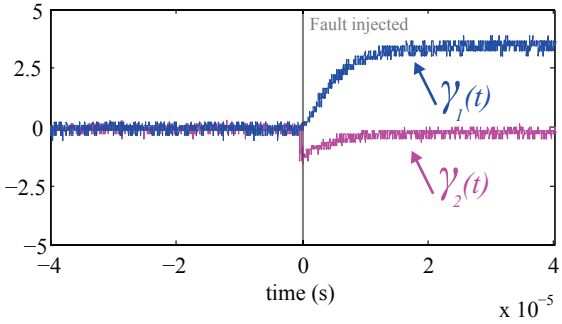
Consider a component fault causing the inductance of L_6 to reduce by 50 percent. From (4.4), we have that the faulted dynamics of $x(t)$ contain an additional term $\phi_i f_i$. Thus, from (4.8), the error residual vector will contain an additional component in the direction of $\overline{Hf_i} = [1, 0]^T$. Indeed, as shown in Fig. 4.2b, we see that when the fault is injected at $t = 0.02$ s, $\gamma_1(t)$ becomes nonzero and $\gamma_2(t)$ remains essentially zero.

We can follow a similar procedure to identify $\overline{Hf_i}$ for faults occurring in the output capacitor C and in the switch pair $SW_{n,t/b}$, as shown in Table 4.6. We see in Figs. 4.2c and 4.2d that in the faulted steady state, $\gamma(t)$ contains the respective $\overline{Hf_i}$ components.

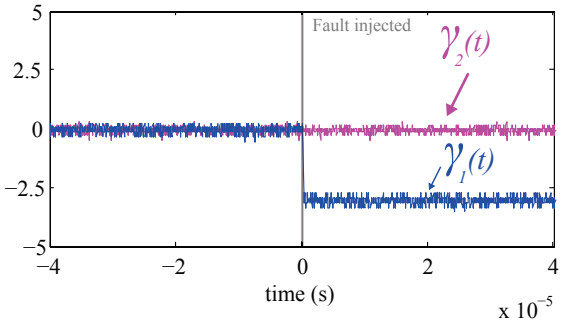
Now, consider a sensor fault that forces the sensor gain of i_{in} to zero. From (4.6), we see that the faulted dynamics of $y(t)$ contain an additional term $\theta_j g_j$. Thus, from (4.8), the error residual vector in steady state will contain an additional component in the direction of $\overline{g_j} = [1, 0]^T$. As shown in Fig. 4.2e, we see that when the fault is injected at $t = 0.02$ s, $\gamma_1(t)$ becomes nonzero and $\gamma_2(t)$ remains zero.



(a) Real-time nominal (fault-free) response.



(b) Fault in switch pair forcing $SW_{6,t} \rightarrow$ 'off' and $SW_{6,b} \rightarrow$ 'on'.



(c) Fault forcing sensor gain of i_{in} to zero.

Figure 4.3: Experimental results of real-time estimator response in nominal and component and sensor fault states.

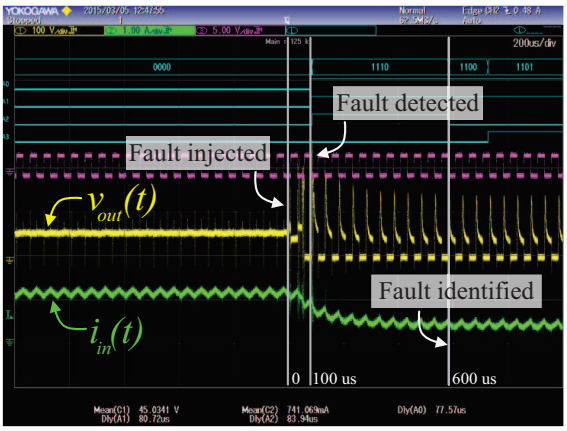
4.4 Real-time experimental implementation

In this section, we present an experimental implementation of the model-based estimator for fault diagnosis for the rack-level UPS module. The full specifications for the experimental testbed are presented in Table 4.1.

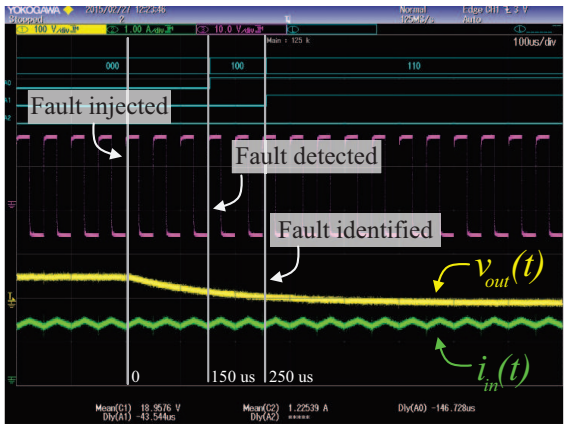
Real-time implementation on FPGA-based control platform

A single field programmable gate array (FPGA) device performs the converter control and solves the model-based estimator from (4.7) and (4.8) in real-time. The FPGA platform is designed for low-latency execution of switched linear state space models of switching power converters (see [25]).

The model-based estimator is solved in discrete time with a fixed 500 ns time step, including input-output latency. Measurements from the converter (i.e. $v_{batt}(t)$ and $i_{in}(t)$) are sampled with a 16-bit ADC at 1 MHz for control and estimation purposes. The FPGA generates a 50 kHz PWM signal for converter control (i.e. $k(t)$) with a 32-bit internal counter, which is directly passed to estimator computation.



(a) Fault detection and identification for a component fault in C.



(b) Fault detection and identification for a sensor fault in v_{out}.

Figure 4.4: Oscilloscope waveforms of experimental tests.

Table 4.7: Time to fault detection and identification for a set of sensor, component, and switch (input) faults.

	t_d (avg.)	t_i (avg.)
Sensor fault		
i_{in}	100 μs	2.5 ms
v_{out}	100 μs	200 μs
Component fault		
C	100 μs	600 μs
Switch (input) fault		
SW_n	100 μs	200 μs

4.5 Results and discussion

In this section, we present experimental results for various component, sensor, and input faults.

Generally, the time to fault detection is on the order of magnitude of the estimator solver time step (500 ns), as shown in Table 4.7. Fault identification for various component and sensor faults requires the L^2-inner product calculation whose solution reaches steady state in around 1 ms. Moreover, the fault diagnosis framework is flexible in that additional component and sensor faults can be accounted for by including the appropriate normalized fault signature.

Nominal (fault-free) response

We test the nominal (fault-free) response of the estimator as shown in Fig. 4.3a. As expected, the error residual vector remains essentially zero in steady state.

Switch fault

We inject a fault in the switch pair $SW_{6,t/b}$ that replicates the switch fault presented in Section 4.3, that is, $SW_{6,t} \rightarrow$ 'off' and $SW_{6,b} \rightarrow$ 'on' for all $t > 0$. The fault is injected into the converter using external MOSFETs that force conduction through the $SW_{6,b}$ path and prevent conduction through the $SW_{6,t}$ path. As shown in Fig. 4.3b, when the fault is injected at $t = 0$, the error residual vector $\gamma(t)$ becomes non-zero in 500 ns, which enables fault detection. Moreover, $\gamma(t)$ evolves in the direction of the normalized component fault signature $\overline{Hf_i}$ predicted in Table 4.6.

Sensor fault in i_{in}

We inject a fault that forces the sensor gain of i_{in} to zero, as in Section 4.3. As shown in Fig. 4.3c, when the fault is injected at $t = 0$, $\gamma_1(t)$ becomes nonzero in 500 ns and $\gamma_2(t)$ remains zero, as predicted by the normalized sensor fault signature $\overline{g_j}$ in Table 4.6.

Component fault in C

We inject a component fault that causes the capacitance of C to become zero. As shown in Fig. 4.4a, the fault causes a large ripple in the output voltage and also causes the input current to fall. The FDI system detects the fault in 100 μs, and identifies the fault in 600 μs.

Sensor fault in v_{out}

We inject a sensor fault that causes the gain of the v_{out} sensor to become zero. As shown in Fig. 4.4b, the fault causes the output voltage measurement to become zero. The FDI system detects the fault in 150 μs, and identifies the fault in 250 μs.

Chapter 5

Conclusions

In this thesis, we have demonstrated an approach to model-based fault detection and identification for switching power converters. The approach is experimentally implemented and validated for three different converter topologies that demonstrate the applicability of the FDI method for both distributed AC grid-connected systems and also distributed DC networked systems. To conclude, we will discuss promising areas of opportunity for research that can extend the work proposed in this thesis.

5.1 Future directions

Thus far, this work has focused exclusively on the fault detection and identification element of fault tolerance. Indeed, the ultimate goal is not simply to detect and identify faults, but to (1) design converters such that they are more reliable and fault tolerant, and (2) if faults occur, be able to remediate the fault either through hardware or control reconfiguration.

Fundamentally, then, an interesting opportunity for future research are efforts towards a unified model-based approach for *fault tolerance* in switching power converters; that is, using a linear-switched model of a switching power converter to *optimally* design fault tolerance into a converter subject to constraints such as cost or number of sensors available.

Fault tolerant converter design

By using the linear-switched model of a switching power converter, one can analytically determine characteristics of the converter, such as controlability and observability in the absence or presence of various faults. An interesting research question is whether there is a closed-form method to optimally design a converter to be fault tolerant with respect to particular faults. Clearly, constraints in this case would be the number of components or sensors in a particular converter design. If such an analytic solution is not possible, then a probabilistic or Monte Carlo-type simulation could potentially reveal useful insights.

A 'safe control' strategy for optimal fault remediation

The proposed linear-switched modeling approach enables us to accurately describe the dynamics of a switching power converter. The fidelity of these models is particularly advantageous when developing control strategies for either non-faulty and faulty modes of operation. For instance, in [11], the authors propose a 'safe control' strategy that analytically determines an optimal control strategy given a set of state constraints. Such an approach could be useful to determine control strategies for optimal control and for fault remediation.

Bibliography

[1] M. Abul Masrur, Z. Chen, and Y. Murphey. "Intelligent diagnosis of open and short circuit faults in electric drive inverters for real-time applications". In: *IET Power Electronics* 3.2 (2010), pp. 279 –291. ISSN: 1755-4535.

[2] A. Alessandri and P. Coletta. "Design of Luenberger Observers for a Class of Hybrid Linear Systems". In: *Proc. Hybrid Systems Computation and Control*. Genova, Italy, 2001.

[3] J.H. Alimeling and W.P. Hammer. "PLECS-piece-wise linear electrical circuit simulation for Simulink". In: *Proc. of IEEE International Conference on Power Electronics and Drive Systems*. Hong Kong, 1999. DOI: 10.1109/PEDS.1999.794588.

[4] R.L. de Araujo Ribeiro, C.B. Jacobina, E.R.C. da Silva, and A.M.N. Lima. "Fault detection of open-switch damage in voltage-fed PWM motor drive systems". In: *IEEE Transactions on Power Electronics* 18.2 (2003), pp. 587 –593. ISSN: 0885-8993. DOI: 10.1109/TPEL.2003.809351.

[5] Subhes C. Bhattacharyya. "Review of alternative methodologies for analysing off-grid electricity supply". In: *Renewable and Sustainable Energy Reviews* 16.1 (Jan. 2012), pp. 677–694.

[6] Dushan Boroyevich, Igor Cvetkovic, Dong Dong, Rolando Burgos, Fei Wang, and Fred Lee. "Future electronic power distribution systems a contemplative view". In: *2010 12th International Conference on Optimization of Electrical and Electronic Equipment*. IEEE, May 2010, pp. 1369–1380. ISBN: 978-1-4244-7019-8. DOI: 10.1109/OPTIM.2010.5510477. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5510477.

[7] F. Chowdhury and J. Aravena. "A modular methodology for fast fault detection and classification in power systems". In: *IEEE Transactions on Control Systems Technology* 6.5 (1998), pp. 623–634.

[8] X. Ding, J. Poon, I. Celanovic, and A.D. Dominguez-Garcia. "Fault Detection and Isolation Filters for Three-Phase AC-DC Power Electronics Systems". In: *Circuits and Systems I: Regular Papers, IEEE Transactions on* 60.4 (2013), pp. 1038–1051. ISSN: 1549-8328. DOI: 10.1109/TCSI.2012.2221222.

[9] Zhaohao Ding, Meng Liu, Wei-Jen Lee, and David Wetz. "An autonomous operation microgrid for rural electrification". In: *2013 IEEE Industry Applications Society Annual Meeting*. IEEE, Oct. 2013, pp. 1–8. ISBN: 978-1-4673-5202-4. DOI: 10.1109/IAS.2013.6682482. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6682482.

[10] *Energy for all: financing access for the poor*. Tech. rep. IEA World Energy Outlook, 2011. URL: http://www.iea.org/publications/worldenergyoutlook/resources/energydevelopment/energyforallfinancingaccessforthepoor/.

[11] Jaime F. Fisac, Mo Chen, Claire J. Tomlin, and S. Shankar Sastry. "Reach-avoid Problems with Time-varying Dynamics, Targets and Constraints". In: *Proceedings of the 18th International Conference on Hybrid Systems: Computation and Control*. HSCC '15. Seattle, Washington: ACM, 2015, pp. 11–20. ISBN: 978-1-4503-3433-4. DOI: 10.1145/2728606.2728612. URL: http://doi.acm.org/10.1145/2728606.2728612.

[12] N. Hingorani and L. Gyugyi. *Understanding FACTS (Concepts and Technology of Flexible AC Transmission Systems)*. Hoboken, NJ: IEEE Press, 1999.

[13] Wei Jiang and Yu Zhang. "Load Sharing Techniques in Hybrid Power Systems for DC Micro-Grids". In: *Power and Energy Engineering Conference (APPEEC), 2011 Asia-Pacific* (2011), pp. 1–4.

[14] Linda Kamas and Seth Sanders. "Parameter and State Estimation in Power Electronics Circuits". In: *IEEE Transactions on Circuits and Systems* 40.12 (1993), pp. 920–928.

[15] John G. Kassakian, Martin Schlecht, and George C Verghese. *Principles of Power Electronics*. Addison-Wesley, 1991.

[16] S. Khomfoi and L.M. Tolbert. "Fault Diagnostic System for a Multilevel Inverter Using a Neural Network". In: *IEEE Transactions on Power Electronics* 22.3 (2007), pp. 1062–1069. ISSN: 0885-8993. DOI: 10.1109/TPEL.2007.897128.

[17] J. Koomey. "Growth in Data center electricity use 2005 to 2010". Oakland, CA, 2011. URL: http://www.analyticspress.com/datacenters.html.

[18] J. Laprie. *Dependability: Basic Concepts and Terminology*. New York, NY: Springer-Verlag, 1991.

[19] K.T. Levin, E.M. Hope, and A.D. Domínguez-García. "Observer-based fault diagnosis of power electronics systems". In: *Proceedings of IEEE Energy Conversion Congress and Exposition*. Atlanta, GA, 2010.

[20] Todd Levin and Valerie M Thomas. "Least-cost network evaluation of centralized and decentralized contributions to global electrification". In: *Energy Policy* 41.C (Feb. 2012), pp. 286–302.

[21] D. Liberzon. *Switching in Systems and Control*. Boston, MA: Birkhauser, 2003.

[22] P. Achintya Madduri, Javier Rosa, Seth Sanders, Eric Brewer, and Matthew Podolsky. "Design and verification of smart and scalable DC microgrids for emerging regions". In: *2013 IEEE Energy Conversion Congress and Exposition* (Sept. 2013), pp. 73–79. DOI: 10.1109/ECCE.2013.6646683. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6646683.

[23] P.A. Madduri, J. Poon, J. Rosa, M. Podolsky, E. Brewer, and S. Sanders. "A scalable dc microgrid architecture for rural electrification in emerging regions". In: *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*. 2015, pp. 703–708. DOI: 10.1109/APEC.2015.7104427.

[24] J. Mahdavi, A. Emaadi, M.D. Bellar, and M. Ehsani. "Analysis of power electronic converters using the generalized state-space averaging approach". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 44.8 (1997), pp. 767 –770. ISSN: 1057-7122. DOI: 10.1109/81.611275.

[25] Dusan Majstorovic, Ivan Celanovic, Nikola Dj. Teslic, Nikola Celanovic, and Vladimir A. Katic. "Ultralow-latency hardware-in-the-loop platform for rapid validation of power electronics designs". In: *IEEE Transactions on Industrial Electronics* 58.10 (Oct. 2011), pp. 4708–4716. ISSN: 0278-0046. DOI: 10.1109/TIE.2011.2112318. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5762345.

[26] T. Manmek, C.P. Mudannayake, and C. Grantham. "Voltage Dip Detection Based on an Efficient Least Squares Algorithm for D-STATCOM Application". In: *Proc. of CES/IEEE Power Electronics and Motion Control Conference*. Shanghai, China, 2006. DOI: 10.1109/IPEMC.2006.4778182.

[27] M. Nouni, S. Mullick, and T. Kandpal. "Providing electricity access to remote areas in India: An approach towards identifying potential areas for decentralized electricity supply". In: *Renewable & Sustainable Energy Reviews* 12.5 (June 2008), pp. 1187–1220.

[28] Ron J. Patton, Paul M. Frank, and Robert N. Clarke, eds. *Fault diagnosis in dynamic systems: theory and application*. Upper Saddle River, NJ, USA: Prentice-Hall, Inc., 1989. ISBN: 0-13-308263-6.

[29] R. Peuget, S. Courtine, and J.-P. Rognon. "Fault detection and isolation on a PWM inverter by knowledge-based model". In: *IEEE Transactions on Industry Applications* 34.6 (1998), pp. 1318 –1326. ISSN: 0093-9994.

[30] J. Poon, I.C. Konstantakopoulos, C. Spanos, and S.R. Sanders. "Real-time model-based fault diagnosis for switching power converters". In: *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*. 2015, pp. 358–364. DOI: 10.1109/APEC.2015.7104375.

[31] G.F. Reed, M. Takeda, and I. Iyoda. "Improved power quality solutions using advanced solid-state switching and static compensation technologies". In: *Proc. of IEEE Power Eng. Society Winter Meeting*. New York, NY, USA, 1999. DOI: 10.1109/PESW.1999.747364.

[32] Seth Sanders and George C. Verghese. "Lyapunov based control for switching power converters". In: *IEEE Transactions on Power Electronics* 7.1 (1992), pp. 17–24.

[33] D. Soto and V. Modi. "Simulations of Efficiency Improvements Using Measured Microgrid Data". In: *Global Humanitarian Technology Conference (IGHTC), 2012 IEEE* (2012), pp. 369–374.

[34] Daniel Soto, Edwin Adkins, Matt Basinger, Rajesh Menon, Sebastian Rodriguez-Sanchez, Natasha Owczarek, Ivan Willig, and Vijay Modi. "A prepaid architecture for solar electricity delivery in rural areas". In: *Proceedings of the Fifth International Conference on Information and Communication Technologies and Development - ICTD '12*. New York, New York, USA: ACM Press, Mar. 2012, p. 130. ISBN: 9781450310451. DOI: 10.1145/2160673.2160691. URL: http://dl.acm.org/citation.cfm?id=2160673.2160691.

[35] Leena Srivastava and I. H. Rehman. "Energy for sustainable development in India: Linkages and strategic direction". In: *Energy Policy* 34.5 (Mar. 2006), pp. 643–654.

[36] A. Tanwani, A.D. Dominguez-Garcia, and D. Liberzon. "An Inversion-Based Approach to Fault Detection and Isolation in Switching Electrical Networks". In: *IEEE Transactions on Control Systems Technology* 19.5 (2011), pp. 1059 –1074. ISSN: 1063-6536. DOI: 10.1109/TCST.2010.2067214.

[37] C. Turpin, P. Baudesson, F. Richardeau, F. Forest, and T.A. Meynard. "Fault management of multicell converters". In: *IEEE Transactions on Industrial Electronics* 49.5 (2002). ISSN: 0278-0046.

[38] A. Yazdani, H. Sepahvand, M.L. Crow, and M. Ferdowsi. "Fault Detection and Mitigation in Multilevel Converter STATCOMs". In: *IEEE Transactions on Industrial Electronics* 58.4 (2011), pp. 1307–1315. ISSN: 0278-0046. DOI: 10.1109/TIE.2010.2050415.

[39] D. Zhang, F. Wang, R. Burgos, J. Kern, S. El-Barbari, and D. Boroyevich. "Internal Fault Detection and Isolation for Paralleled Voltage Source Converters". In: *Proc. of IEEE Applied Power Electronics Conference and Exposition*. Washington, DC, 2009.

[40] Li Zhang, Tianjin Wu, Yan Xing, Kai Sun, and Josep. M Gurrero. "Power control of DC microgrid using DC bus signaling". In: *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, Mar. 2011, pp. 1926–1932. ISBN: 978-1-4244-8084-5. DOI: 10.1109/APEC.2011.5744859. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5744859.

[41] Wei Zhang, Dong Dong, I. Cvetkovic, F. Lee, and D. Boroyevich. "Lithium-based energy storage management for DC distributed renewable energy system". In: *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* (2011), pp. 3270–3277.