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ELECTRICAL TRANSPORT PROPERTIES AND FIELD EFFECT TRANSISTORS OF CARBON NANOTUBES

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This paper presents a review on our recent work on carbon nanotube field effect transistors, including the development of ohmic contacts, high-κ gate dielectric integration, chemical functionalization for conformal dielectric deposition and pushing the performance limit of nanotube FETs by channel length scaling. Due to the importance of high current operations of electronic devices, we also review the high field electrical transport properties of nanotubes on substrates and in freely suspended forms. Owing to their unique properties originating from their crystalline 1D structure and the strong covalent carbon–carbon bonding configuration, carbon nanotubes are highly promising as building blocks for future electronics. They are found to perform favorably in terms of ON-state current density as compared to the existing silicon technology, owing to their superb electron transport properties and compatibility with high-κ gate dielectrics. Future directions and challenges for carbon nanotube-based electronics are also discussed.

Keywords: Carbon nanotubes; FETs; ballistic transport; phonon scattering; thermal transport; contacts.

1. Introduction

Much progress has been made recently showing that single-walled carbon nanotubes (SWNTs) are advanced quasi-1D materials for future high performance electronics.[1–8] SWNT field effect transistors (FETs) can outperform state-of-the-art silicon FETs owing to near ballistic electrical transport, chemical robustness, lack of surface dangling bonds and sustained electrical properties when integrated into realistic device structures. The strong covalent C–C bonding and lack of surface dangling bonds are the fundamental reasons underlying the advanced properties of carbon nanotubes and high potential for future electronics. In this review, we present our recent progress in developing Ohmic contacts, gate dielectric integration and channel length scaling for SWNT FETs.

Ever since the beginning of the integrated circuit era, aggressive scaling of the device elements has been actively pursued in order to increase the speed and density. The end of this "evolutionary" path, however, is only a decade or so away due to the physical and technical limitations of the current technologies. Beyond this scaling limit, short channel effects and high leakage currents severely degrade the performance of the conventional devices so that they can no longer operate properly.[9] "Revolutionary" concepts, therefore, need to be developed for further miniaturization of digital components down to the molecular scales.

As the conventional CMOS technology reaches its scaling limit, many have approached novel

concepts, such as nanotube-based electronics, as alternatives. Carbon nanotubes are molecular-scale (~ 1 nm diameter) wires with atomically well-defined structures.[1−3] They are ideal for elucidating basic phenomena in 1D and have been proposed as the potential building blocks for future nanoelectronics. SWNTs can be thought of as 2D graphene sheets that are wrapped around to form 1D cylinders.[1−3] They are composed of only C–C sp^2 bonds, which are among the strongest chemical bonds, making them unique structures that are chemically inert, electrically stable, and mechanically robust. With diameters $d = 0.5$–5 nm and lengths $L = \sim 10$ nm to ~ 1 cm, nanotubes are perhaps the closest known materials to ideal 1D structures. Nanotubes are mainly characterized by their wrapping vector $\mathbf{R}_{nm} = (n, m) = n\mathbf{a_1} + m\mathbf{a_2}$, which refers to the folding of the graphene sheet as shown in Fig. 1(a). The wrapping vector governs the electrical characteristics of nanotubes, which can be either metallic or semiconducting (Figs. 1(b) and 1(c)) with band gaps inversely proportional to the diameter.[1−3] There are virtually unlimited number of possibilities for the chirality and diameter combination of nanotubes, making them a novel *class* of materials with a wide spectrum of properties and potential applications in electronics.

2. Achieving Zero Schottky Barrier Metal Contacts for Nanotube FETs

SWNT FETs were first demonstrated by Dekker and coworkers,[10] and by researchers at IBM[11] and Stanford.[12] Like any materials for potential electronic applications, achieving Ohmic contacts is the key to high device performance. The existence of "barriers" (not specifically named "Schottky barriers") between metal contacts and SWNTs, and the resulting thermally activated transport were initially reported by Zhou *et al.*[13] A correlation between the barrier height and SWNT diameter was also noted.[13] Later, systematic work by researchers

(a)

(10,10)
armchair
metallic

(11,7)
chiral
semiconductor
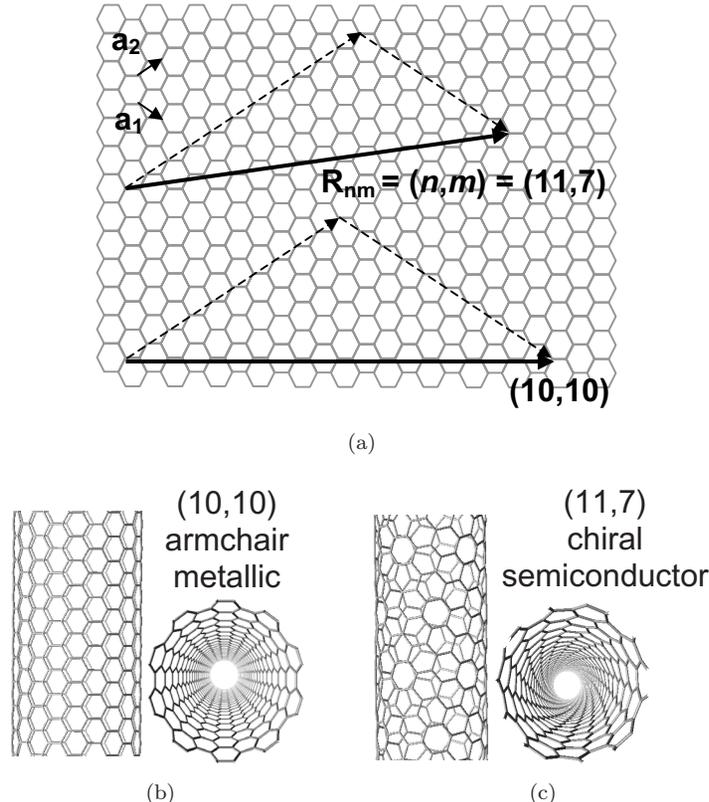
(b)   (c)

Fig. 1.   Folding of graphene into nanotubes. (a) Various chiralities of carbon nanotubes can be obtained by folding along different wrapping vectors $\mathbf{R}_{nm}$. (b) and (c) are schematics of $(10, 10)$ and $(11, 7)$ nanotubes. A (n, m) tube is metallic when $n = m$ (armchair). A nanotube with $n - m = 3j$, where j is an integer, is a semi-metal with a curvature-induced band gap on the order of few meV. A nanotube is semiconducting when $n - m \neq 3j$.

at IBM further established the existence of Schottky barriers (SBs) between SWNTs and metals (e.g., Ti).[14] It is now well accepted that in many cases, SBs exist between metal contacts and quasi 1D SWNT semiconductors. How to overcome, reduce or eliminate this barrier to achieve Ohmic contacts to semiconducting nanotubes has been actively pursued by researchers in recent years. Progress has been made but challenges remain.

In order to understand the intrinsic electron transport physics of carbon nanotubes and explore their device performance limits, it is essential to form near-Ohmic contacts without any significant scattering or energy loss of the carriers at the source/drain (S/D) interfaces. It is difficult to form Ohmic metal contacts to intrinsic planar Si channels due to the Fermi-level pinning. It is widely believed that the metal-induced gap states (MIGS) at the metal–semiconductor interfaces, which result in planar dipoles, pin down the Schottky barrier (SB) heights and make them nearly independent of the contact metal work function.[15] For a 1D channel, such as carbon nanotubes, however, the dipole layer that is created at the metal–channel interface due to MIGS has a "molecular" scale (nearly 0D) with different electrostatics than the planar dipoles.[16] Unlike the planar dipoles where the potential is constant outside of the dipole layer, in "molecular"-scale dipoles, the potential decays to zero in regions far away from the S/D interfaces. As a result, in 1D nanotube devices, MIGS do not induce a strong pinning of the Fermi-level, and therefore the Schottky barrier heights are primarily governed by the energy difference of the work function of the metal contacts and the conduction/valance band edge of the nanotubes.

Based on this principle, zero SB contacts to the valence band of chemically intrinsic nanotubes with diameter $d > \sim 1.6$ nm (band gap $E_g < \sim 0.6$ eV) have been experimentally demonstrated using high work function palladium (Pd, $\Phi_m \sim 5.0$ eV) as the electrode material (Figs. 2(a) and 2(b)). These
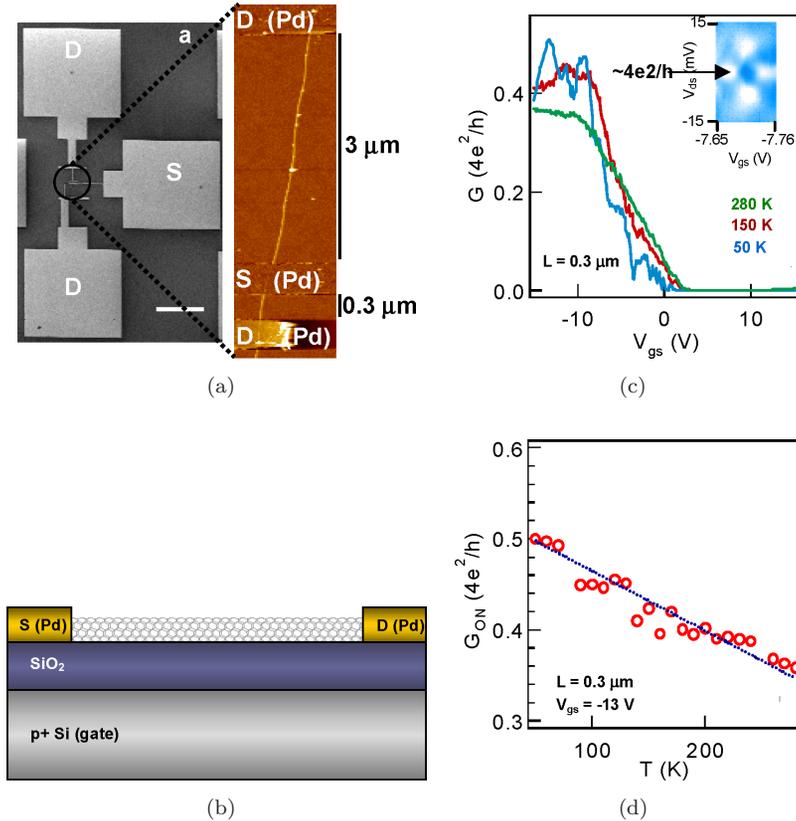

Fig. 2. Pd-contacted and back-gated SWNT-FETs on Si/SiO$_2$ ($t_{ox} \sim 500$ nm) substrates. (a) Scanning electron microscopy (SEM, left) and atomic force microscope (AFM, right) images of a SWNT bridging three Pd contacts. (b) Schematic view of a device. (c) Transconductance G versus V_{gs} for a 300-nm long tube device at various temperatures. Differential conductance dI_{ds}/dV_{ds} versus V_{ds} and V_{gs} (inset) at $T = 1.5$ K shows a Fabry–Perot-like interference pattern, a hallmark of ballistic transport. (d) ON-state conductance as a function of temperature for the same device.

nanotubes are capable of delivering high current (μA) densities at relatively low bias voltages.[5] The ON-state of the Pd-contacted p-FETs exhibits metallic-like behavior, with the low-bias conductance linearly increasing as the temperature is lowered due to the freezing of acoustic phonons (Figs. 2(c) and 2(d)). At cryogenic temperatures, the ON-state conductance approaches the quantum conductance limit of $G_0 = 4e^2/h$ (Fig. 2(c) inset), implying a ballistic device without any significant scattering of the carriers in the nanotube channel or at the S/D contact interfaces. This is in clear contrast to the SWNT SB-FETs (for example, Ti-Ni- and Cr-contacted FETs) that become nearly insulating at low temperatures as the thermionic emission and thermally assisted-tunneling components of the carrier injection vanish. The lack of positive Schottky barriers at the contacts is a critical step for achieving state-of-the-art SWNT FETs that operate near the performance limit of an ideal 1D system.

It is well established that the surface work function of Pd can be reversibly modified upon exposure to molecular hydrogen. Hydrogen molecules dissociate at the surface of Pd, resulting in atomic hydrogen that can dissolve in Pd and lower its work function. This phenomenon has been utilized to modify the metal contact work function of nanotube FETs *in situ* and shed light on the SB height nature at the interfaces.[5] Figure 3 shows the transfer characteristics of a Pd-contacted nanotube device upon exposure to various concentrations of H_2 in dry air. It is evident that as the concentration of H_2 is increased and therefore the Pd work function is decreased, the p-channel (n-channel) conductance decreases (increases) due to the Schottky barrier height modulation at the Pd–nanotube interfaces (Fig. 3). This result provides a clear experimental proof of the lack of Fermi-level pinning at the interfaces and demonstrates the large sensitivity of Schottky barrier height on the work function of the metal contacts.

3. Metal Type and Diameter Dependence of Electrical Contacts to Carbon Nanotubes

Recently, we have found that Rh can afford similar contact interfaces to nanotubes as Pd.[17] While near-zero SB contacts can be made to $d > \sim 1.6$ nm semiconducting nanotubes with Pd or Rh metal
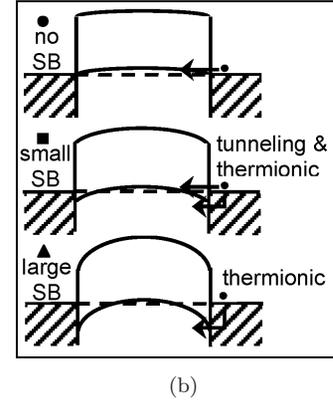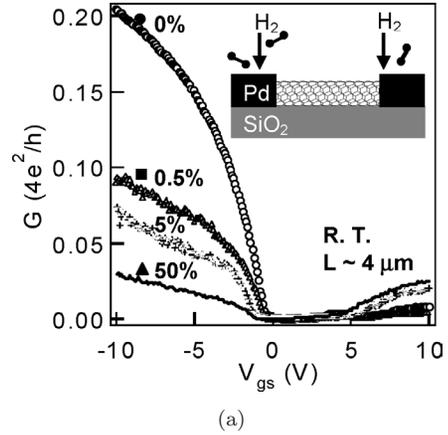

(a)

(b)

Fig. 3.   Shedding light into metal-SWNT contacts by *in situ* metal work function modification. (a) Linear conductance (G) versus V_{gs} for a SWNT-FET before and after the pure Pd contacts were exposed to various concentrations of H_2. (b) Schematic ON-state (for p-channel) band diagrams for the device under various H_2 concentrations, depicting the development of SBs to the valence band for higher and lower Pd workfunction (caused by dissolution of H_2 in Pd). The symbols in the diagrams (solid circle, square and triangle) correspond to those used in (a) to label the ON-state gate voltages.

contacts, non-negligible positive SBs exist for smaller diameter nanotubes due to their larger band gap (Fig. 4). Metal type and diameter-dependent contacts to semiconducting SWNTs have also been investigated by Chen *et al.*[18] Beside the Schottky barriers, pure tunneling barriers (gate-independent) may also develop at the metal–nanotube interface, therefore, limiting the ON-state conductance and current drive of a device. These pure tunneling barriers can be observed when metal–nanotube bonding interactions are weak and the relaxation bond lengths are large. As a result, charge carriers have to tunnel through a "vacuum" interface between the metal and nanotube. Experimental observations have shown that Pd and Rh are favorable as contact
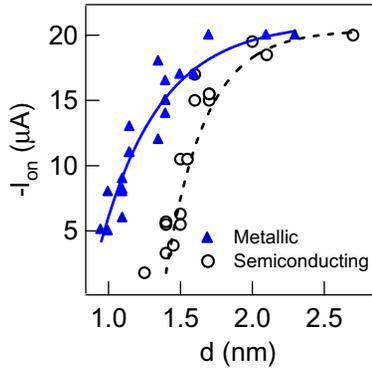
Fig. 4. Diameter-dependent electrical properties of metallic and semiconducting SWNTs. Room temperature I_{on} (defined as the current under $|V_{ds}| = 1$ V) versus d plots for both metallic and semiconducting SWNT devices with Rh or Pd contact (similar results for both metals).

materials over other high work function metals such as Au and Pt. This may in fact be due to the larger bonding interactions between Pd/Rh and nanotube as compared to Pt and Au, although more detailed experimental and theoretical work is still needed to better understand the precise nature of this observation.

A surprising observation is that the contact resistance between Pd/Rh electrodes and metallic nanotub es is also found to be diameter-dependent for small nanotubes (Fig. 4).[17] Since there are no SBs at the interface for zero band gap metallic nanotubes, the low current drive for $d \leq \sim 1.0$ nm nanotubes is attributed to the development of pure tunneling barriers as the chemical reactivity of nanotubes is known to be diameter-dependent. The existence of SBs for small semiconducting SWNTs is responsible for lower currents than in same-diameter metallic tubes. Chemical doping can be invoked to suppress the positive SBs as demonstrated experimentally.[19] However, the tunnel barrier appears to be independent of doping and causes non-Ohmic contact for $d < 1.2$ nm SWNTs (for semiconducting and metallic tubes alike) even under chemical doping. Little is known currently about how to suppress this contact barrier for such small diameter SWNTs. The origin of this tunnel barrier could be coming from significant alteration of the SWNT structure due to chemical perturbations by the contact metal, that is, small nanotubes are chemically more reactive than larger tubes, and the interaction with metal atoms may give rise to invasive contact effects that lead to degradation of the transport properties of the nanotubes at the

electrodes. This possibility however, requires further investigation.

Making Ohmic contacts to very small ($d \leq 1$ nm) nanotubes is currently a key challenge and requires developing a strategy to eliminate the large electrode tunnel barriers. Various chemical synthesis methods including HiPco[20] and CoMo[21] are known to produce very small tubes predominantly in the 0.7–1.2 nm range. An Ohmic contact solution for down to 0.7 nm tubes will be needed in order to enable high performance electronics with these materials. To achieve this goal, systematic experiments and theoretical understanding will be needed, including continued search for an optimum contact material.

4. High-κ Dielectric Integration

Thin films of high-κ materials, such as ZrO_2 and HfO_2 ($\kappa \sim 15$–25), are highly desirable for gate dielectric integration in field effect transistors as they enable high ON-state current densities (speed) and low operating power consumptions. The integration of high-κ dielectrics, however, has been a challenge in planar MOSFETs because of the inherent mobility degradation of the Si channels. A unique advantage of carbon nanotubes is their compatibility with high-κ dielectrics. The lack of dangling bonds at the nanotube/high-κ interface and the weak noncovalent bonding interactions between the two materials, prevent any large perturbation of electron transport in carbon nanotubes.[4]

Figure 5 shows TEM images of suspended (a) and on substrate (b) carbon nanotubes after atomic layer deposition (ALD) of ~ 8 nm thick high-κ film. It is evident that high-κ materials do not nucleate on pristine carbon nanotubes,[6] except at defect sites (Fig. 5(a)). For nanotube devices on substrates, the ALD of high-κ dielectrics initiates on the surrounding SiO_2 substrate and "drowns" the nanotubes once the thickness of the film surpasses the diameter of the nanotube (Fig. 5(b)). As a result, the interface bonding between nanotubes and the high-κ dielectric is only through weak van der Waals forces, and the intrinsic chemical and physical nature of the nanotubes are well preserved after ALD. However, since as-grown SWNT-derived FETs with high-κ dielectrics rely on ALD nucleation and growth on OH-terminated SiO_2 substrates, ALD of relatively thick high-κ films (≥ 8 nm) are needed to fully cover the SWNTs and avoid gate leakage.
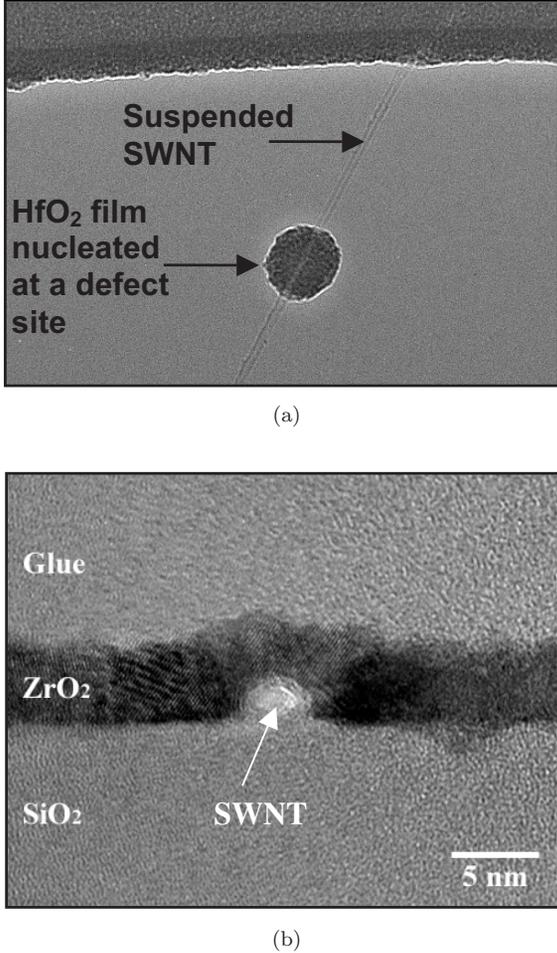
(a)

(b)

Fig. 5.   TEM images of (a) suspended and (b) on SiO_2 substrate SWNTs after atomic deposition ALD of high-κ dielectrics.

Recently, we found that by noncovalent functionalization of SWNTs with ploy-T DNA molecules (dT40), one can impart functional groups of sufficient density and stability for uniform and conformal ALD of high-κ dielectrics with thickness down to 2–3 nm on SWNTs (Fig. 6).[22] This enables us to approach the ultimate vertical scaling limit of nanotube FETs and reliably achieve $S \sim 60$ mV/decade at room temperature (Fig. 7). For nanotube FETs without DNA functionalization, severe gate leakage and shorts were observed for most FETs with high-κ thickness $t_{ox} \leq 5$ nm. With DNA functionalization, high performance nanotube/high-κ FETs were reliably obtained with HfO_2 down to $t_{ox} \sim 2$ nm (Fig. 7). These DNA functionalized SWNT FETs reproducibly reached the theoretical limit of $S \sim 60$ mV/decade at 300 K (Fig. 7(a)).[22] With noncovalent DNA functionalization, we observed no degradation in the SWNT FET

conductance after the functionalization and subsequent ALD.

We have carried out microscopy investigations to understand ALD processes on SWNTs with and without DNA functionalization (Fig. 6). For SWNTs on SiO_2 substrates with DNA functionalization, we observed concurrent ALD of HfO_2 on both nanotube and SiO_2 surfaces, evidenced by the post-ALD topographic height difference between the nanotube site and surrounding being approximately the tube diameter d (Fig. 6(a) left panel). In contrast, for SWNTs on SiO_2 without DNA functionalization, "grooves" were observed along the nanotubes after ALD of HfO_2 (Fig. 6(a) right panel), indicating the lack of nucleation and growth of HfO_2 directly on the tube surface and engulfing of the tube by HfO_2 grown on the SiO_2. We also carried out ALD on suspended SWNTs grown on transmission electron microscopy (TEM) grids. With DNA functionalization, suspended SWNTs allowed for quasi-continuous and conformal HfO_2 coating by ALD (Fig. 6(b) left image). This differed from "balling up" of high-κ material locally on as-grown tubes presumably on defect site (Fig. 6(b) right image).[6,23]

Our microscopy data provides direct evidence of active nucleation and growth of HfO_2 on the sidewalls of DNA functionalized SWNTs in ALD. DNA is known to noncovalently absorb[24] on SWNT sidewalls via π-stacking[25] of the base-pairs. This functionalization is found to be thermally stable at the ALD temperature of 90°C. The functional groups in DNA molecules (OH, phosphate, etc) are involved in chemisorption of precursor species in the ALD process, affording uniform nucleation and growth of HfO_2 coating on nanotubes.

The vertical scaling of high-κ dielectrics for SWNT FETs is expected to be useful for investigating interesting device physics in quasi-1D systems such as electron tunneling. In a 1D channel, electrostatics are dependent on the gate dielectric thickness and the widths of tunnel barriers (Schottky, band-to-band tunneling BTBT,[26,27] etc) are often set by the gate dielectrics thickness.[28]

5.   Approaching the Performance Limit — Nearly Ballistic Nanotube FETs

To explore the potential of nanotube building blocks for nanoelectronic applications, it is essential to explore their performance limit and compare it
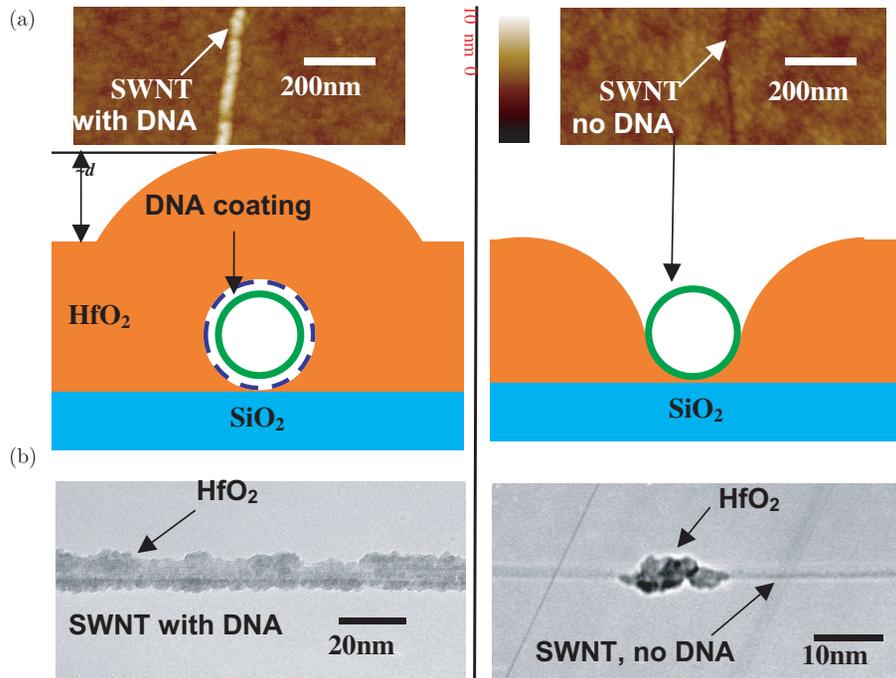
Fig. 6. ALD of HfO$_2$ on SWNTs with and without DNA functionalization. (a) AFM images of ~ 5 nm thick HfO$_2$ coatings on SWNTs lying on SiO$_2$ with (left image) and without (right side) DNA functionalization prior to ALD. Cross-sectional view schematics of the coating profiles are shown under images. (b) TEM images of nominally 5 nm thick ALD-HfO$_2$ coating on suspended SWNTs with (left) and without (right) DNA functionalization, respectively. Note that the uniformity of high-κ coatings on DNA-treated SWNTs is imperfect, but are drastically better than those on nonfunctionalized nanotube.
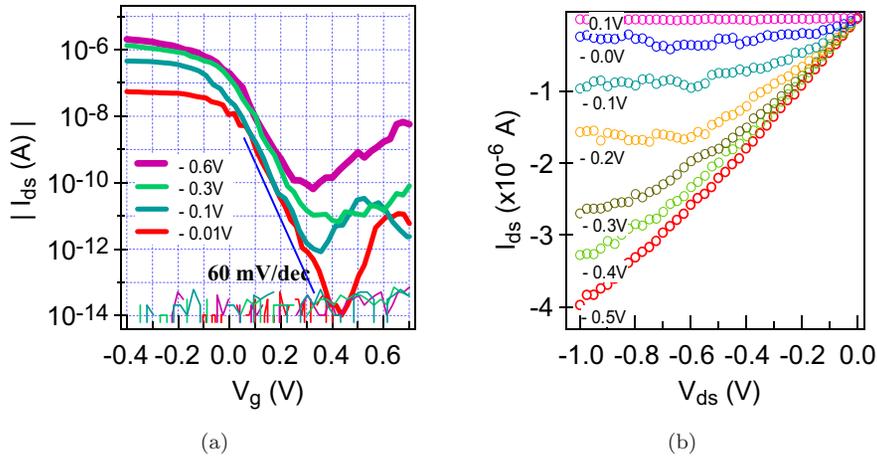

Fig. 7. A DNA-functionalized SWNT-FET ($d \sim 1.2$ nm) with $t_{ox} \sim 2$ nm high-κ gate dielectrics. (a) Current versus top-gate voltage characteristics. (b) Current versus bias-voltage characteristics under various gate voltages labeled on each curve.

with the state-of-the-art silicon technology. In order to approach the performance limit, it is desirable to integrate high-κ gate dielectrics, zero barrier contacts, ballistic nanotube channels, and self-aligned fabrication strategies for the ideal alignment of the gate with respect to the S/D. The first two criteria were discussed earlier. Ballistic transport can be observed in nanotube channels at sub-100 nm length scales as the electron scattering mean free path (mfp) with acoustic phonons $l_{ac} \sim 0.3\,\mu$m, with defects $l_{def} \sim 1\,\mu$m, and with optical phonons $l_{op} \sim 15$ nm.[29–31] Although optical phonons have a relatively short mean free path, these high energy phonon modes (~ 0.2 eV) do not play a significant
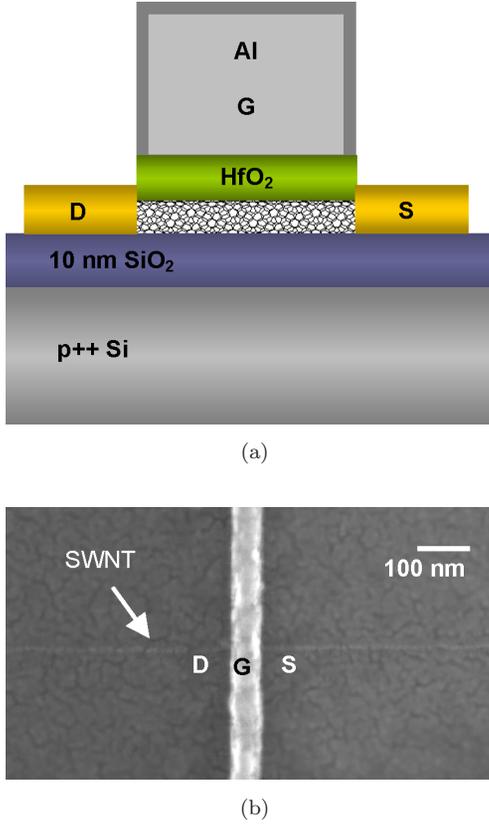
(a)

(b)

Fig. 8.   Self-aligned near-ballistic SWNT FETs. (a) Side-view schematic of a device. (b) Scanning electron microscopy (SEM) image showing the top-view of a device. The nanotube appears faint under the thin Pd electrodes.
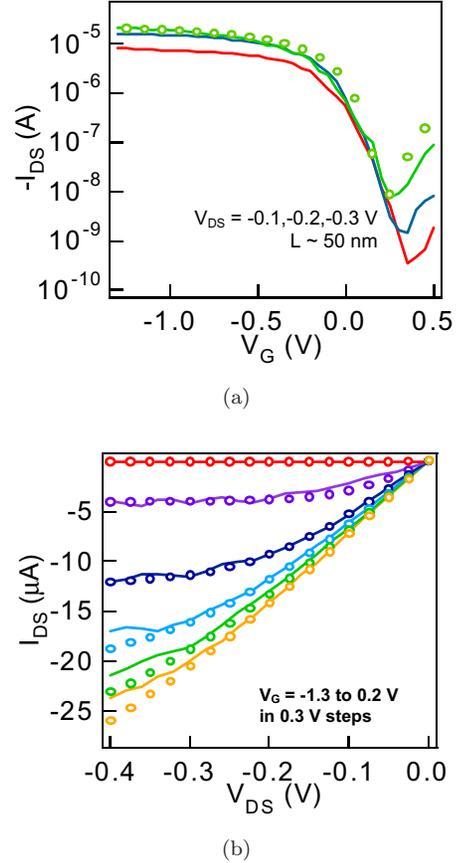

(a)

(b)

Fig. 9.   Self-aligned near-ballistic SWNT FETs. (a) Current versus top-gate voltage $(I_{DS} - V_G)$ for a device with a $L \sim 50$ nm and $d \sim 1.7$ nm SWNT. (b) $I_{DS} - V_{DS}$ characteristics of the same device. Solid lines are experimental data and symbols are ballistic quantum simulation.

scattering role at low V_{DS}.[32] As a result, quasi ballistic transport can be readily observed in nanotubes at relatively long lengths owing to the large mfp of the defects and acoustic phonons.

We have developed a novel strategy that combines all of the mentioned criteria for approaching the performance limit (Figs. 8 and 9) of nanotube FETs. The gate stack acts as a mask in forming the "self-aligned" Pd S/D electrodes as described in Ref. 6. This approach allows the fabrication of nanotube FETs with no significant overlap or underlap of the gate with the S/D electrodes (Fig. 8(a)), minimizing the parasitic capacitance and resistance of the structures.

The electrical transport properties of a miniaturized self-aligned SWNT-FET with high-κ gate dielectric and $L \sim 50$ nm is shown in Fig. 9, exhibiting high peak transconductance of $\sim 30 \, \mu$S, maximum linear ON-state conductance of $\sim 0.5 \times 4e^2/h$ and saturation current up to $\sim 25 \, \mu$A for a $d \sim 1.7$ nm tube.[6] The experimental data (solid lines, Fig. 9) is consistent with the simulation

(symbols, Fig. 9) which assumes ballistic transport in the channel. This suggests that the nanotube FET with integrated high-κ gate dielectric is operating near the ballistic regime with no extra sources of resistance in the channel or at the interface. As a result, the device is capable of delivering high currents at low V_{DS}, which is significant for realizing fast and low power electronics. To compare the performance of this SWNT FET with the state-of-the-art Si MOSFETs, the current densities of the two technologies are evaluated as a function of I_{ON}/I_{OFF} in Fig. 10.[33] For all I_{ON}/I_{OFF} values, the SWNT FET outperforms the Si MOSFET at the same V_{DD}. By developing better contact technologies to smaller diameter tubes, it should be possible to achieve even higher I_{ON}/I_{OFF} while maintaining the same I_{ON}, by using larger band gap nanotubes. Novel device concepts, such as chemically doped S/D SWNT FETs[19] and band-to-band tunneling FETs.[27,34] have also
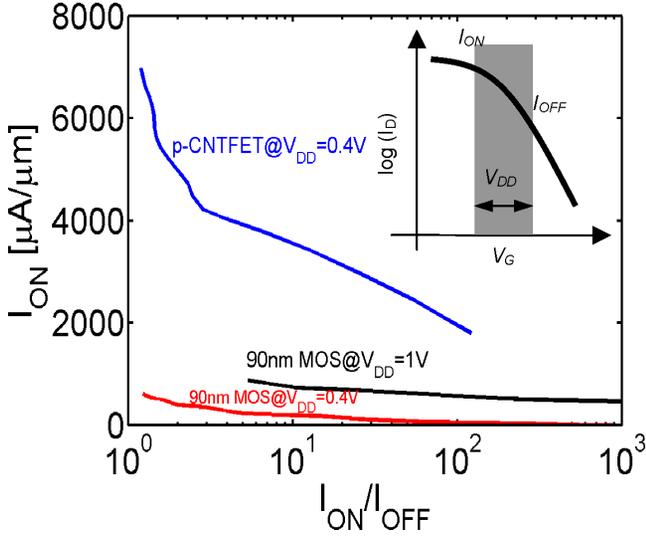
Fig. 10. ON-current drive of a SWNT FET with $L \sim 50$ nm and a 90-nm node Si MOSFET ($L \sim 50$ nm) as a function of I_{ON}/I_{OFF}. I_{ON} is an important figure of merit in performance benchmarking as the switching speed is linearly proportional to it. For a given operating voltage V_{DD}, I_{ON} at each I_{ON}/I_{OFF} value is obtained by sweeping a V_{DD} regime across an I_{DS}–V_{GS} curve as shown in the inset. The edges of the V_{DD} regime define I_{ON} and I_{OFF}.[33]

been shown to be promising in further improving the I_{ON}/I_{OFF} by reducing the OFF-state leakage currents.

6. High Field Transport Properties: Nanotubes on Substrates

High field transport properties of SWNTs are important to high power operations of nanotube electronics. Despite the ballistic nature of transport in SWNTs at low bias (where the intrinsic resistance is close to $h/4e^2 \approx 6.5$ kΩ), strong electron-optical phonon (OP) scattering dominates high field transport, when electrons can gain energies more than 0.16 eV, the zone-boundary OP energy.[29] In general, the electron-acoustic phonon (AP) interaction in SWNTs is assumed to be nearly elastic (electrons are simply backscattered, but their energy is not changed) while the OP interaction is strongly inelastic, such that electrons lose (gain) $h\omega_{OP} \approx 0.16-0.20$ eV energy when emitting (absorbing) OP phonons.[29] These effects are gleaned from transport data of Ohmically contacted metallic SWNTs in the low and high bias regimes as a function of tube lengths (Fig. 11(a)). At high biases, currents saturate at the ~ 20 μA level for long tubes due to the optical or zone-boundary phonon scattering, but
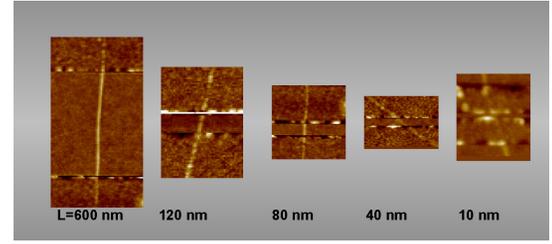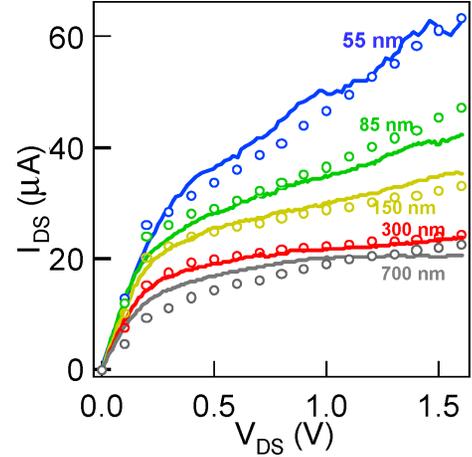
Fig. 11. Length-dependent electrical transport properties of SWNTs. (a) Atomic force microscopy (AFM) images of five devices consisting of individual SWNTs with lengths in the range of $L = 600$ to 10 nm between the edges of Pd contact electrodes. (b) Electrical properties of Ohmically contacted metallic SWNTs of various lengths. Solid lines are experimental current versus bias curves and the symbols are Monte Carlo calculation and fitting results.

the currents increase for shorter tubes (Fig. 11(b)). Monte Carlo simulations of the electrical characteristics are carried out to solve the Boltzmann transport equation. Fitting the calculated current versus bias voltage curves (Fig. 11(b) symbols) to the experimental results (Fig. 11(b) lines) reveals a mean free path (mfp) of $l_{ap} \sim 300$ nm for acoustic phonon backscattering and a mfp of $l_{op} \sim 15$ nm for optical phonon backscattering. By reducing the nanotube length to ~ 10–15 nm, up to 110 μA of current can be delivered through an ultra-short SWNT,[35] corresponding to $\sim 4 \times 10^9$ A/cm^2 current density (or 55 000 A/m, normalized by nanotube diameter). This current density is three orders of magnitude higher than that tolerable by a typical metal (e.g., Cu or Al) before breakdown via electromigration. Carbon nanotubes can sustain such high currents due to the strong chemical bonding in the covalent sp^2 carbon network.

Recent work has shown that metallic SWNTs on insulating substrates (e.g., SiO_2, Si_3N_4) heat up significantly at very high biases, suggesting that the experimentally observed current saturation (around $20\,\mu$A for tubes longer than $1\,\mu$m) may be limited by Joule self-heating.[36,37] Researchers have been able to reproduce on-substrate current–voltage (I–V) characteristics by including a simple Joule heating model, without the assumption of phonon nonequilibrium,[36,37] although some arguments to the contrary also exist.[38] The presence of nonequilibrium hot phonons in tubes on solid substrates is less certain than for suspended SWNTs (see section below), since hot OP phonons may couple with and decay into the substrate modes. Figure 12 shows the electrical characteristics of a 3-μm long metallic SWNT on a SiO_2 substrate, up to breakdown in air near 15 V. Since breakdown in inert (e.g., Ar) gas ambients occurs at much higher voltages, the breakdown in air is attributed to burning by oxidation, which occurs when the peak temperature of the tube reaches about $600°$C $= 873$ K.[39] The inset of Fig. 12 shows the experimental[40] trend (squares) of breakdown voltages for metallic SWNTs, which scales approximately as 5 V/μm with the nanotube length for tubes longer than $1\,\mu$m. This implies a breakdown voltage around 15 V for a 3-μm long metallic SWNT, as seen in the experimental

I–V curve. The scaling of breakdown voltage with length can be used to assess the SWNT-to-substrate thermal conductance, which is approximately $0.17\,$WK^{-1}m^{-1} per nanotube length. This value is up to an order of magnitude lower than the thermal conductance due to the substrate itself, suggesting that heat loss from the metallic SWNT is limited by the nanotube–substrate interface rather than the thermal properties of the substrate.

In metallic SWNTs shorter than about $1\,\mu$m, the high bias current has been experimentally observed to be notably higher than $20\,\mu$A (Fig. 11(b)). Recent analysis suggests this current enhancement is aided by increased heat dissipation and sinking at the contacts,[36,37] rather than along the length of the tube itself. The nature of the contacts and of the contact resistance (both electrical and thermal) play more significant role for such short tubes, in the length range comparable to or shorter than both the electron and the phonon mean free paths. Undoubtedly, more research needs to be done to understand the nature of the high field transport and power dissipation in very short SWNTs. However, with advances in understanding both electrical *and* thermal transport in SWNTs, engineering solutions may eventually be found to optimize both types of transport, and consequently yield more reliable and efficient carbon nanotubes for device and interconnect applications.
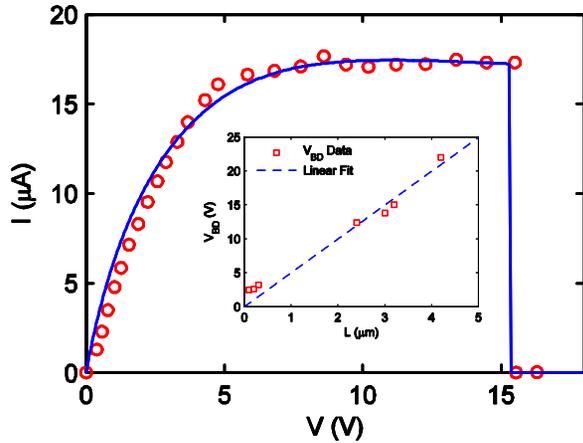

Fig. 12.   Length-dependent electrical breakdown of SWNTs on substrate. The measured electrical I–V up to breakdown in air for a 3-μm long metallic SWNT (symbols, from Ref. 30 and simulation using the model of Ref. 36 (solid line)). The simulation is interrupted when the peak temperature of the tube (in its middle) reaches $T_{BD} = 873$ K. The inset shows the linear scaling of breakdown voltage with metallic SWNT length, at approximately 5 V/μm.

7. High Field Transport Properties: Suspended Nanotubes

Despite their very high thermal conductivity, the thermal *conductance* of SWNTs is relatively low, owing to their small diameter.[41] The consequences of this low conductance are most evident in the electrical characteristics at high bias in freely *suspended* SWNTs, as shown in Fig. 13. While even long SWNTs on insulating substrates exhibit very high ($\sim 20\,\mu$A) currents at high bias, recent work has shown that suspended nanotubes carry high bias currents almost an order of magnitude lower (Fig. 13), due to significant self-heating and electron scattering with hot nonequilibrium phonons.[42] This observation is consistent with other recent studies indicating much longer phonon lifetimes in suspended SWNTs.[43] The lack of an intimate coupling with a solid substrate has a two-fold effect on the high bias electrical characteristics of a suspended
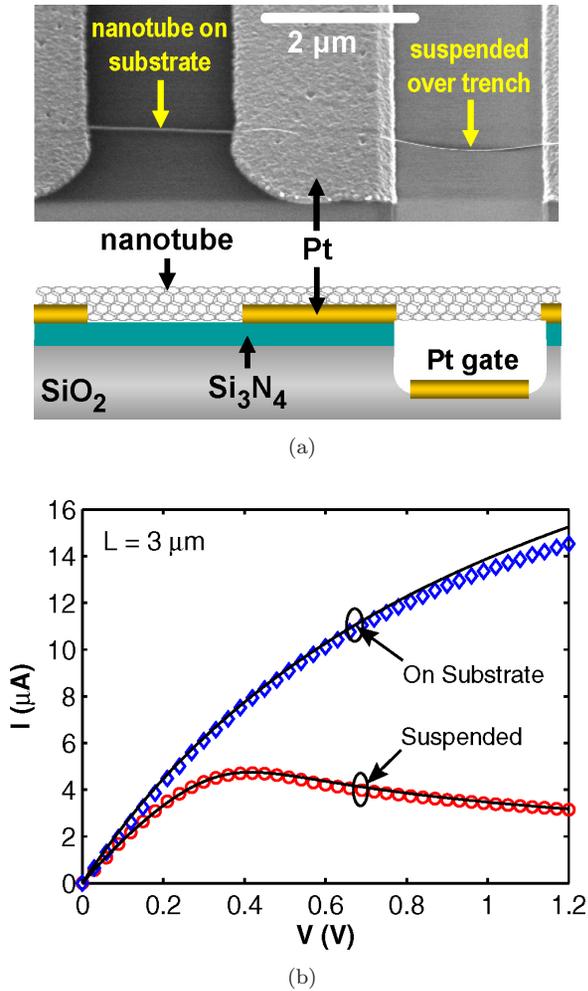
(a)

(b)

Fig. 13. Self-heating and negative differential conductance of suspended SWNTs. (a) SEM (top) and diagram (bottom) of a metallic SWNT with one portion grown across a substrate, the other suspended across a trench. (b) The measured (symbols) and calculated (lines) I–V characteristics of the two nanotube segments in vacuum are plotted for a similar device with length $3\,\mu$m and diameter 2.4 nm.

nanotube: (1) It restricts the dissipation of Joule heat along the SWNT, facing a much higher thermal resistance (due to the small diameter) and leading to significant temperature rise, and (2) it removes direct phonon relaxation channels into the substrate, preventing the immediate decay of the generated SWNT OPs and significantly raising their population (beyond the thermal average). Mann *et al.* have shown that even gaseous "substrates" in contact with suspended SWNTs can reduce hot OP lifetimes, by introducing additional phonon decay channels.[44] The suspended SWNTs in gas ambients deliver high bias currents larger than those in vacuum, but lower than for similar SWNTs on solid substrates.[44]

As a consequence, freely suspended, unperturbed SWNTs in vacuum seem to represent the extreme case of a thermally isolated and long phonon lifetime scenario for nanotubes. All such suspended SWNTs exhibit negative differential conductance (NDC) (Fig. 13(b)), but the longer ones ($10\,\mu$m) show it at much lower electric fields (~ 200 V/cm) than predicted by theoretical models that assume isothermal conditions (~ 5 kV/cm).[45] This also indicates that the observed NDC is a thermal and not electrical (e.g., contact or field-related) effect. A simple two-temperature (corresponding to acoustic and optical phonons) model[42] can be used to calculate the theoretical I–V characteristics (solid lines in Fig. 13(b)). The optical phonons are assumed to be stationary with small group velocity, and the acoustic phonons are solely responsible for heat dissipation. The approach self-consistently computes the nanotube resistance, Joule heating and temperature along its length. A key feature is the temperature-dependence of the SWNT thermal conductivity, which is found to be essential for reproducing the high bias behavior of the electrical characteristics. The approximately $1/V$ shape of the suspended SWNT I–V characteristics at high bias was found to be a consequence of the $1/T$ dependence of the thermal conductivity at high temperature from Umklapp-limited phonon scattering.[42] This provides an indirect way to measure the thermal conductivity of individual suspended SWNTs in the high temperature regime,[41] indicating it to be approximately described by $3600(300/T)$ Wm^{-1}K^{-1} from $400 < T < 700$ K. A more detailed study of the thermal conductance of individual SWNTs is described in Ref. 41.

The above results have implications to the application of nanotubes as interconnects and FETs, both of which will involve high current operation. It is interesting to note that self-heating effects in SWNT electronics including FETs (and optoelectronic devices) have been completely neglected thus far, partly owing to the quasi-ballistic transport in length scaled nanotube devices. Nevertheless, even for the shortest nanotube FETs (tens of nanometers) thus far, transport at high fields is still only *quasi*-ballistic with appreciable OP emission. Devising strategies to maximize OP decay in SWNT FETs could lead to further device performance and increase ON currents. Interface design for thermal management of SWNT electronics could therefore be an interesting direction for future research.

8. Conclusions and Future Challenges

In conclusion, SWNTs are proven to be promising building blocks for future electronics. Due to their unique crystalline 1D structure, they are capable of delivering near-ballistic currents at relatively long channel lengths and are compatible with high-κ gate dielectrics. Much progress has been achieved in enabling Ohmic contacts with zero Schottky barriers to SWNTs with diameters ≥ 1.5 nm. However, transparent contacts to both metallic and semiconducting SWNTs with diameters on the order of 1 nm have not been achieved thus far. The 1–1.3 nm diameter range is important since SWNTs synthesized by many growth techniques fall into this range. The lack of Ohmic contacts to SWNTs in this range may limit the applications of these materials for high performance electronics. Dielectric integration into carbon nanotube FETs has enabled vertical scaling to the 2 nm regime as facilitated by noncovalent chemical functionalization. High quality gate stacks for SWNT FETs can be easily obtained owing to advances in high-κ integration and the lack of dangling bonds and interface states on nanotube surfaces. In order to obtain high current nanotube FETs to compete with planar silicon transistors, one must pack SWNTs at a pitch of about twice the diameter of nanotubes, wire up these nanotubes in parallel and use them as transistor channels collectively. Importantly, only semiconducting nanotubes should be included in such FET devices to avoid electrical shorts. These are currently the most formidable challenges to the carbon nanotube electronics area. Much work is required in order to pack and assemble nanotubes together in controlled fashions, and importantly, be able to do so with only semiconducting nanotubes (or metallic tubes for other applications).

Acknowledgments

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