BY ROBERT COLWELL

TIMING DIAGRAMS: HOW TO READ AND USE THEM

Ability to interpret timing diagrams from device manufacturers is essential in designing and troubleshooting digital circuits

IN A digital system, whether it is a simple countdown circuit or a complex computer, timing is everything. Except for the simple inverter (one input, one output), logic elements such as gates, flip-flops, and counters require that two or more signals be applied to their respective inputs at the right time in order to produce the desired output. If there is a timing error and one signal is delayed for some reason, the logic element will not function properly—if at all. Thus, timing diagrams are important tools in the work of digital circuit designers.

The waveforms of digital signals are invariably shown in ideal shapes such as that in Fig. 1A. Note the infinitely fast rising and falling edges of the ideal pulse. However, we live in a world where capacitance, inductance, and time are realities,

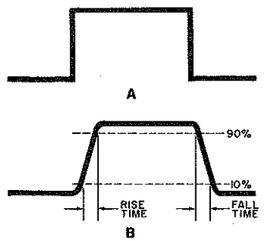


Fig. 1. An ideal digital signal (A) and a more realistic waveshape (B).

Fig. 2. Input and output waveforms for an inverter. Propagation delay shown at (C).

so it takes a finite amount of time (usually measured in nanoseconds) for a digital signal to change states. This is shown in Fig. 1B, where rise and fall times are measured between the 10% and 90% points of the waveform.

In the waveforms shown in this article, idealized shapes are used to simplify the drawings. In reality, they would look more like the waveshape in Fig. 1B.

The Timing Diagram. A timing diagram illustrates how logic signals change with time in relation to other signals. The format is: logic level (or voltage) on the vertical axis, and time on the horizontal axis. The diagram is "read" from left to right.

Consider the inverter shown in Fig. 2A. (The small circle at the output indicates signal inversion.) The timing diagram for this device (Fig. 2B) shows how the output is the inverse of the input signal. However, in the real world, it takes time for the semiconductor elements within the device to respond to the input signal. This is known as the "propagation delay" between the two signals (Fig. 2C). This delay is present in all logic elements

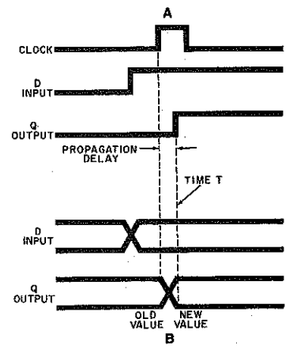


Fig. 3. Timing diagram for a D flip-flop (A); modified at (B) to show delay.

and has to be accounted for in timing diagrams.

The timing diagram for a D flip-flop is shown in Fig. 3A. Operation of this device is such that, when the clock input is a signal with a rising edge, the data (logic 0 or logic 1) at the D input is transferred to the Q output and held there until the next clock pulse. The diagram in Fig. 3A is for the case where the D input was at logic 1 when the clock pulse appeared. The Q output shows the D-input transfer along with the propagation delay. If the D input were at logic 0 when the clock pulse was received, the Q output would not have changed. There would still be a propagation delay but it would not show on the timing diagram because both sides would be at logic 0. In either case, the Q output would be valid at time T.

In the modified partial timing diagram shown in Fig. 3B, the D input and the Q output are shown at logic 0 and logic 1 at the same time—clearly an impossible situation. This technique is used to illustrate both logic conditions (old value and new value) that can exist before the clock pulse and after the clock pulse propagation delay time. After time T, the signals assume their proper states.

In computer circuits, there are sets of signals called "busses." In an 8-bit processor, there will be eight signals in the data bus, 16 in the address bus, and some undetermined number in the control bus. As shown in Fig. 4A, instead of drawing all eight input and output signals separately, we show them as a group. Here the inputs settle in before the arrival of the clock pulse, and the outputs assume the required state after the propagation delay of the data pulse. In the logic diagram of Fig. 4B, the large arrows with the numbers inside them are used to indicate the eight inputs and outputs.

Another symbol that is often used is shown in Fig. 5. In this case, the falling edge of signal 1 causes the falling edge of signal 2 or the rising or falling edges of whatever other signals are being triggered.

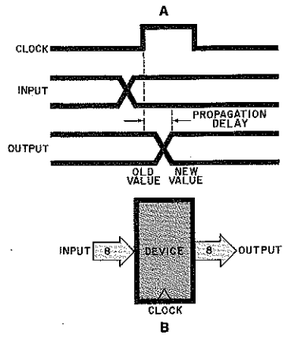


Fig. 4. How sets of signals are indicated as busses in an 8-bit processor.

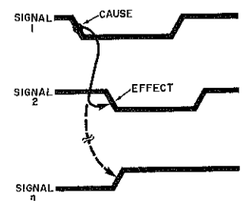


Fig. 5. Arrows are used to indicate cause and resultant effects.

A Real Chip. Let us examine the specifications for a real TTL device—in this case a 74LS163 4-bit counter. As indicated by the letters "LS" in the number, this is a low-power Schottky device.

Other than gates, most digital logic (regardless of family) is timed from a system "clock"—a pulse train with steep rising and falling edges. Since the 74LS163 is a TTL device, the clock must be "TTL compatible." This means that a clock level less than 0.8 volt is considered a logic 0 and a level greater than 2 volts is considered a logic 1. Input voltages between these two levels are disallowed.

To determine the maximum clock frequency that can be used, one must examine the specification sheet for the 74LS163. When the chip is operated at 5 V at 25°C, the specs say the maximum clock frequency (f_{clock}) is 25 MHz. Some individual chips may operate above this frequency, but there is no guarantee.

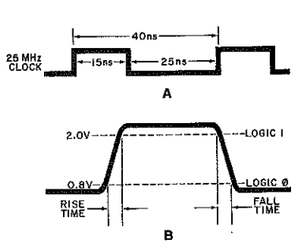


Fig. 6. The clock period has a lowtime and a hightime.

At 25 MHz, a single clock period is 40 ns and 25 million of these occur in every second. On the spec sheet it also states that the minimum period allowed (clock hightime plus clock lowtime) is 40 ns and that the width of the clock pulse (T_{wclock}) is 25 ns min. The manufacturer defines T_{wclock} as the low interval, leaving 15 ns for the high interval. This is shown in Fig. 6A. Note that ideal waveforms are used in this illustration. The more realistic waveforms are shown in Fig. 6B. Here, the rise time is the length of time the clock voltage spends in the region between a valid logic 0 and a logic 1.

The fall time is the analogous length of time when the clock voltage is falling from a logic 1 to logic 0. The rise and fall periods are known as the clock's "edges." Maximum rise and fall times are usually not specified, but they should be kept as fast as possible in a clock circuit.

In Fig. 7A, the 74LS163 is counting the clock pulses to produce an output sequence of 0000, 0001, 0010 0011, etc., which converts to 0, 1, 2, 3, etc., in decimal. This is clearly shown in the timing diagram of Fig. 7B, where the outputs for each clock pulse are shown. In a diagram like this, it is customary to put the input (cause) on the top and the outputs (effects) below.

If clocking of the circuit in Fig. 7A continues, it will eventually arrive at its maximum count of 1111 (decimal 15), with the next clock pulse producing an 0000 output. The cycling between decimal 0 and decimal 15 continues as long as clock pulses are provided.

To make this circuit count to some number less than decimal 15, say 12, some means of detecting the occurrence of decimal 12 (1100 binary) must be used. This is shown in Fig. 8A, where a two-input NAND gate has been added. The binary sequence from 0000 to 1111 for the output terminals of the 74LS163 is as follows:

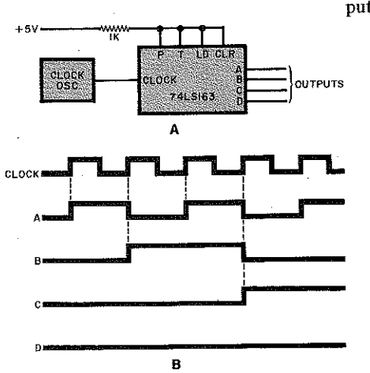


Fig. 7. The circuit at (A) is counting the clock pulses to produce the proper output sequence as illustrated by the waveforms in (B).

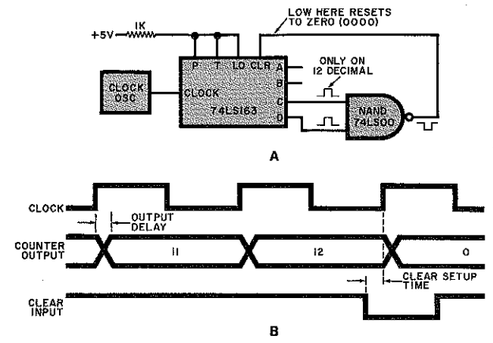


Fig. 8. The circuit of Fig. 7 modified to detect the occurrence of decimal 12.

Binary				Decimal
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

There are two important facts about this circuit: (1) when both inputs of a NAND gate are high, the output is low—otherwise it is high; (2) when the CLR (clear) input of the 74LS163 is low, the counter resets to 0000 and when the CLR is high, the device counts.

In this example, the two NAND gate inputs are connected to outputs C and D, with the normally high output connected to the clear input of the counter. It counts normally from 0000 until it reaches 1100. Then the output of the NAND gate goes low, resetting the counter to 0000. Thus, the counter/gate arrangement can be forced to count up from 0000 to 1100 in cyclic fashion. The timing diagram for this is shown in Fig. 8B. The circuit and the timing diagram appear to be satisfactory, but it is important to determine whether the 74LS163 will produce the new output and whether the NAND gate will produce an output in time to provide the clear signal before the next clock pulse.

The time period labelled "output delay" is a measure of how fast the counter changes states with the clock pulse. If we refer to the specification sheet for the 74LS163, we find that two different switching parameters are listed: one when switching from a 0 to 1 and another for the 1-to-0 transition. Since the major concern is to produce a 1100 signal for the NAND gate, the maximum specification of 24 ns will be used. Thus, at most, 24 ns after the twelfth clock pulse's rising edge, both of the inputs to the NAND gate will be at logic 1. According to the specification sheet for the 74LS00, the output goes to logic 0 within 15 ns max. This becomes the clear signal for the 74LS163 and will get clocked into the counter at the next clock edge.

The timing diagram is now as shown in Fig. 9. When the time delays through the counter and NAND gate are added, the result is 39 ns—just barely in time for the next clock edge. Will this work? Although it looks as if it would, one more specification has to be accounted for.

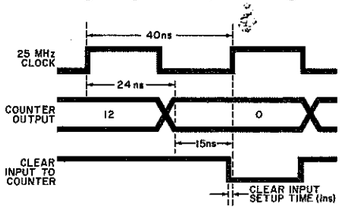


Fig. 9. Timing diagram for the circuit in Fig. 8 using parts specified.

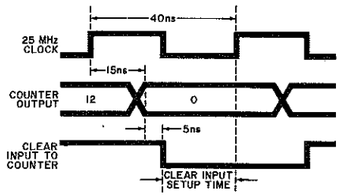
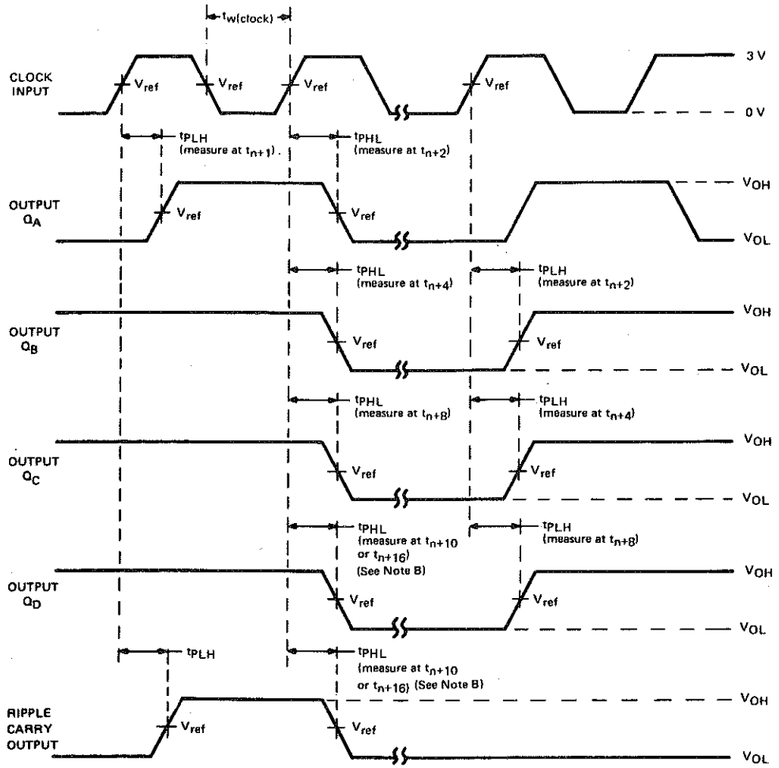


Fig. 10. Timing diagram for the clock circuit using a faster counter unit.

TYPES SN54160 THRU SN54163, SN54LS160A,THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for 'LS160A thru 'LS163A $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S162, 'S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max}.
B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.
C. For '160 thru '163, 'S162, and 'S163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 1–SWITCHING TIMES

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Timing diagrams for the 74LS163 from "The TTL Data Book."

This is setup time, the minimum amount of time the IC requires a signal to be valid before the next clock edge appears.

The 74LS163 specifies a "Clear Input Setup Time" of at least 25 ns. Unfortunately, according to the timing diagram, our circuit provides only 1 ns. If we used a faster Schottky NAND gate instead of low-power Schottky, the gate delay would be 5 ns instead of 15 ns. Since we are off by 24 ns, substituting a faster Schottky makes the circuit off by 14 ns. So it still will not work properly.

Now if the counter were a faster Schottky, the "Clock to Output Valid" time is reduced to 15 ns (instead of the 24 ns for the low-power Schottky). The setup time on the clear input is reduced to 14 ns. This is shown in Fig. 10. Thus the new Schottky version will indeed work.

There is one circuit "trick" that can be used with the low-power Schottky devices. That is to detect the decimal-11 state as shown in Fig. 11. The circuit uses a three-input NAND gate and a flip-flop to detect the decimal-11 state and delay the result by one clock pulse so that clock-pulse 12 catches up before clearing the counter. The gate has a 7-ns propagation delay and the flip-flop requires 5 ns to setup. The flip-flop propagates the D input to the Q output in 9 ns max. Thus the 25-ns setup required is met. Note that the counter has 31 ns to setup on the clear input.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
	Enable P or T	20			20			
	Load	20			20			
	Clear◊	20			20			
Hold time at any input, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

◊ This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			$C_L = 15$ pF, $R_L = 2$ kΩ, See Figures 1 and 2 and Notes 8 and 9	25	32		MHz
t_{PLH}	Clock	Ripple carry			20	35	ns
t_{PHL}					18	35	
t_{PLH}	Clock (load input high)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Clock (load input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Enable T	Ripple carry			9	14	ns
t_{PHL}					9	14	
t_{PHL}	Clear	Any Q			20	28	ns

¶ f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

NOTES: 8. Load circuit is shown on page 3-11.
9. Propagation delay for clearing is measured from the clear input for the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.

Characteristics for the 74LS163 from the "The TTL Data Book."

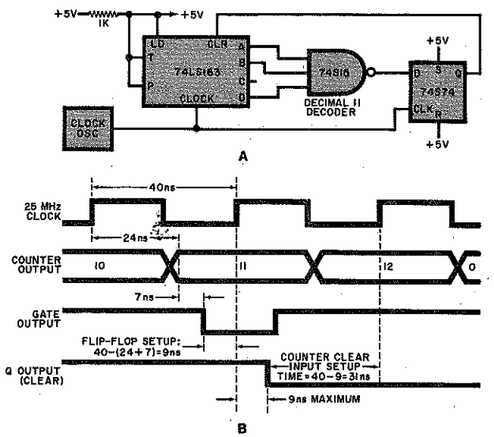

Fig. 11. Circuit and timing diagrams to detect the decimal-11 state.

Conclusion. There are two areas to watch. Timing specifications are usually given for devices operating at 5 V and 25°C. Since chips tend to get warm when operating, their timing specifications degrade at higher temperatures. This is why cooling fans are used in most equipment. Since winter temperatures may go below specifications, low-temperature specifications must also be considered when selecting chips for outdoor or automotive use.

The second problem may arise because specifications are published only for dc loads. If the dc load (fanout) of the circuit exceeds that of the specifications, other values will be downgraded. Increasing the surface area of a printed circuit trace or attempting to drive a length of cable could cause the IC to "see" a higher capacitance than specified. In each of these cases, the chip will exhibit slightly degraded performance. Most manufacturers provide a "derating" graph to take care of such contingencies.

Now you can see how even a circuit as simple as a counter can be assembled in correct logical order yet not work properly. What is important is that the timing diagram of the circuit is a valuable design tool which can save a lot of time later. ◇