IPnexus®

CPC5505

2.16-Compliant, High-Performance,
Low-Power, Single Board Computer

User's and System Integrator's Guide

PERFORMANCE TECHNOLOGIES

Revision History

Revision Date	Revision History
06/18/04	Initial Production Release
10/14/04	Corrected board height
04/06/05	Clarified Ethernet topic. Added serial port default baud rate. Corrected “J21-J24 PTMC Interface Pinout” table.
05/26/05	Added PTMC Installation topic. Updated graphics.
08/02/05	Added Sensors topic. Added BIOS POST error codes. Updated for 1.8GHz processor.
10/14/05	Added BMC Command Line Interface topic.
12/22/05	Detailed which PCBs require Kapton washers between a PTMC card and the PCB.

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Errors and Omissions

Although diligent efforts are made to supply accurate technical information to the user, occasionally errors and omissions occur in manuals of this type. Refer to the Performance Technologies, Inc. Web site to obtain manual revisions or current customer information: http://www.pt.com.
Performance Technologies, Inc., reserves its right to change product specifications without notice.

Symbols and Conventions in this Manual

The following symbols appear in this document:

Caution: There is risk of equipment damage. Follow the instructions.

Warning: Hazardous voltages are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

Electrostatic Discharge

Caution: Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is recommended that anti-static ground straps and anti-static mats are used when installing the board in a system to help prevent damage due to electrostatic discharge.

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Section

1 Introduction

This section provides a brief introduction to the IPnexus® CPC5505 System Master Processor Board. It includes a product definition, a list of product features, a "CPC5505 Faceplate" figure, a functional block diagram, and a description of each block. Unpacking, initial board configuration, and other setup information are provided in Section 2, "Getting Started."

1.1 Product Definition

The CPC5505 is an Intel® Pentium® M-based single board computer designed for carrier-grade telecom and Internet applications. The board incorporates the Intel 855GME chipset supporting a 400MHz processor bus and 2GB single channel 333MHz DDR SDRAM with ECC. The CPC5505 is fully compliant with PICMG 2.16 (Packet Switching Backplane) and also provides a 32-bit/33MHz Compact PCI bus.

The CPC5505's Pentium M Processor provides optimum performance in uniprocessing or multiprocessing systems. The board occupies one CompactPCI slot (4HP) and comes with a Pentium M Processor installed. Additionally, the CPC5505 supports hosting hot swap peripherals in a powered system.

The on-board Intelligent Platform Management Controller (IPMC or BMC) monitors, controls, and performs remote diagnostics for many on- and off-board functions through five IPMI (Intelligent Platform Management Interface) compliant system management bus interfaces.

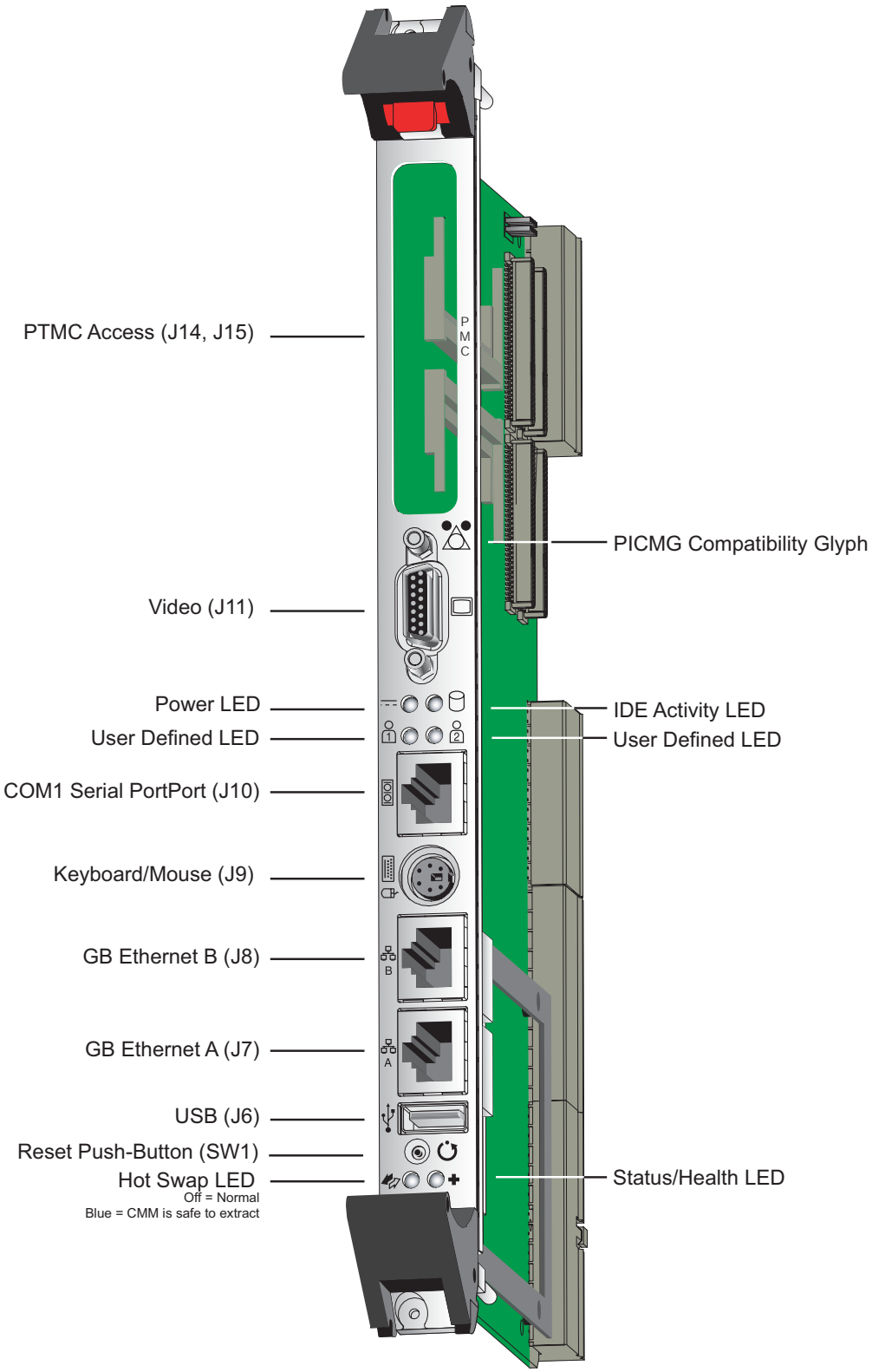
Support for an optional PTMC card is provided on the faceplate to add base board functionality such as IPSec accelerators, network processors, and additional Ethernet connectivity.

1.2 CPC5505 Features

- Single Slot 6U CompactPCI System Master Single Board computer
- CompactPCI Specification, PICMG 2.0, R 2.1 compliant
- CompactPCI Hot Swap Specification, PICMG 2.1, R 2.0 compliant
- CompactPCI Packet Switched Backplane Specification, PICMG 2.16, R 1.0 compliant
- CompactPCI System Management Specification, PICMG 2.9, R 1.0 compliant
- IPMI v1.5 specification compliant
- Designed for NEBs level-3 and ETSI installations

- 1.8 GHz Intel Pentium M Processor (400 MHz FSB)
- Integrated 1 MB L2 cache
- 32-bit/33 MHz Compact PCI bus
- 64-bit/66 MHz PTMC interface
- SMBus
- Intel ICH and 855GME GMCH Chipset
  - Intel 855GME Graphics Memory Controller Hub (GMCH-M) North Bridge
  - Intel 6300ESB I/O Controller Hub (ICH) South Bridge
- Dual 10/100/1000 Mb/s Ethernet links through backplane J3 (PICMG 2.16), faceplate J7/J8.
- Supports up to 2 GB of DDR SDRAM with ECC at 2.7 GB/s peak bandwidth.
- Performance Technologies' Embedded BIOS (AMI core) stored in local flash memory
- VxWorks, Windows® 2000/XP and Linux Operating Systems.
- Two IPMB interfaces on backplane J1 and J2 (PICMG 2.9).
- Standard AT® peripherals include:
  - Real-time clock/CMOS RAM (146818)
  - Two IDE interfaces. On board ATA/100 hard drive. Rear Panel ATA/33 support
  - Two 16C550 RS-232 serial ports
  - Video Interface
  - Floppy disk controller
  - Speaker interface (rear panel only)
  - Three USB ports
  - PC/AT keyboard/mouse controller
- Supports 2.5" low-profile, board-mounted, EIDE hard drive
- Dual-stage watchdog timer
- Push-button Reset switch
- LEDs:
  - Status (Green/Amber)
  - Two User (Green/Amber/Off)
  - Local IDE Disk Activity (Green/Off)
  - Hot Swap (Blue/Off)
  - Power/Reset (Green/Amber/Off)
  - Ethernet A and B:
    - 10/100/1000 (Off/Green/Amber)
    - Link (Green)
    - Activity (Flashing Green)

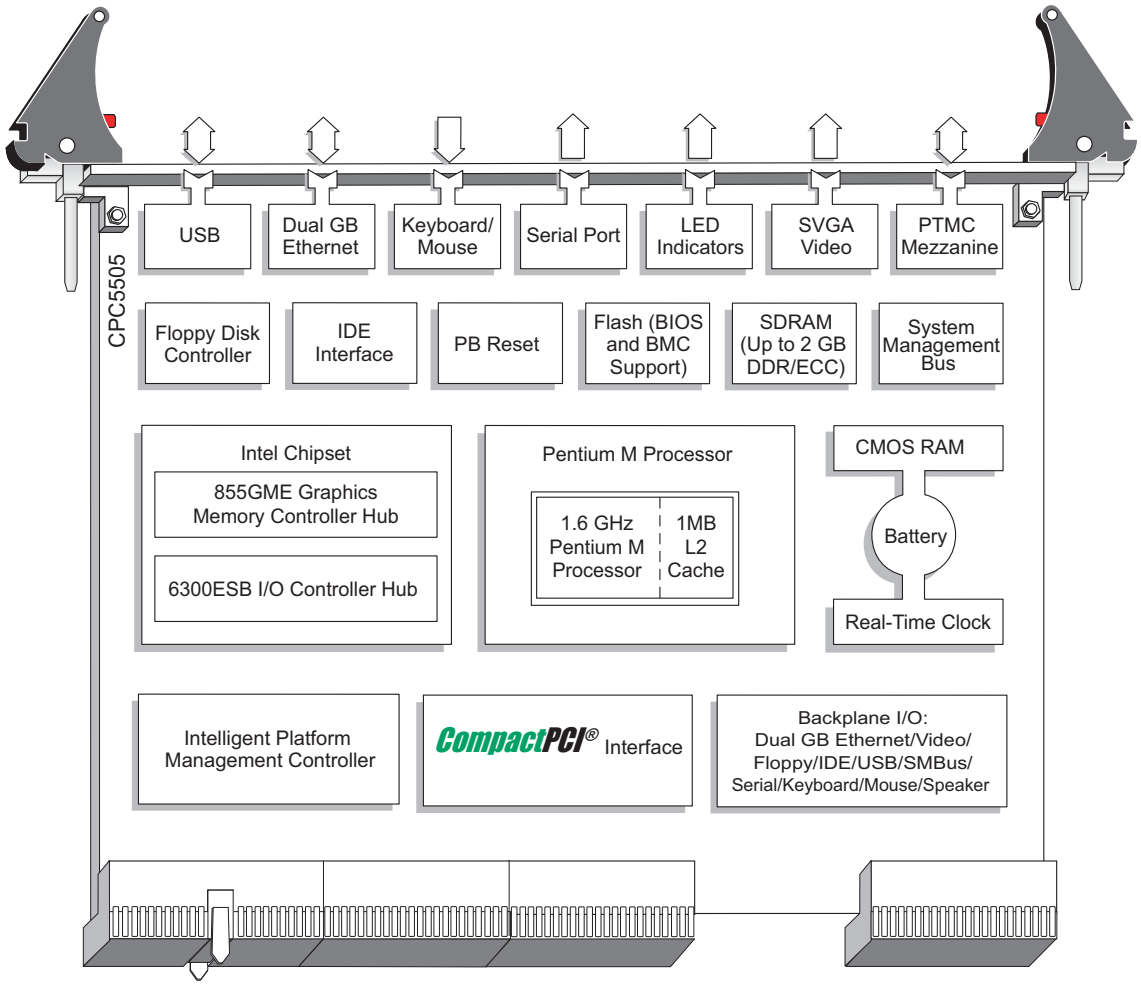
Figure 1. CPC5505 Faceplate



1.3 CPC5505 Functional Blocks

Below is a functional block diagram of the CPC5505. The following topics provide overviews of the functional blocks.

Figure 2. CPC5505 Functional Block Diagram



Intel Pentium M Processor

The CPC5702 incorporates a 1.8GHz core frequency Pentium M processor in a 479-pin FCBGA package.

The Intel Pentium M processor is a high performance, low power, 32-bit CISC processor. It is manufactured on Intel's advanced 0.13 micron process technology with copper interconnect. The processor maintains support for MMX™ technology and Internet streaming SIMD instructions. It also provides full compatibility with IA-32 software. The on-die separated 32 KB Level 1 instruction and data caches and the 1MB Level 2 cache with advanced transfer cache architecture enable significant performance improvement over other mobile processors.

The 400MHz processor system bus uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock. Along with the 4X data bus, the address bus can deliver addresses two times per bus clock. The processor features Enhanced Intel SpeedStep technology, which enables real-time dynamic switching between multiple voltage and frequency points instead of two points supported on previous versions of Intel SpeedStep technology. For the applications that require constant computing power, SpeedStep can be disabled by setting the CPU to “Maximum Performance” in the BIOS configuration.

The “Pentium M Processor” topic in Section 14 contains a link to the data sheet for this device.

Chipset

The CPC5505 incorporates the Intel 855GME Graphics Memory Controller Hub (GMCH-M) as the North Bridge and the Intel 6300ESB I/O Controller Hub as the South Bridge Chip.

Intel 855GME Graphics Memory Controller Hub (GMCH-M) North Bridge

The Intel 855GME GMCH provides bus-control signals, address paths, and data paths for transfers between the processor’s host bus, the Hub Link 1.5 bus, Video and main memory. The North Bridge features:

- Processor/Host Bus Support
- Memory System
- System Interrupts
- Video Stream Decoder
- Video Overlay
- Analog display support
- Internal Graphics Features
- Hub Interface to Intel 6300ESB I/O ControllerPower Management

The “Chipset” topic in Section 14 contains a link to more information for this device.

Intel 6300ESB I/O Controller Hub South Bridge

The Intel 6300ESB I/O Controller Hub (ICH) is a multifunctional PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub functionality, and enhanced power management. The ICH South Bridge features:

- 8-Bit Hub Interface
- PCI-X BUS I/F
- PCI BUS I/F

- Integrated IDE controller
- USB
- Power Management Logic
- External Glue Integration
- Firmware Hub(FWH) I/F supports BIOS Memory size up to 8 MB
- Enhanced DMA Controller
- Real- Time Clock
- Interrupt Controller
- Multimedia Timers based on 82C54
- Watch dog timer
- SMBus
- Integrated 16550 compatible UART
- Port 60/64 Emulation
- GPIO

The "Chipset" topic in Section 14 contains a link to more information for this device.

CompactPCI Bus Interface

The CPC5505 processor board uses the Intel 6300ESB I/O Controller Hub to support a 32-bit, 33 MHz CompactPCI interface at backplane connectors J1/J2.

Performance Technologies designed the CPC5505 to be used as a System Master or a stand-alone processor board in a CompactPCI system. The board occupies one CompactPCI slot (4HP) with Pentium M processor installed. Its CompactPCI bus design allows it to supports a maximum of seven CompactPCI peripheral cards.

The CPC5505 backplane is compliant with the CompactPCI Specification, PICMG 2.0, Version 2.1. When used in a hot swap compliant backplane and in accordance with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*, the CPC5505 supports hosting hot swap peripherals in a powered system. The CPC5505 can also function in a standard (non-hot swap) CompactPCI system. The CPC5505 is also compliant with the *CompactPCI System Management Specification, PICMG 2.9 Version 1.0, PICMG 2.15 R1.0 configuration 7 (PT7CC)*, and with the *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, Version 1.0*.

Section 14, "Data Sheet Reference," contains links to the PICMG Web site, where these CompactPCI Specifications may be obtained.

For more information on Hot Swap implementation, refer to the *Performance Technologies Hot Swap Kit Software Manual*.

Intelligent Platform Management Controller

The CPC5505 includes an Intelligent Platform Management Controller (IPMC or BMC) based on the Qlogic Zircon UL. The BMC subsystem monitors, controls, and performs remote diagnostics for many on- and off-board functions through IPMI (Intelligent Platform Management Interface) compliant system management bus interfaces.

The BMC monitors system sensors for system management events, such as overtemperature, out-of-range voltages, fan failures, etc., and logs any occurrences in its non-volatile System Event Log (SEL). The BMC also provides the interface to the sensors and SEL so system management software can poll and retrieve the present status of the system.

The CPC5505 is compliant with standard Intelligent Platform Management Interface v1.5 Specification functionality. See the Intelligent Platform Management Interface in Section14 for information about this specification.

Sensors

Several sensors on board the CPC5505 collect status data and relay the information to the Intelligent Platform Management Controller. The following table describes each onboard sensor.

Table 1. CPC5505 Sensors

Sensor Number (dec)	Sensor Name	Sensor Description
80	Temp - CPU	Processor core temperature
81	Temp - DIMM1	Board solder side temperature behind DIMM1
82	Temp - DIMM2	Board solder side temperature behind DIMM2
96	IPMB_PWR3	3.3V derived from IPMB_PWR for IPMC core
97	IPMB_PWR	5V standby IPMB (standby) power after conditioning
98	VIO	Backplane I/O voltage after power control
99	VCC2_5	2.5V regulated power for DDR memory
100	VCC1_5	1.5V regulated power for Southbridge
101	VGME_CORE	1.35V regulated power for Northbridge
102	VREF1_25	1.25V reference voltage for DDR memory
103	VTT1_25	1.25V termination voltage for DDR memory
104	VCCP	1.05V termination voltage for CPU frontside bus
105	VBAT_MON	Battery voltage
106	VCC	5V backplane voltage after power control
107	VCC3	3.3V backplane voltage after power control
108	P12V	+12V backplane voltage after power control
109	N12V	-12V backplane voltage after power control
110	VCCCORE	CPU core voltage
112	FRNT PNL EJECT	Ejector handle switch status: Open: asserted Closed: deasserted

Memory

The CPC5505 includes two 200-pin, right angle, Small Outline Dual Inline Memory Module (SODIMM) socket populated with up to 2GB DDR SDRAM with ECC at 2.7Gbyte/s peak bandwidth.

Flash/BIOS Recovery

The CPC5505 incorporates 16 MB of on-board, programmable, BIOS Flash memory. The BIOS resides in the first megabyte of flash. The FLASH.EXE utility allows you to install an operating system image or any executable image into the remaining 15MB of flash. See the *Performance Technologies Embedded BIOS Software Manual* for more information. The User Documentation topic in Section 14 provides a link to this document.

A second flash device is used as a BIOS recovery module. The CPC5505 can be configured to use either device for boot control. When booting from the BIOS recovery module, the BIOS update utility can access the onboard flash device by manipulating the system registers. The onboard flash is write protected on power up and reset. See Section 6, "BIOS Recovery," for more information.

PTMC Interface

The CPC5505 is also a PMC carrier card that supports the following specifications:

- Complies with PICMG 2.15 R1.0 configuration 7 (PT7CC).
- Dual channel Ethernet links (MDI) compatible with PICMG 2.15 ECN 2.15-1.0-001 (Ethernet MDI Links on PTMC, configurations 5 and 6).
- Complies with IEEE1386.1 PCI Mezzanine Card (PMC).
- Complies with VITA 39: PCI-X for PMC (66MHz).

The PCI Telecom Mezzanine Card (PTMC) interface is compatible with the PICMG 2.15 PT7CC specification. The PTMC provides a way to add modules such as IPSec accelerators and network processors to increase base board functionality.

The CPC5505 PTMC site provides an industry standard interface for a high performance, dual channel, gigabit Ethernet PMC mezzanine card. High performance is achieved by means of a 64-bit wide, 66MHz interface that is capable of PCI or PCI-X signaling. Dual channel Ethernet links (MDI[1]) are routed on PTMC interface connector J24 per PICMG 2.15 configurations 5 and 6. The Ethernet links can be routed to CPC5505 rear-panel gigabit Ethernet connector J3 for connection to the CompactPCI backplane per PICMG 2.16.

PCI/PCI-X signaling is supported for 3.3V VIO. Contact the factory if 5V mezzanine support is required.

The CPC5505 is backward compatible with all standard 32-bit and 64-bit PMC cards. However, these cards do not respect the PTENB# signal. We advise caution when installing a standard PMC card with P4 (rear I/O) signaling. Please check the pinout carefully.

PTMC modules interfacing to the CPC5505 must advertise their PTID (PCI Telecom Identifier) as “configuration 7” before they are enabled (PTENB# asserted). PTMC modules supporting configurations 1,2,3,4,5,6 will not have their PTMC interface enabled by PTENB#.

Please contact the factory if I^2C bus connectivity to the PTMC site is desired. It is not enabled in the default configuration.

The mezzanine interface is at J21-J24 on the CPC5505. See Section 8, “Connectors,” for more information.

Drone Mode

Typically, the CPC5505 operates as the System Master from the system slot. The CPC5505 can also operate in Drone Mode from a peripheral slot. In Drone Mode, the CPU board receives power from the system but it cannot communicate on the CompactPCI bus. Onboard logic uses SYSEN# to qualify the CPC5505's location when inserted in a peripheral slot, thereby isolating the board from the CompactPCI bus.

The CPC5505 can be hot swapped when operating in Drone Mode (in peripheral slots, the board is operating in isolation from the backplane).

Caution: The CPC5505 is not intended to be hot swapped in the system slot. Hot swapping the CPU board in the system slot may damage other boards in the system.

Power Ramp Circuitry

The CPC5505 features a hot swap controller with power ramp circuitry that enables the board’s voltages to ramp in a controlled fashion. The power ramp circuitry eliminates any large voltage or current spikes caused by removing or inserting hot swappable boards while the system is still under power. This controlled ramping is a requirement of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*.

The CPC5505’s hot swap controller unconditionally resets the board when it detects that the 3.3V, 5V, and 12V supplies are below an acceptable operating limit. These limits are defined as 4.75V (5V supply), 3.15V (3.3V supply), and 10.0V (+12V supply).

Fault current sensing is also provided. If a board fault (short circuit) or over-current condition is detected, the hot swap controller automatically removes power from the CPC5505 components.

Reset

The CPC5505 provides the following reset types:

- Push-button reset
- Backplane reset input

- Watchdog timer reset

See Section 11, “Reset,” for more information.

Two-Stage Watchdog Timer

The watchdog timer optionally monitors system operation and is programmable for one of eight different timeout periods (from 0.25s to 256s). It is a two-stage watchdog, meaning that it can be enabled to produce a Non-Maskable Interrupt (NMI) before it generates a system reset. Failure to strobe the watchdog timer within the programmed time period may result in an NMI, a system reset, or both. A register bit is set if the watchdog timer caused the reset event. This watchdog timer register is not cleared on reset. It is cleared on power-up, enabling system software to take appropriate action on reboot.

See Section 5, “Watchdog Timer,” for more information.

DMA

An enhanced, 8237-style DMA controller is provided on the CPC5505 for use by on-board peripherals. DMA channel 2 is assigned to the optional floppy drive.

The CPC5505’s DMA controllers reside in the Intel 6300ESB I/O Controller Hub. The “Chipset” topic in Section 14 provides a link to the data sheet for this device.

Interrupts

Two enhanced, 8259-style interrupt controllers implemented in the Intel 6300ESB ICH, provide the CPC5505 with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/timers
- Serial I/O
- System timer
- Floppy disk
- DMA channels
- IDE interface
- Real-time clock
- On-board PCI devices
- Keyboard/Mouse

Enhanced capabilities include the ability to configure each interrupt level for active high-going edge or active low-level inputs.

The CPC5505’s interrupt controller resides in the Intel 855GME Chipset. The “Chipset” topic in Section 14 provides a link to the data sheet for this device.

Enhanced IDE Controller

The CPC5505 features an IDE controller that supports onboard and optional external IDE drives. ATA/100 is supported on the primary IDE channel, allowing up to 100 MBps throughput. ATA/33 is supported on the secondary IDE channel, allowing up to 33 MBps throughput.

Primary channel IDE signals are available through internal connector J13. Secondary channel IDE signals are available through rear-panel I/O connector J5. See Section 4, "IDE Interface," for more about the CPC5505's IDE support.

The CPC5505's IDE controller resides in the 6300ESB ICH Chipset. The "Chipset" topic in Section 14 provides a link to the data sheet for this device. Connector locations and pinouts are documented in Section 8, "Connectors."

Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a common interface to slower-speed peripherals such as keyboard, serial ports, and mouse ports. The CPC5505 supports booting from a USB CD-ROM or floppy device.

The CPC5505 supports three USB ports. One v2.0 USB port (Port 0) is available at faceplate connector J6. Two v1.1 USB ports (Port 1 and Port 2) are directed through RPIO connector J5.

The CPC5505's USB resides in the 6300ESB ICH Chipset. The "Chipset" topic in Section 14 provides a link to the data sheet for this device. Connector locations and pinouts are documented in Section 8, "Connectors."

Counter/Timers

Three counter/timers as defined for the PC/AT® are included on the CPC5505. Operating modes supported by the counter/timers include:

- Interrupt on count
- Square wave generator
- Hardware triggered
- Frequency divider
- Software triggered
- One shot

The CPC5505's 8254-compatible counter/timer resides in the ICH Southbridge. The "Chipset" topic in Section 14 provides a link to the data sheet for this device.

Floppy Controller

The CPC5505 includes a standard floppy disk controller. The floppy disk controller supports an optional external floppy drive that is compatible with an 82077 diskette drive controller and supports PC-AT and PS/2 modes. Floppy signals are available through RPIO connector J5.

The CPC5505's floppy disk controller resides in the National Semiconductor PC87417 I/O controller. The "I/O Controller" topic in Section 14 provides a link to the data sheet for this device. Connector locations and pinouts are documented in Section 8, "Connectors."

NOTE: Floppy disks are magnetically recorded media. Avoid placing floppy disk drives near magnetic sources such as power supplies.

Real-Time Clock, CMOS RAM and Battery

The real-time clock performs timekeeping functions and includes 256 bytes of battery- backed CMOS RAM in two banks that are reserved for BIOS use. Timekeeping features include a time-of-day clock and a multi-century calendar with alarm features and century rollover. The clock is accurate to ± 13 minutes/year at 25 ºC. The time, date, and CMOS values can be specified or returned to their defaults by using the BIOS Setup program. See the "BIOS Configuration Overview" topic in Section 2 for more information.

NOTE: The recommended method of accessing the date in systems with IPnexus processor boards is indirectly from the real time clock via the BIOS. The BIOS on IPnexus processor boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the real time clock during each BIOS request (INT 1Ah) to read the date and, if less than 80 (1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

A coin-cell battery located on the CPC5505 processor board powers the real-time clock and CMOS memory. When the CPC5505 is not powered externally, the battery has an estimated life of six years. When the CPC5505 is powered up, the 3.3 V backplane current from the power supply extends the life of the battery.

The CPC5505's real-time clock resides in the National Semiconductor PC87417 I/O controller. The "I/O Controller" topic in Section 14 provides a link to more information for this device.

Speaker Interface

For external speaker interfacing, the CPC5505 supports an external AT-compatible speaker through the RPIO connector J5. Connector locations and pinouts are documented in Section 8, "Connectors."

Serial I/O

The CPC5505 provides two 16C550, PC-compatible serial ports. COM1 is available at the faceplate via 8-pin RJ-45 connector J10 and is also routed to connect to the IPMI Controller Emergency Management Serial Port (EMP). COM1 and COM2 are also available to an RTM via RPIO connector J5.

Both ports are compatible with RS-232 signaling levels and support data transfers at speeds up to 115.2 Kbits/sec with BIOS support. The baud rate defaults to 9600 and is set in the BIOS Setup utility.

The CPC5505's serial controller resides in the National Semiconductor PC87417 I/O controller. The "I/O Controller" topic in Section 14 provides a link to more information for this device. Connector locations and pinouts are documented in Section 8, "Connectors."

Keyboard/Mouse Controller

The CPC5505 includes an on-board PC/AT keyboard/mouse controller. Keyboard and mouse signals are available at the faceplate via J9. A "Y" interface cable is required to use both interfaces at once. The keyboard and mouse signals are also available through the RPIO connector J5.

The CPC5505's keyboard/mouse controller resides in the National Semiconductor PC87417 I/O controller. The "I/O Controller" topic in Section 14 provides a link to more information for this device. Connector locations and pinouts are documented in Section 8, "Connectors."

Video Interfaces

The CPC5505 provides on-board video using the 855GME Graphics Memory Controller Hub (GMCH-M). GMCH-M provides support for progressive scan analog monitor pixel resolution up to 1600x1200 at 85-Hz refresh and up to 2048x1536 at 75-Hz refresh.

VGA-compatible video signals are available at the CPC5505 faceplate via connector J11 and also at rear-panel I/O connector J5.

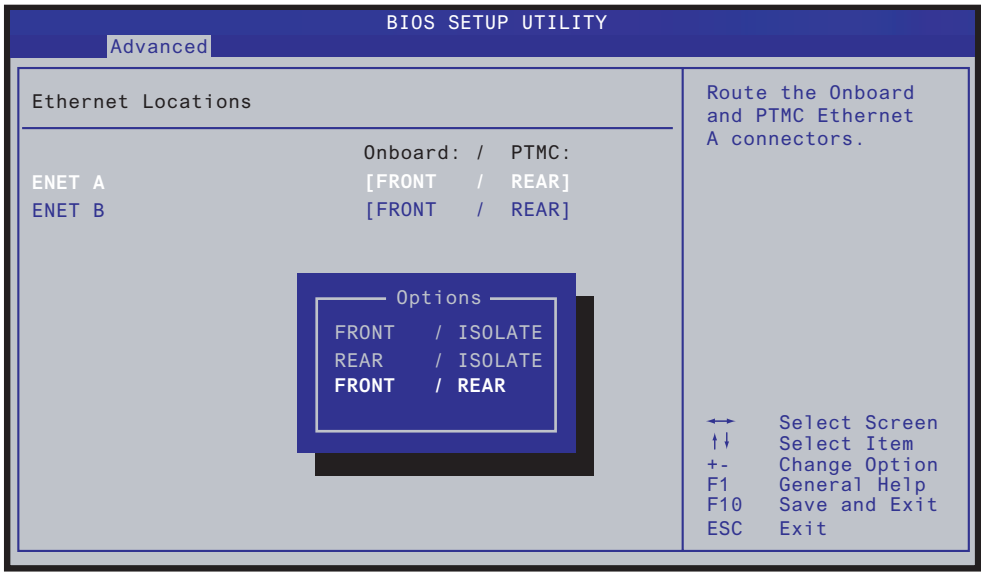
The "Chipset" topic in Section 14 contains a link to the data sheet for the GMCH-M. Connector locations and pinouts are documented in Section 8, "Connectors."

Ethernet Interfaces

The CPC5505 provides two onboard 10/100/1000Base-T Ethernet channels (ENET A and ENET B) through the Intel 82546 Gigabit Ethernet PCI Controller. Both Ethernet channels can be directed through the BIOS Setup utility to faceplate RJ-45 connectors J7 and J8, which have LEDs to indicate the status of each channel. Alternatively, both Ethernet channels can be routed to RPIO connector J3. See the "Ethernet BIOS Setup" figure below.

The CPC5505 PTMC site also provides an interface for a dual channel gigabit Ethernet PMC mezzanine card. The BIOS Setup utility allows these Ethernet signals to be either isolated or routed to CPC5505 RPIO connector J3. See the "PTMC Interface" topic for more information.

Figure 3. Ethernet BIOS Setup



The “Ethernet” topic in Section 14 contains links to the data sheets for the Intel 82546 Gigabit Ethernet device used onboard the CPC5505. Connector locations and pinouts are documented in Section 8, “Connectors.”

LED Indicators

The LEDs located on the faceplate are defined below. See the topic “Programming the LEDs” in Section 2 for software code used to program the user-defined LEDs.

Power/Reset

- Green = out of reset, power enabled
- Amber = active reset, power enabled
- Off = Power disabled

IDE disk activity (primary or secondary)

- Green = active
- Off = inactive

User-defined LEDs—one may be defined as clock throttle

- Green = user defined
- Amber = user defined
- Off = user defined

Ethernet A, Ethernet B RJ-45 LEDs, one per channel

- Flashing green = activity
- Green = Link
- Off = 10 Mbps
- Green = 100 Mbps
- Amber = 1000 Mbps

Hot Swap

- Blue = safe to extract board
- Off = not safe to extract board

Status/Health

- Green = healthy
- Amber = needs service

Rear-Panel I/O

The CPC5505 transitions the following I/O signals through CompactPCI connector J5 to an RPIO board such as the IPnexus ZT 4807e Rear-Panel Transition Board:

- Floppy
- Keyboard
- PS/2 mouse
- Video
- Two serial ports (COM1 and COM2)
- EIDE (ATA-2) secondary channel
- Ethernet LED
- Local CPU SMBus
- USB channels 1 and 2
- RPIO Eject
- Power/Ground
- Speaker
- NMI / PBRST / RPIO_PRESENT / PWRGD signals

In addition, the CPC5505 transitions Ethernet A and B through CompactPCI connector J3.

See Section 8, “Connectors,” for more information on the connectors present on the CPC5505.

1.4 Software

BIOS

The Performance Technologies Embedded BIOS (AMI core) is loaded in flash on board the CPC5505. The BIOS is user-configurable to boot an operating system from one of the following locations:

- Local flash memory
- Hard drive
- CD-ROM/DVD-ROM drive
- Floppy drive
- Network source

Operating Systems

The CPC5505 is compatible with all major PC operating systems. Performance Technologies provides additional operating system support when the CPC5505 is purchased in conjunction with an IPnexus development system. This support may include additional drivers for Performance Technologies products such as peripherals and flash drives. Software device drivers for the CPC5505 can be found on the Performance Technologies Web site.

The following operating systems are supported:

- Microsoft® Windows® 2000
- Industry standard version of Linux®
- Comprehensive board support package (BSP) for VxWorks®. The CompactPCI VxWorks-5.4 BSP streamlines the implementation of VxWorks on the CPC5505. The VxWorks development system must be purchased directly from WindRiver.

Refer to the Performance Technologies Web site for a complete list of compatible operating systems.

IPMI

For more information about how to program software to interact with the IPMI firmware, refer to the *Intelligent Platform Management Interface v1.5 Specification* and the *Intelligent Platform Management Interface Implementer's Guide*.

Hot Swap

Hot swap refers to the dynamic insertion and removal of devices in a computer system without halting the system.

When used in a hot swap compliant backplane and in accordance with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*, the CPC5505 supports hosting hot swap peripherals in a powered system. Section 14, "Data Sheet Reference," contains a link to the CompactPCI Hot Swap Specification.

The Performance Technologies Hot Swap Kit provides software that collaborates with the operating system to provide hot swap support for CompactPCI. Operating systems supported include Windows 2000, VxWorks, and Linux. For more information about the Hot Swap Kit, refer to the *Performance Technologies Hot Swap Kit Software Manual*.

Section

2 Getting Started

This section summarizes the information you need to make the CPC5505 operational. Please read it before attempting to use the board.

2.1 Unpacking

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Performance Technologies for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to Performance Technologies. Refer to Section 15 for assistance information.

Warning: Like all equipment that uses MOS devices, the CPC5505 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with your order when handling the board.

2.2 CPC5505 System Requirements

The following CPC5505 system requirements are briefly described below:

- Backplane connectivity
- Electrical and environmental requirements

Backplane Connectivity

The CPC5505 can be installed as a System Master in the System Slot or as a stand-alone computer in a peripheral slot. Refer to the "Drone Mode" topic for more information on using the CPC5505 as a stand-alone computer.

The CPC5505 is designed for use in a CompactPCI Packet Switching Backplane (compliant with the CompactPCI Specification, PICMG 2.16, Version 1.0). This requires that the backplane provide a CompactPCI bus on connectors J1 and J2 and Ethernet pins on J3. To support optional rear-panel transition (RPIO) boards, the backplane's RPIO connector (J5) must be available and have through pins to the CPC5505's J5 connector.

The CPC5505 supports universal voltage: it operates in both 3.3V V(I/O) and 5V V(I/O) slots.

See Section 8, “Connectors,” for complete connector locations, descriptions, and pinout tables.

Electrical and Environmental Requirements

The CPC5505 with a 1.8 GHz processor loaded requires a maximum of +5 VDC +5%, -3% @ 2.9 A, +3.3 VDC +5%, -3% @ 9.5 A, and +12 VDC ± 5%, -3% @ 10 mA. Electrical specifications are presented in more detail in Section 9.

The CPC5505 is supplied with a heat sink that allows the processor to operate between 0° and approximately 50°C ambient with a minimum of 250 LFM (1.27 meters per second) of external airflow. It is the user’s responsibility to ensure that the CPC5505 is installed in a chassis capable of supplying adequate airflow. The maximum power dissipation of the processor is 24W. External airflow **must** be provided at all times. See Section 9, “Specifications,” and Section 12, “Thermal Considerations,” for more details.

Warning: Operating the CPC5505 without adequate airflow will damage the processor.

The CPC5505 may contain materials that require regulation upon disposal. Please dispose of this product in accordance with local rules and regulations. For disposal or recycling information, please contact your local authorities or the Electronic Industries Alliance at http://www.eiae.org/.

2.3 Memory Configuration

The CPC5505 can *address* up to 4 GB of memory that is allocated between system memory and PCI devices. Two SO-DIMM sockets provide up to 2 GB of DDR system memory. The memory address space is divided between memory local to the board (system memory) and memory located on the two PCI buses. Any memory not reserved or occupied by a local memory device (DDR or flash) is available to the onboard PMC site or to devices on the CompactPCI bus.

The CPC5505 is optionally populated with PC2700 ECC DDR SDRAM located on two registered, 200-pin SDRAM DIMM sockets (J14, J15). The socket supports 256 MB, 512MB or 1 GB memory modules, giving a memory size range from a minimum of 256 MB to a maximum of 2 GB of 333 MHz DDR (PC2700) memory.

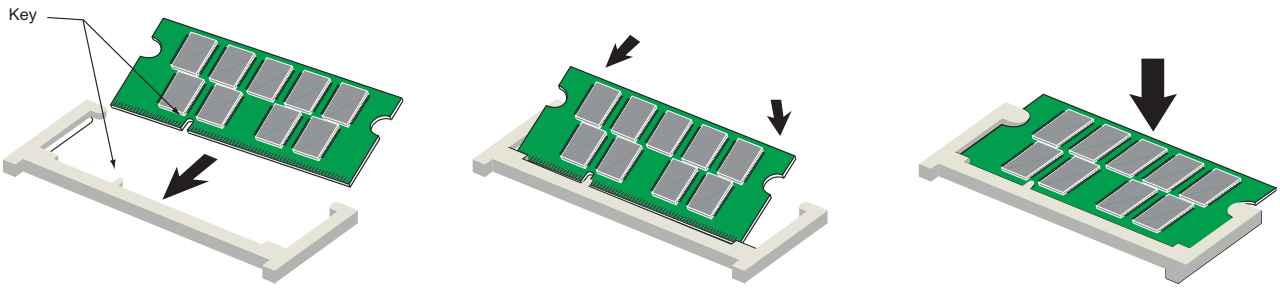
The “Memory Address Map Example” illustration shows an example of memory addressing for the CPC5505.

Installing Memory

Performance Technologies recommends installing only memory validated for the CPC5505.

1. Locate DIMM sockets J14 and 15. See the Connector Locations figure in Section 8.
2. The DIMM sockets are reversed, mirror images of each other, with their registration keys both located toward the backplane connectors. One memory module is installed reversed from the other.
3. Insert the memory module so its registration notch aligns with the key in the desired memory socket and its edge connector slides into the socket connector.
4. Press the memory module down until the latches click into place and retain the module.
5. Once installed correctly, the memory module appears as it does at the right of the "Memory Module Orientation" figure.

Figure 4. Memory Module Orientation



2.4 I/O Configuration

The CPC5505 addresses up to 64 KB of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the CompactPCI bus. Any I/O space not occupied by a local I/O device is available for the CompactPCI bus.

The CPC5505 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Map" illustration.

Figure 5. Memory Address Map Example

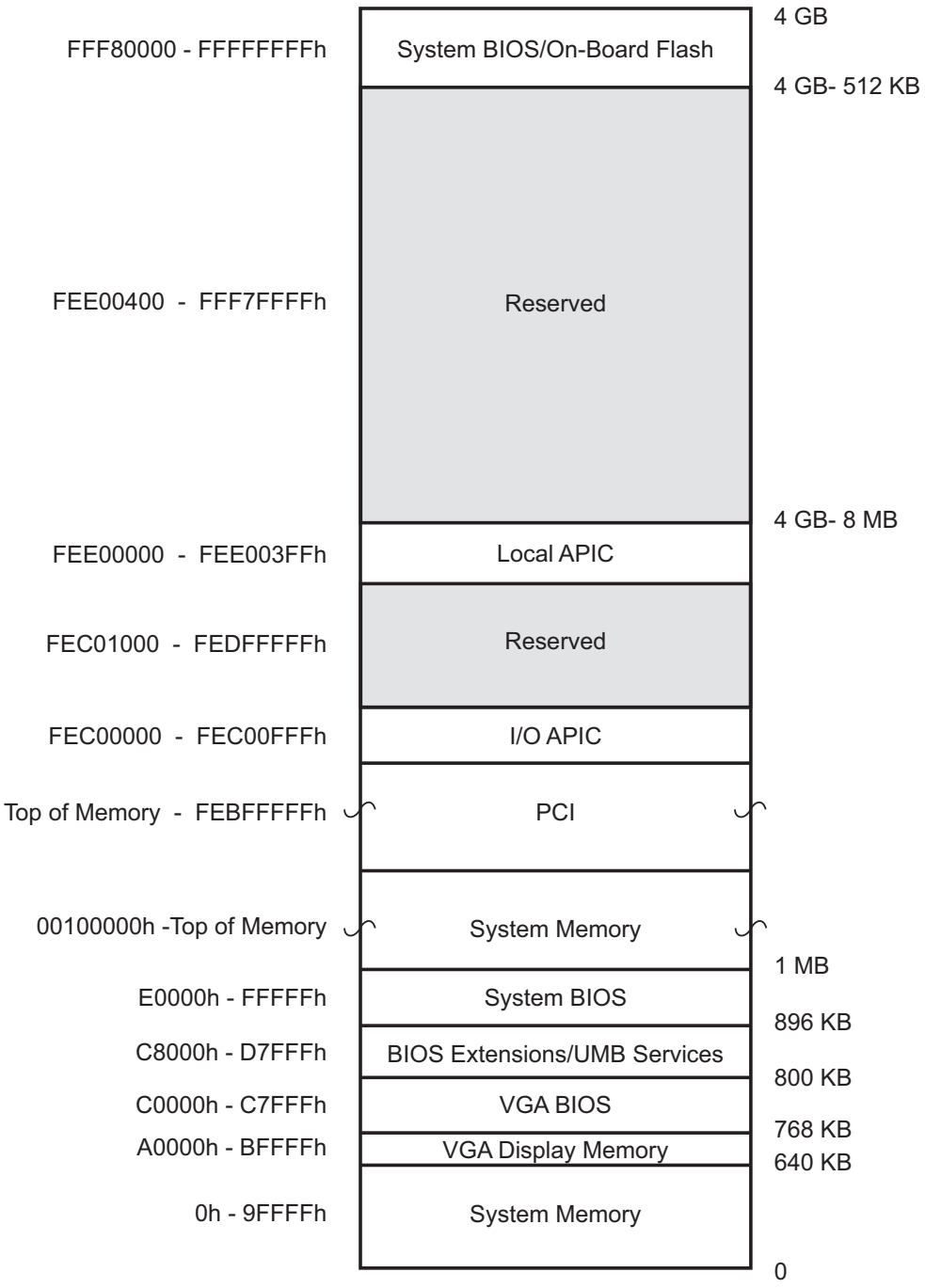


Figure 6. I/O Address Map

CF9h	Reset Generator
CA3h	IPMI Command Status
CA2h	IPMI KCS Data
800h	SB Power Management Base
5A0h	SIO GPIO Base
560h	SIO XBus Base
540h	SIO PM Base
520h	SIO SWC Base
4D0 - 4D1h	Interrupt Controller
480h	SB GPIO Base
400h	SB SMB Base
3F6h	Primary IDE Registers
388 - 38Bh	AdLib
376h	Secondary IDE Registers
208 - 20Fh	Gameport High
200 - 207h	Gameport Low
1F0 - 1F7h	Primary IDE Registers
170h - 177h	Secondary IDE Registers
F0h	Coprocessor
E9 – Efh	Reserved
E1-E8h	CPC5505 System Registers
C0 – DFh	On-board Slave DMA Controller
B4 - BDh	Interrupt Controller
B2 - B3h	Power Management
A4 - B1h	Interrupt Controller
A0 - A1h	On-board Slave Interrupt Controller
93 – 9Fh	DMA Controller
92h	Fast Gate A20/Reset Control
81 - 8Fh	On-board DMA Page Registers
78 - 80h	CPC5505 System Registers
70 - 77h	NMI Enable/RTC Controller
67h	NMI Controller
66h	Reserved
65h	NMI Controller
64h	PS/2 Keyboard/Mouse
63h	NMI Controller
62h	Reserved
61h	NMI Status Register
60h	PS/2 Keyboard/Mouse
50 - 53h	On-board Timer/Counters
4Fh	SIO IO Data (Write Only)
4Eh	SIO IO Index (Write Only)
40 - 43h	On-board Timer/Counters
30 - 3Dh	On-board Master Interrupt Controller
2Fh	IPMC IO Data
2Eh	IPMC IO Index
24 - 2Dh	Interrupt Controller
20 - 21h	On-board Master Interrupt Controller
0 - 1Fh	On-board Master DMA Controller

Analog Video Interface

The CPC5505 provides access to video at the faceplate through J11 or through the rear-panel I/O connector J5, using integrated graphics support from the Intel 855GME. Video connector J11 is a standard 15-pin D shell connector. See Section 8, "Connectors," for connector locations and pinout information.

A small portion of the system RAM is devoted to the 855GME video memory. The 855GME can be set to consume between 4 MB and 32 MB of system RAM for video memory (see the table "Shared Video RAM"). In most cases it is best to let the Performance Technologies Embedded BIOS set the video memory size (select the default, "automatic," in the BIOS setup menu). Setting the video memory size to less than 1.5625% of the total system memory results in areas of uncached system memory, which significantly impacts overall system performance.

Table 2. Shared Video RAM

System RAM	Video Memory
2 GB	32 MB
1 GB	16 MB
512 MB	8 MB
256 MB	4 MB

The CPC5505 must be used with an analog monitor. If your monitor is capable of both digital and analog modes, be sure it is set to analog.

The CPC5505 can be used in a wide variety of video applications. To ensure the best quality display, take into account such factors as environment, noise from surrounding equipment, video mode, distance from video source, and cabling.

The analog video signals are comprised of a horizontal and vertical sync and three color signals (red, green, and blue). The signals are driven by a RAMDAC, which is used to convert the digital video data to analog signals. The RAMDAC's analog outputs have an impedance of 75 Ω. Ideally, the connection to this output should use high-quality 75 Ω shielded cable.

2.5 Video BIOS

The video BIOS provides low-level control of the VGA controller. It is used to interpret higher-level commands and transform them into register-level instructions that the VGA controller can understand. The CPC5505's BIOS is fully IBM VGA and VESA compatible. The BIOS is automatically installed during system initialization and is mapped to the standard C0000 to C7FFFh VGA BIOS memory space.

2.6 Connectivity

The CPC5505 provides several connectors for interfacing to application-specific devices. Refer to Section 8, "Connectors," for complete connector descriptions and pinouts.

2.7 Switches

The CPC5505 provides switch configuration options for features that cannot be provided through the BIOS Setup utility discussed in the "BIOS Configuration Overview" topic. Refer to "Switch Options and Locations" in Section 3 for location figures and descriptions.

2.8 BIOS Configuration Overview

This topic presents a brief introduction to the Performance Technologies Embedded BIOS. For more detailed information about the BIOS and other utilities, see the *Performance Technologies Embedded BIOS (AMI Core) Software Manual*.

The Performance Technologies Embedded BIOS has many separately configurable features. These features are selected by running the built-in Setup utility. The system configuration settings are saved in a portion of the battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot-up or reset. The configuration is protected by a checksum word for system integrity.

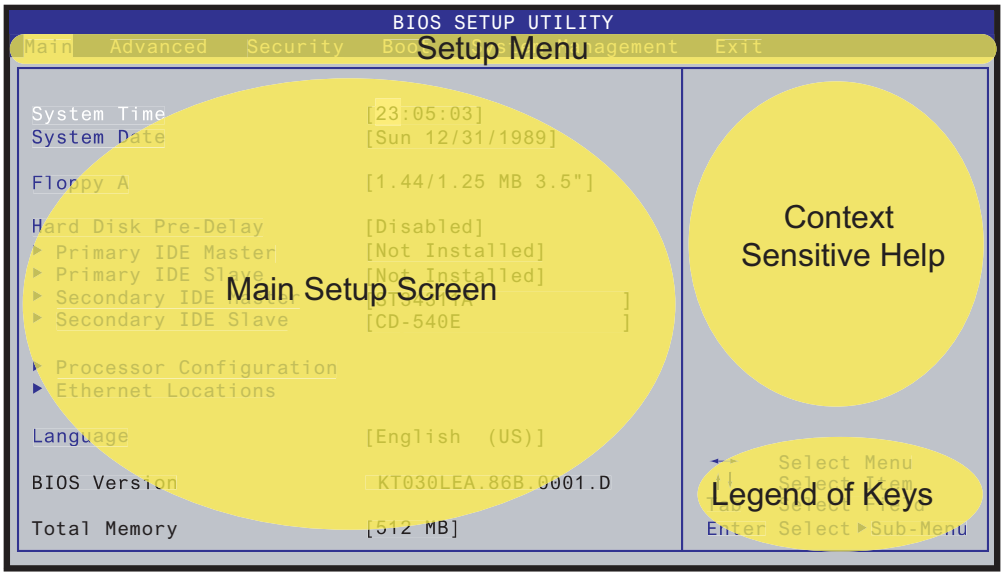
To access the Setup utility, press the **F2** key during POST test and initialization at boot time. Setup runs once the POST functions complete.

When Setup runs, an interactive configuration screen displays. See the "Setup Screen Layout" illustration for an example. Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the Setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the Setup screen. Context-sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the Setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the + or – keys to change the value of a parameter.

Items in the main portion of the screen that have a triangular mark to their left are submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press the **Enter** key.

Figure 7. Setup Screen Layout



Console Redirection

Console redirection allows users to monitor the CPC5505's boot process and to run the CPC5505's Setup utility from a remote serial terminal. Connection is made either directly through a serial port or through a modem.

The console redirection feature is most useful in cases where it is necessary to communicate with a processor board, such as the CPC5505, in an embedded application without video support.

The console redirection option in the BIOS can be overridden by hardware switch 4-1. Console Redirection is enabled by default in the BIOS but is disabled by default by the hardware switch. See the "Switch Options and Locations" topic in Section 3 for more information.

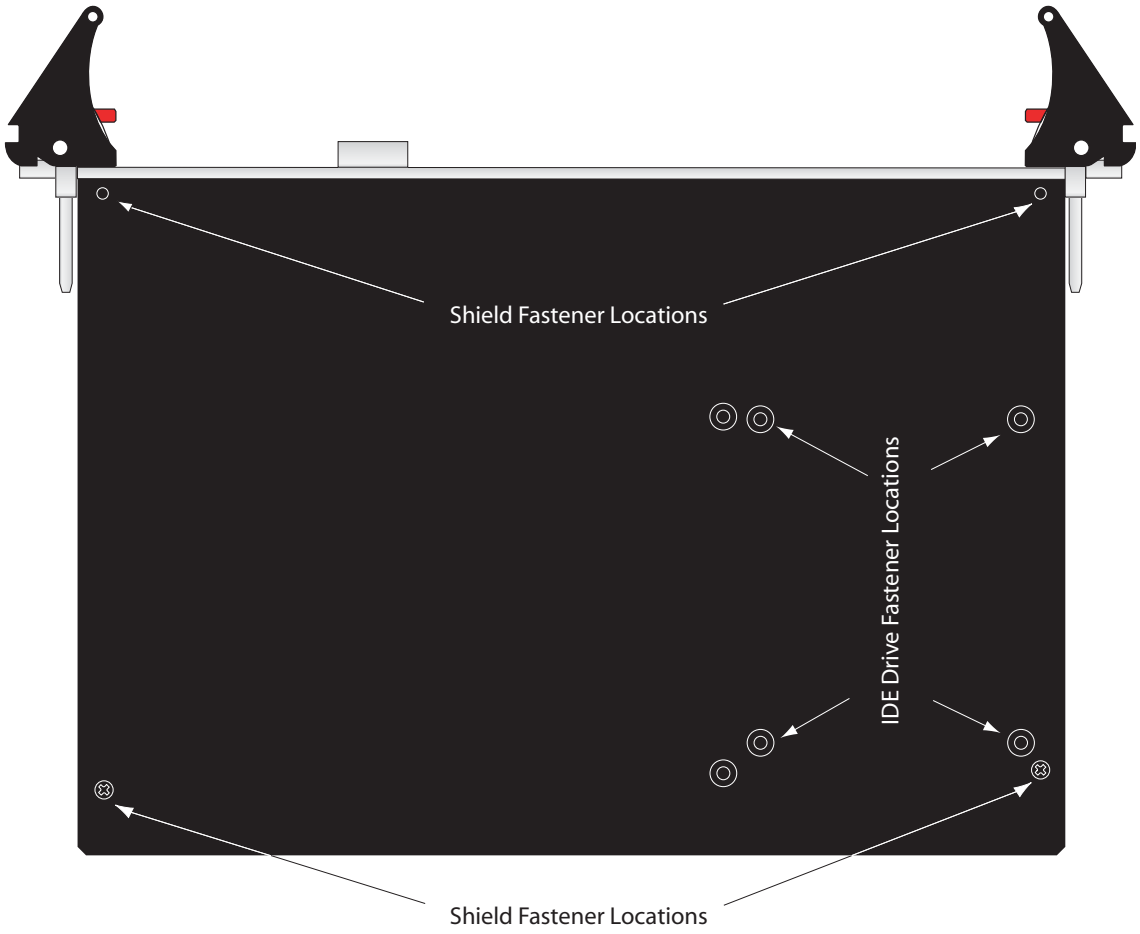
See the *Performance Technologies Embedded BIOS (AMI Core) Software Manual* for more information about console redirection.

2.9 Installing an IDE Drive

The drive mounts to the CPC5505 IDE interface J13 via an IDE header adapter bracket. See the "IDE Drive Replacement" figure.

1. To uncover the IDE drive fastener locations, take off the black shield from the solder side of the board by removing the four shield fasteners (see the "Solder-Side Shield" figure).

Figure 8. Solder-Side Shield



2. Assemble the drive and bracket by mating the drive pins with the adapter bracket socket as shown in the "IDE Drive Replacement" figure. The mounting holes on the bottom of the drive should align with the standoff holes on the bracket.

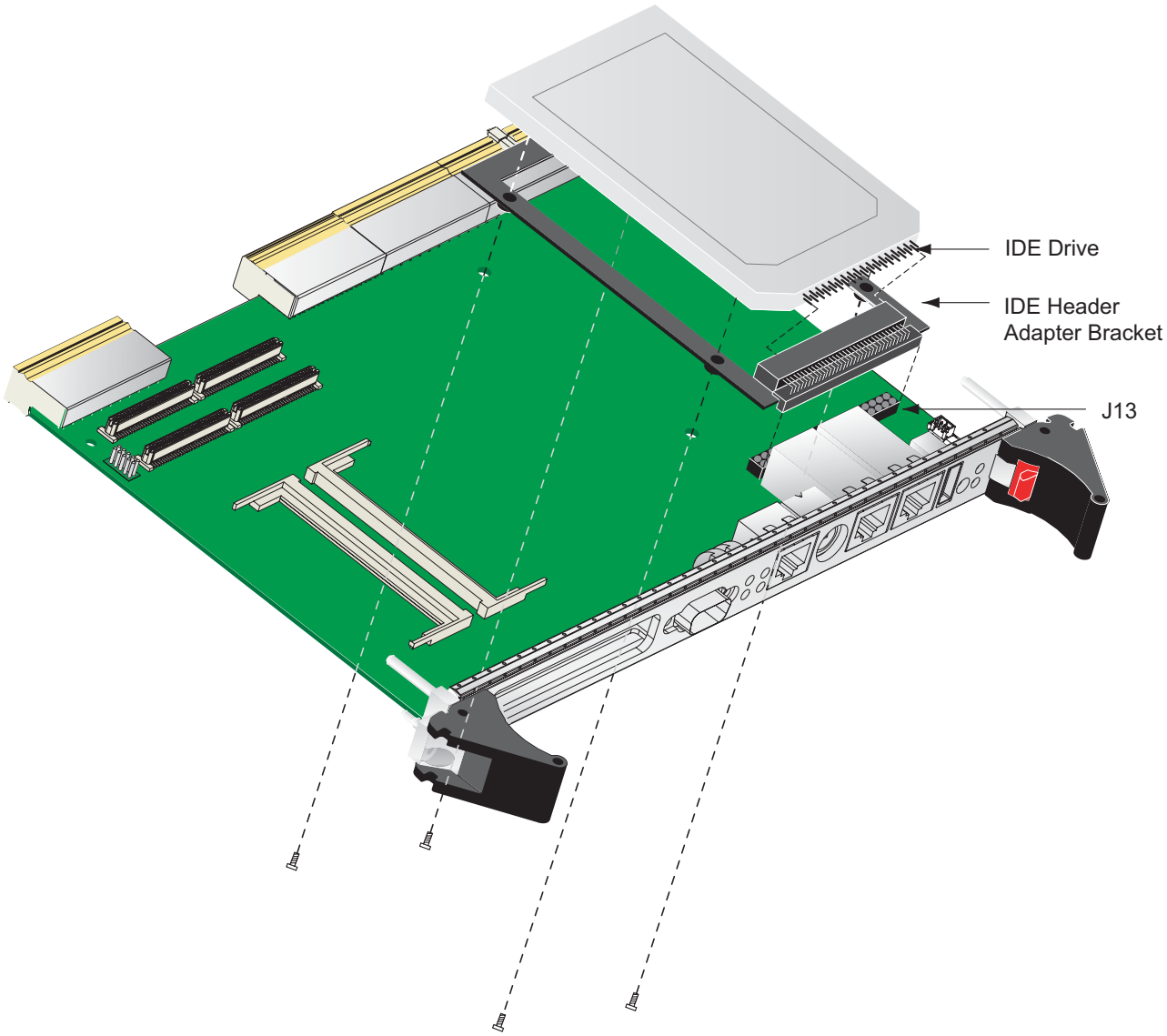
3. Insert the drive and bracket into connector J13. The bracket standoffs should align with the fastener locations on the CPC5505.

4. Secure the drive with four flathead screws as shown in the "IDE Drive Replacement" figure.

5. Replace the solder-side shield, making sure the front edge of the shield is tucked under the faceplate.

6. Replace the four shield fasteners.

Figure 9. IDE Drive Replacement



2.10 Installing a PTMC Device

The following instructions are for mounting a PTMC device on the CPC5505. Refer to the figure "PTMC Card Installation" when installing the PTMC device.

Caution: Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. We recommend using anti-static grounding straps and anti-static mats to help prevent damage due to electrostatic discharge when installing the PTMC device.

1. Take the necessary precautions to protect from static discharge the PTMC, CPC5505, and any other devices you are working with.

2. If the CPC5505 includes a filler plate covering its PTMC opening, remove it.

3. If the CPC5505 includes a protective cover on its solder side, remove it if necessary. See "Installing an IDE Drive" for directions.

4. Lay the CPC5505 solder-side down on a flat surface covered with an anti-static mat.

5. Insert the PTMC front panel into the CPC5505 front panel PTMC opening.

6. Align the CPC5505 3.3V or 5V voltage key post with the corresponding hole in the PTMC.

7. Align the PTMC device's PTMC connectors with the CPC5505 PTMC connectors and press together until the connectors are completely engaged.

8. After the PTMC connectors are properly seated, check that the PTMC device standoffs are flush with the appropriate holes on the CPC5505.

9. Insert four insulating Kapton washers in two locations between the PTMC card and the CPC5505 PC board to prevent shorting. These washers can be obtained from Seastrom Manufacturing Co (1-800-634-2356), Seastrom PN: 5611-41-5, or from Performance Technologies. See the "Kapton Washer Locations" illustration for correct washer placement.

   Note: The following PCB assemblies require Kapton washers. All other PCBs do not. See the "Kapton Washer Locations" illustration for the location of the label identifying the PCB assembly. "x" in the following numbers represents any number.

   120P0453xx
   920P1173xx
   120P14531x
   120P14532x
   120P14533x

10. Insert screws through the CPC5505 and into the standoffs.

11. Tighten screws to 2 to 4 in/lbs.

12. If appropriate, reattach the solder-side cover to the CPC5505.

Figure 10. PTMC Card Installation

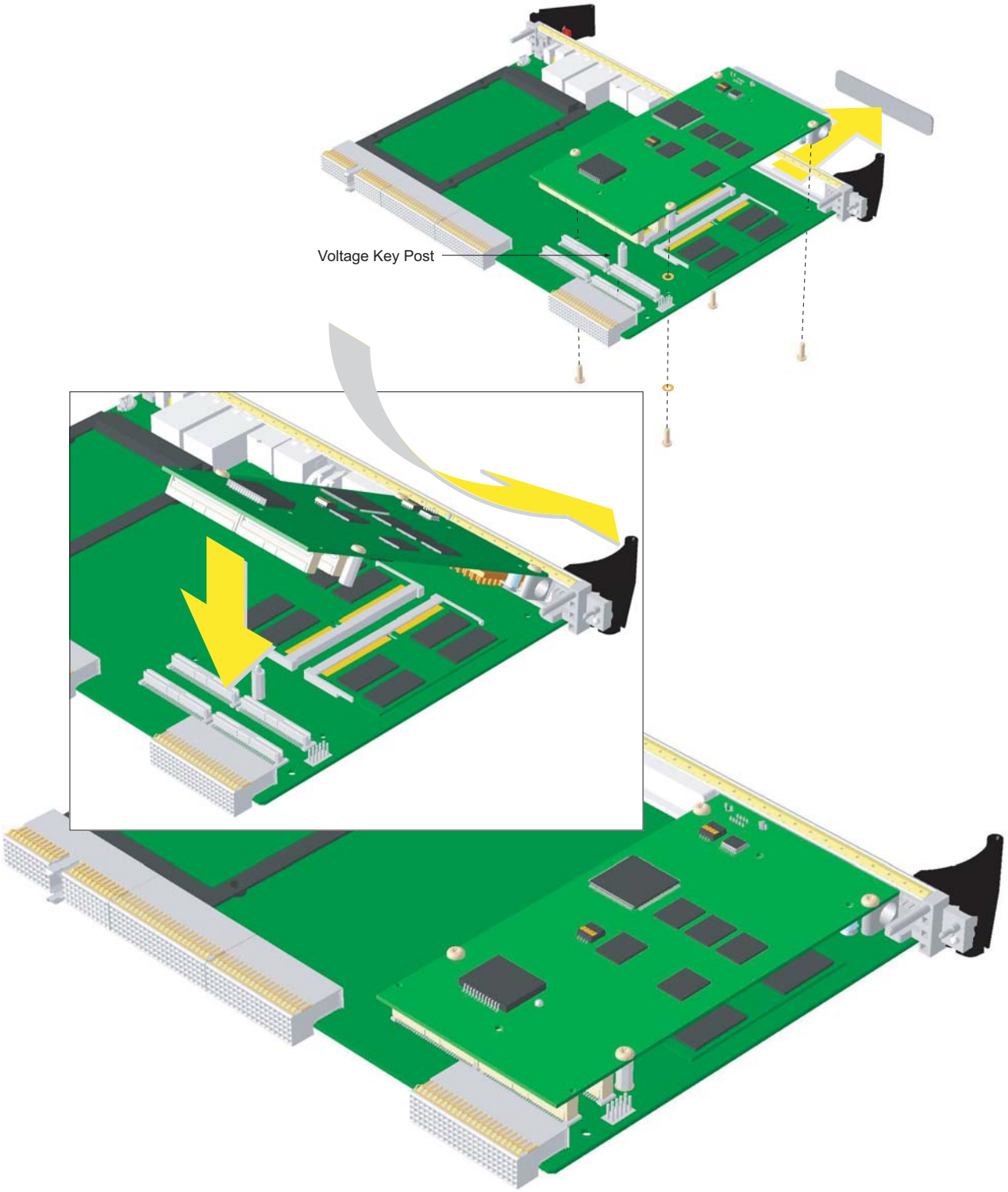
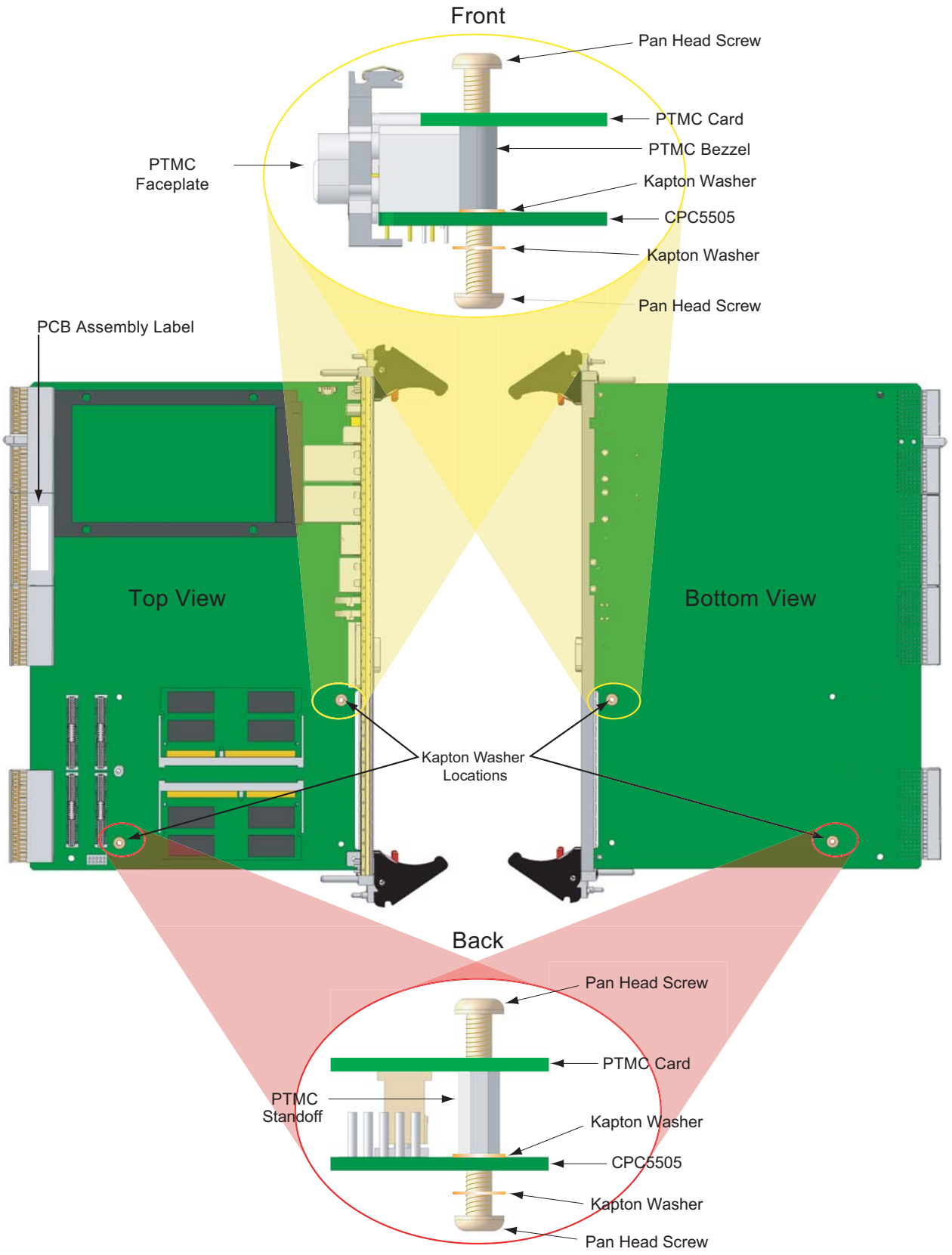


Figure 11. Kapton Washer Locations



2.11 Installing the Operating System

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor and to the Performance Technologies Web site.

To install the operating system:

1. Install peripheral devices. CompactPCI devices are automatically configured by the BIOS during the boot sequence.

2. Most operating systems require initial installation on a hard drive from a floppy or CD-ROM drive. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.

3. Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any readme files or documents provided with the OS as these typically note documentation discrepancies or compatibility problems.

4. Select the appropriate boot device order in the Setup boot menu depending on the OS installation media used. For example, if the OS includes a bootable installation floppy, select **Removable Media** as the first boot device and reboot the system with the installation floppy installed in the floppy drive. (Note that if the installation requires a non-bootable CD-ROM, it is necessary to boot an OS with the proper CD-ROM drivers in order to access the CD-ROM drive). To boot from a USB CD-ROM, first connect the USB drive, then enter the BIOS Setup utility and move the “CD-ROM” device to the top of the boot list (or above any other bootable devices). To boot a USB Floppy, connect the floppy device to the board, then enter the BIOS Setup utility, move “Removable Devices” to the top of the boot order on the Boot screen, and then move the USB floppy device to the top of the removable devices list.

5. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of IPnexus products.

6. When installation is complete, reboot the system and set the boot device order in the Setup boot menu.

7. The Flash Write Protect/Write Enable switch, SW4-1, must be open when installing an operating system image into flash. See “SW3-1 (Flash Write Protect/Write Enable)” in Section 3 for more information.

2.12 Programming the LEDS

The CPC5505 includes two user-controlled, bi-color (amber/green), LEDs located on the faceplate. The user LEDs are software programmable through bits 0-3 of the Video/LED Control Register (Port E5h). The LEDs are turned off after a power cycle or a reset.

As shown below, two bits each are used to control the state of User LEDs 0 and 1. Since bi-color LEDs are used, there are three states for each LED: amber, green, and off. Both LEDs may be turned off or on at the same time.

	S T A T E			
User LED 1	**Amber**	**Green**	**Both Off**	**Both On**
Bit 2	1	0	0	1
Bit 3	0	1	0	1
User LED 2				
Bit 0	1	0	0	1
Bit 1	0	1	0	1

The LED bits are in the same register as other functions. It is important not to change the state of other bits in this register when modifying the User LED status. The following code demonstrates the mechanism for modifying the bits for User LED 1:

```
; set USER LED 1 ON (GREEN)
cli                          ; clear interrupts
in    al, E5h                ; read current state
and   al, F3h                ; preserve other register bits
or    al, 08h                ; set USER LED 1 (GREEN and enabled)
out   E5h, al                ; output new value for register
sti                          ; re-enable interrupts
; set USER LED 1 ON (AMBER)
cli                          ; clear interrupts
in    al, E5h                ; read current state
and   al, F3h                ; preserve other register bits
or    al, 04h                ; set USER LED 1 (AMBER and enabled)
out   E5h, al                ; output new value for register
sti                          ; re-enable interrupts
; set LED OFF
cli                          ; clear interrupts
in   al, E5h                 ; read current state
and   al, F3h                ; clear bits 2 and 3 to turn off LED
out  E5h, al                 ; output new value for register
sti                          ; re-enable interrupts
```

Section

3 Configuration

The CPC5505 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS Setup mechanism (discussed in the topic "BIOS Configuration Overview" in Section 2). Some options cannot be software controlled and are configured with switches. Closing or opening the desired switch selects each switch's options. This section details the CPC5505's switch options.

3.1 Switch Options and Locations

The CPC5505 contains three banks of switches located on the component side of the board (SW2-SW4). S1 is a push-button switch located on the faceplate.

The "Factory Default Switch Configuration" figure shows the CPC5505's switch settings as shipped from the factory. The "Customer Switch Configuration" figure provides a blank switch layout; print this figure and use it to document your switch configuration if it differs from the factory default. This will allow you to restore your configuration if it is changed for any reason.

The "CPC5505 Switch Cross-Reference" table presents the switch options by function.

Table 3. CPC5505 Switch Cross-Reference

Function	Switch
BMC CPU Power Override	SW3-4
Boot Source	SW3-2
Clear RTC CMOS	SW2-1
Console Redirection	SW4-1
CPU Reset	SW1 (push button on the faceplate)
Drone Reset Control	SW3-3
Ethernet Port Select	SW2-2
Flash Write Protect/Write Enable	SW3-1
PCI-X Enable	SW2-4
User Defined	SW4-2,3,4
Video Select	SW2-3

Figure 12. Factory Default Switch Configuration

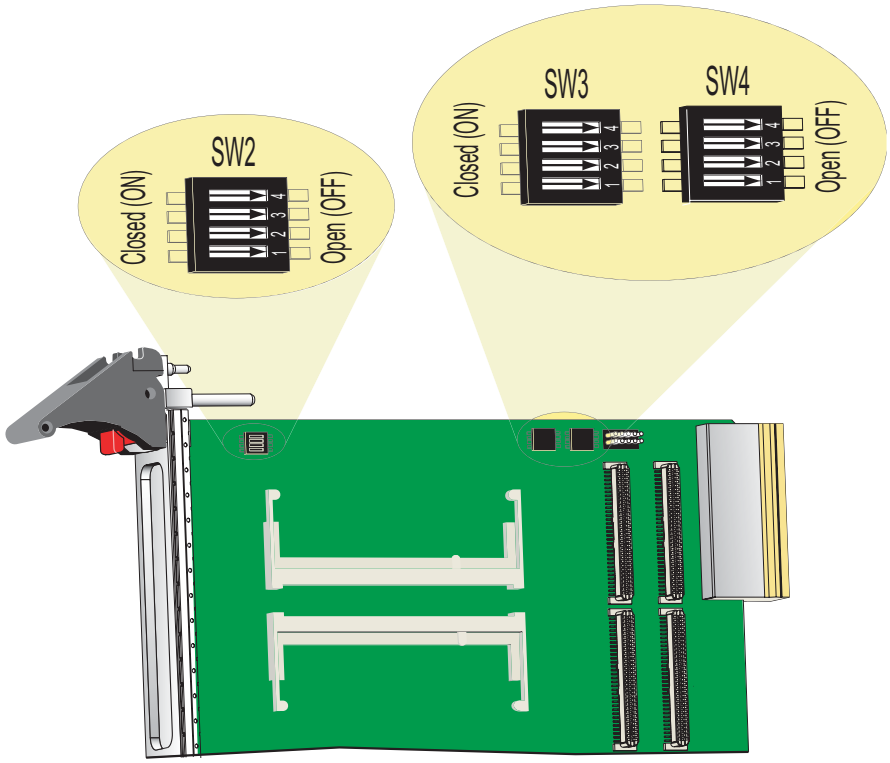
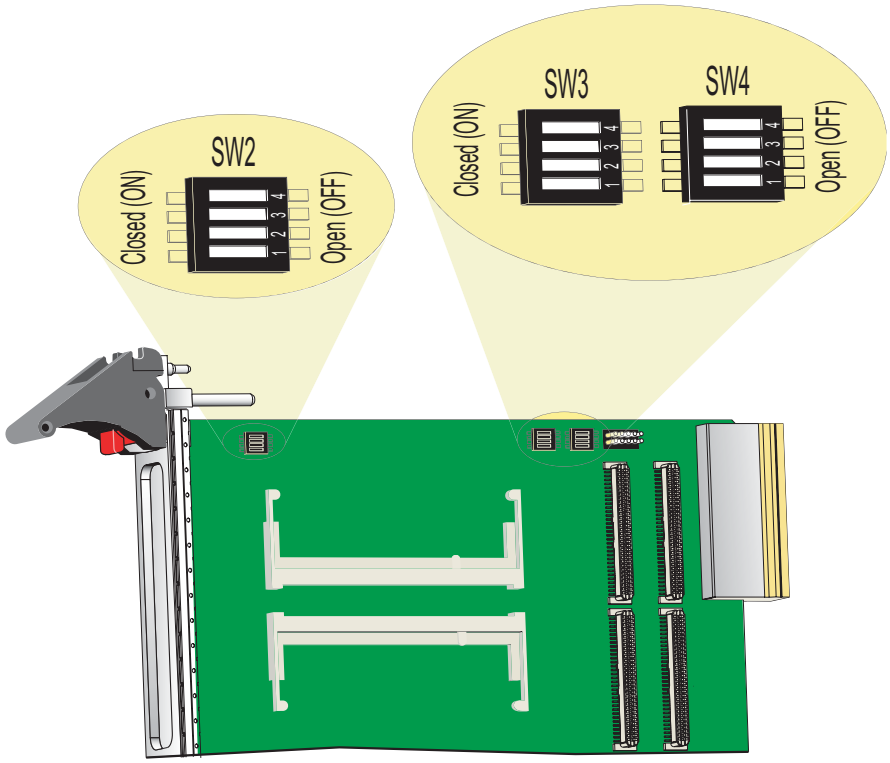


Figure 13. Customer Switch Configuration



3.2 Switch Descriptions

The following topics present the switches in numerical order and provide a detailed description of each switch. Multiple-position switches are identified in the form **SWx-N**, where **x** is the switch number and **-N** is the switch position (for example, SW3-2 means “switch number 3, position 2”).

SW1 (CPU Reset)

SW1 is a push button on the CPC5505’s faceplate. When pressed with a short pulse, SW1 issues a Reset Request to the CPU. Pressing on the switch for 2 seconds or more forces a hard CPU reset.

SW2-1 (Clear RTC CMOS)

SW2-1 is used for clearing CMOS memory and RTC configuration bits. The factory default sets SW2-1 to the open position. To clear CMOS, power down the processor board and close SW2-1. After two seconds, return SW2-1 to the open position. When the processor board is booted, the BIOS clears the RTC CMOS array.

SW2-1		Function
Open	Default	Normal operation– battery backed CMOS
Closed		Clear CMOS (return to open position before rebooting)

SW2-2 (Ethernet Port Select)

SW2-2 is used to route Ethernet to the faceplate Ethernet connectors. By default (SW2-2 open), the CPC5505 is configured to allow the BIOS to determine Ethernet access as configured in the BIOS setup. Close SW2-2 to override the BIOS settings and force Ethernet to faceplate connectors J7 and J8.

SW2-2		Function
Open	Default	Ethernet ports software controlled through BIOS setup utility
Closed		Force Ethernet to faceplate connectors

SW2-3 (Video Select)

SW2-3 is used to route video signals to the faceplate. By default (SW2-3 open), the CPC5505 is configured to allow the BIOS to determine Video signal access as configured in the BIOS setup. Close SW2-3 to override the BIOS settings and force video to the faceplate connector J11.

SW2-3		Function
Open	Default	Video ports software controlled through BIOS setup utility
Closed		Force video to faceplate connectors

SW2-4 (PCI-X Enable)

SW2-4 is used to force the onboard 64-bit/66MHz bus to operate in PCI mode (default is PCI-X mode). The onboard 64/66 bus is routed to the Intel 82546 Ethernet controller and the PMC site. The factory sets SW2-4 to open to enable PCI-X operation. Close SW2-4 to force the onboard 64/66 bus to operate in PCI mode.

SW2-4		Function
Open	Default	PCI-X mode capable.
Closed		PCI mode only.

SW3-1 (Flash Write Protect/Write Enable)

Closing SW3-1 write-protects the BIOS portion of flash memory. Open SW3-1 when installing an operating system image (such as VxWorks) into flash or when using the FLASH.EXE utility to recover from a corrupted BIOS. The status of this switch can be read back at the Flash Write-Protect Status bit of the Switch Monitor register (Port E3h, bit 7). Factory default is open. The Flash Write Enable bit of the Flash Control register (Port 78h, bit 7) must also be properly set to write to flash.

SW3-1		Function
Open	Default	BIOS read/write
Closed		BIOS read only

SW3-2 (Boot Source)

Open this switch to boot from flash (normal operation). Close this switch to recover from a corrupted BIOS. This allows the CPC5505 to boot from the BIOS Recovery Module. See Section 6, "BIOS Recovery," for more information. The status of this switch can be read back at the Boot Source Monitoring bit of the Switch Monitors register (Port E3h, bit 6). Factory default is open.

NOTE: The BIOS Recovery Module Override Bit (Port 78h, bit 6) must be set to 0 for this switch to be operational.

SW3-2		Function
Open	Default	Boot from Flash
Closed		Boot from BIOS Recovery Module

SW3-3 (Drone Reset Control)

Closing SW3-3 allows the backplane PCI Reset signal to be ignored when the CPC5505 is used in a peripheral slot (Drone Mode). Factory default is open.

SW3-3		Function
Open	Default	Ignore backplane PCI Reset
Closed		Drone PCI Reset Enabled

SW3-4 (BMC CPU Power Override)

Close this switch to disable the BMC functionality or to recover from a loss of the BMC flash memory (update mode). Factory default is open.

SW3-4		Function
Open	Default	Normal BMC operation
Closed		BMC flash update mode (recovery only).

SW4-1 (Console Redirection)

Close this switch to enable console redirection. The status of this switch can be monitored by user software through the Switch Monitors register (Port E3h Bit 0). When open, this switch reads back a 0; when closed it reads back a 1. Factory default is open.

SW4-1		Function
Open	Default	Console redirection disabled
Closed		Console redirection enabled

SW4-2, SW4-3, SW4-4 (User Defined)

These switches can provide configuration information to user software. The Software Configuration bits of the Switch Monitors register (Port E3h Bits 1-3) monitor the status of SW4 segments as listed below. An open switch reads back a 0; a closed switch reads back a 1. The switch segments correspond to register bits as follows:

SW4-2 = Bit 1, **SW4-3** = Bit 2; **SW4-4** = Bit 3

Section

4 IDE Interface

This section provides an introduction to the CPC5505's IDE interface controller. It documents the CPC5505's support for local and remote IDE disk drives. The CPC5505 supports ATAPI devices (such as CD-ROM drives) and ATA devices.

The CPC5505's IDE interface provides two IDE channels for interfacing with up to three IDE devices. The primary IDE channel provides Ultra ATA/100 operation. The secondary IDE channel supports Ultra ATA/33 data transfers.

The IDE controller is incorporated into the Intel 6300ESB ICH Chipset, which uses the Intel Hublink architecture. The IDE interface can sustain a maximum transfer rate of 100 MBps between the IDE drive buffer and the Intel Hublink.

The "Chipset" topic in Section 14 provides a link to the Intel 6300ESB ICH Chipset data sheet.

4.1 CPC5505 IDE Interface Features

- IBM-AT compatible
- Supports PIO and Bus Master EID
- Ultra DMA/100 synchronous DMA operation on primary channel
- Bus Master IDE transfers up to 100 MB/s on primary channel
- Primary and secondary channels for interfacing up to three devices
- On-board IDE drive
- Individual software control for each IDE channel

4.2 Disk Drive Support

The CPC5505 supports either internal or external IDE drives. These configurations are described below. Connector locations and pinouts are documented in Section 8, "Connectors."

Primary IDE Channel

The CPC5505 primary IDE channel is directed to internal 50-pin (2mm) IDE connector J13. Connector J13 is normally populated and is intended to connect to a 2.5 inch, low-profile hard drive. The on-board IDE interface requires a carrier to mount the hard drive to the CPC5505. This carrier is included if the CPC5505 is ordered with a hard drive.

Secondary IDE Channel

The CPC5505 secondary IDE channel is routed to rear-panel I/O connector J5, providing an optional transition board (such as the ZT 4807 or ZT 4808 Rear Transition Module) signals for up to two external IDE devices.

4.3 I/O Mapping

The I/O map for the IDE interface varies depending on the mode of operation. The default mode is *compatibility mode*, which means that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h, and interrupt IRQ15. No memory addresses are used.

Section

5 Watchdog Timer

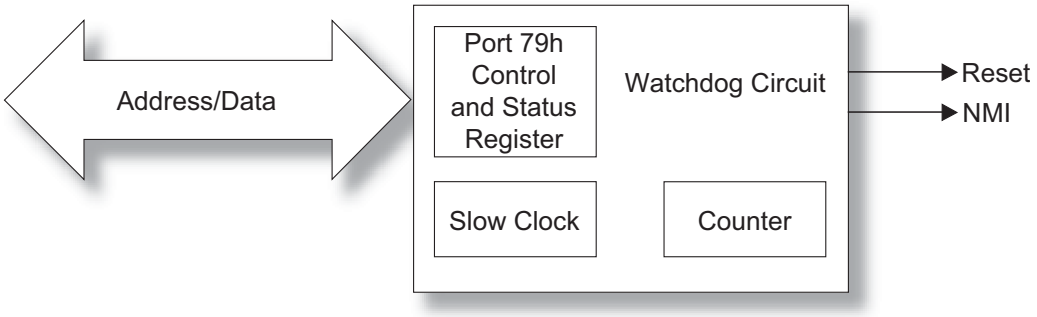
This section explains the operation of the CPC5505's watchdog timer. It provides an overview of watchdog operation and features, as well as sample code to help you learn how the watchdog timer works with applications.

5.1 Overview

The primary function of the watchdog timer is to monitor CPC5505 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are:

- Two-stage operation
- Enabled and disabled through software control
- Armed and strobed through software control

Figure 14. Watchdog Timer Architecture



The CPC5505's custom watchdog timer circuit is implemented in a programmable logic device. The watchdog timer contains a Control and Status register (referred to in this document as the Watchdog register, Port 79h. See Section 10 for the Watchdog register description). The register allows the BIOS or user application to determine the source of a particular reset (watchdog time-out, power-up, power out-of-range/low voltage, and so on). When the watchdog times out, it drives an NMI and RST. Watchdog NMI and RST can be independently disabled through the Watchdog register.

Eight timeout intervals are selectable from the Watchdog register, ranging from a minimum timeout period of 250 ms to a maximum timeout period of 256 seconds. The watchdog is strobed by reading the Watchdog register. This resets the timer. If the timer is not reset within the timeout interval, the watchdog timer drives an NMI followed by RST 250 ms later. The NMI gives the application 250 ms to perform essential tasks before the hardware is reset.

Power-Up Initialization

The watchdog timer's programmable logic is initialized only at power-up. This ensures that the NMI, RST, NMI ENABLE, and RESET ENABLE status and control bits power up to unasserted states, allowing the BIOS or user applications to determine the reset source (watchdog time-out, power-up, power out-of-range/low voltage, and so on).

Time-Out Values

The watchdog timer has its own separate slow clock source. This clock runs at a maximum frequency of 32 Hz (25 Hz nominal—because this slow clock is based on an RC oscillator, the nominal timeout period is approximately 30% longer than the minimum value). The watchdog is guaranteed to time-out in no less than the programmed minimum value.

5.2 Using the Watchdog in an Application

The following topics help you learn how to use the watchdog in an application. They describe the watchdog's reset and NMI functions and provide sample code. Watchdog reset and NMI are controlled through the watchdog's Control and Status register (referred to in this document as the Watchdog register, Port 79h). See the "Watchdog" topic in Section 10 for more information.

Watchdog Reset

An application using the reset feature:

1. Enables the watchdog reset
2. Sets the terminal count period
3. Periodically strobes the watchdog to keep it from resetting the system
4. If a strobe is missed, the watchdog assumes that an application error has occurred and resets the system hardware

Enabling the Watchdog Reset

C code for enabling the watchdog reset might look like the following:

```
#define WD_RESET_EN_BIT_SET      0x20
void EnableWatchdogReset(void){
   unsigned char WdValue;               // Holds watchdog register values.
                                        //
   WdValue = inb(WD_CSR_IO_ADDRESS);    // Read the current contents of the watchdog //
                                        register.
```

```
   WdValue |= WD_RESET_EN_BIT_SET;       // Assert the enable bit in the local copy.
   outb(WD_CSR_IO_ADDRESS,WdValue);      // Assert the enable in the watchdog
                                         // register.
}
```

Setting the Terminal Count

The terminal count determines how long the watchdog waits for a strobe before resetting the hardware. C code for setting the terminal count might look like the following:

```
#define WD_CSR_IO_ADDRESS        0x79    // IO address of the watchdog
#define WD_T_COUNT_MASK   0x07    // Bit mask for terminal count bits.
#define WD_500MS_T_COUNT  0x01    // Terminal count values . . . .
#define WD_1S_T_COUNT             0x00    //
#define WD_250MS_T_COUNT  0x00    //
.
.
.
void SetTerminalCount(void){
   Unsigned char WdValue;                // Holds watchdog register values.
                                         //
   WdValue = inb(WD_CSR_IO_ADDRESS);     // Get the current contents of the watchdog //
                                         register.
   WdValue &= ~ WD_T_COUNT_MASK;         // Mask out the terminal count bits.
   WdValue |= WD_500MS_T_COUNT;          // Set the desired terminal count.
   outb(WD_CSR_IO_ADDRESS,WdValue);      // Furnish the watchdog register with the new
                                         // count value.
}
```

Strobing the Watchdog

Once the watchdog is enabled, it must be strobed within the terminal count period to avoid resetting the system hardware. C code to strobe the watchdog might look like the following:

```
void StrobeWatchdog(void){
   inb(WD_CSR_IO_ADDRESS);               // A single read is all it takes.
}
```

Watchdog NMI

When enabled, an NMI precedes a watchdog reset by 250 ms. The NMI generation feature gives the application 250 ms to perform essential tasks before the hardware is reset. Before using watchdog NMI, ensure the following:

- The code for performing the essential tasks is included in an interrupt service routine (ISR)

- The ISR is chained to the existing NMI ISR
- The watchdog NMI is enabled

Chaining the ISRs

Save the original NMI ISR vector so that it can be invoked from the new watchdog NMI ISR. Alter the interrupt vector table so that the NMI ISR vector is overwritten with a vector to the watchdog ISR. C code to do this in DOS might look like the following:

```
#define NMI_INTERRUPT_VECTOR_NUMBER 2

void interrupt far (*OldNMIIsr)();

void HookWatchdogIsr(void){

   //
   // To be absolutely certain the interrupt table is not accessed by an NMI (This is
   // quite unlikely.), the application could disable the NMI in the chipset before
   // installing the new vector.
   //
                          .
                          .
                          .
   //
   // Install the new ISR.
   //
   OldNMIIsr = getvect(IsrVector);                          // Save the old vector.
   setvect(NMI_INTERRUPT_VECTOR_NUMBER, WatchdogIsr);   // Install the new.
}
```

Enabling the Watchdog NMI

To activate the NMI feature, enable it in the Watchdog register (Port 79h). The code to do this might look like the following:

```
#define WD_NMI_EN_BIT_SET 0x10

void EnableWatchdogNMI(void){

   unsigned char WdValue;              // Holds watchdog register values.

                                       //

   WdValue = inb(WD_CSR_IO_ADDRESS);   // Read the current contents of the watchdog //
                                       register.

   WdValue |= WD_NMI_EN_BIT_SET;       // Assert the enable bit in the local copy.

   outb(WD_CSR_IO_ADDRESS,WdValue);    // Assert the enable in the watchdog

                                       // register.
```

```
}
```

NMI Handler

Because the NMI may have originated from another source such as a RAM Error Correction Code (ECC) error, the NMI handler cannot assume that the NMI occurred due to a watchdog time out. Therefore, the NMI handler must check the Watchdog Status register before taking watchdog-related emergency action. When the NMI handler completes handling the emergency, it invokes the original NMI handler. The code to do this might look like the following:

```
#define WD_NMI_DETECT_BIT_SET    0x40           // Bit that indicates a NMI occurred, set.
                                                //
void WatchdogIsr(void){                         //
                                                //
   //
        // Did the watchdog cause the NMI?
        //
   if(inb(WD_CSR_IO_ADDRESS) & WD_NMI_DETECT_BIT_SET){
                                                //
           TripAlarm();                         // Take care of essential tasks.
                                                //
           TurnOffTheGas();                     //
   }                                            //
   _chain_intr(OldNMIIsr);                      // Invoke the originally installed ISR.
}
```

Other Watchdog NMI Uses

The watchdog NMI feature can be used independently of the watchdog reset feature. Code for checking the bit is provided in the “NMI Handler” topic above.

Section

6 BIOS Recovery

The CPC5505 provides 16 MB of on-board flash memory containing the system BIOS. The PAL uses the flash paging bits in Flash Control register 78h to divide the 16 MB flash into four 4 MB pages mapped into a window in extended memory (FFC00000h–FFFFFFFFh). The current implementation uses only “Page 0” and “Page 1” (bits 0 and 1 in register 78h). The BIOS resides in page 0 of flash (78h = xxxxxx00b). Avoid using either xxxxx000b or xxxxx100b since both pages map to page 0. “Page 2” (bit 2) is not used. “Page 2” was added to the flash control register to support the possible future use of 32 MB parts.

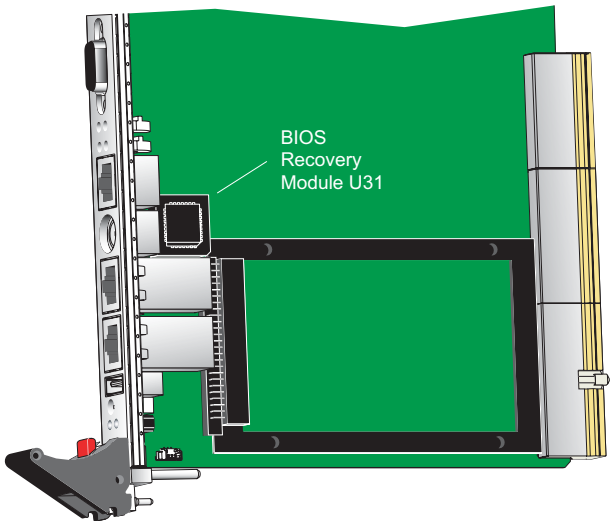
The CPC5505 includes a second flash device, called the BIOS recovery module, programmed with a backup copy of the BIOS. To reprogram the BIOS or update it if it becomes corrupted, use the BIOS recovery module and FLASH.EXE utility.

6.1 BIOS Recovery Module

If the CPC5505 system BIOS stored in on-board flash becomes corrupted, the CPC5505 can boot from an onboard flash device, called the BIOS recovery module, and flash memory can be reprogrammed with the BIOS recovery module image via the FLASH.EXE program.

The board is shipped with the BIOS recovery module installed in a 32-pin socket (U31). If the BIOS recovery module is removed for any reason, ensure that it is correctly oriented when reinstalled. Orient the beveled corner of the BIOS recovery module as shown in the “BIOS Recovery Socket Location” figure below.

Figure 15. BIOS Recovery Socket Location



Forcing a Boot from the BIOS Recovery Module

To force a boot from the BIOS recovery module:

1. Remove the board from the enclosure.
2. Close switch SW3-2 to boot from the BIOS Recovery Module.
3. Make sure flash write protection is disabled (SW3-1 = open).
4. Re-insert the board in the enclosure; apply power to the board. The system should boot.
5. See the "Flash Utility Program" topic below for detailed instructions on reprogramming the on-board flash with the BIOS.
6. After flashing the BIOS, turn off power, remove the board from the enclosure, and open switch SW3-2 to boot from flash.
7. If desired, enable flash write protection by closing switch SW3-1.
8. Re-insert the board in the enclosure.

Flash Utility Program

FLASH.EXE is a utility program that is available for download free from Performance Technologies. Run FLASH.EXE to modify or restore the BIOS in on-board flash memory. FLASH.EXE eliminates the need for a PROM programmer and for removing boards and chips from the system.

Before attempting to program the flash, make sure that switch SW3-1 (Flash Write Protect/Write Enable) is open.

To reprogram the BIOS on the CPC5505, use the following syntax at a DOS prompt:

FLASH /b BIOS.XXX

where **BIOS.XXX** is the BIOS image for the CPC5505. See the *Performance Technologies Embedded BIOS (AMI Core) Software Manual* for more information on the Flash utility.

Section 7

System Monitoring and Alarms

7.1 Overview

The CPC5505 performs system monitoring and alarming functions using the flexible, industry standard, Intelligent Platform Management Interface (IPMI). The CPC5505 comes equipped with an on-board Intelligent Platform Management Controller (IPMC or BMC) chip, IPMI and IPMB J-connector pinouts, and IPMI v1.5 firmware already installed on the board. Some of the functions available on this board through the IPMI interface include:

- Monitoring of the CPU and board temperatures with critical and non-critical alerting
- Monitoring of the voltage rails (+5V, ±12V, +3.3V, +2.5V, VBAT, CPU core voltages) with critical and non-critical alerting
- Remote reset and shutdown of the board
- Monitoring of ejector switches for hot swap functionality
  - Intel IPMI driver and firmware provide features for hot swap
- Monitoring and event recording of critical errors
- Board power up/power down by monitoring BD_SEL# lines on the CompactPCI backplane
- Dual domain capability (this refers to the ability of the BMC to act as either a BMC or as a System Management Controller when there is already a BMC present on the IPMI bus)
- Interface to dual IPMB lines (IPMB 0 and IPMB 1)

In order to take advantage of the features provided by the firmware, IPMI aware applications must be developed. Information on IPMI v1.5 is provided at:

http://www.intel.com/design/servers/ipmi/spec.htm

7.2 BMC Command Line Interface

The following is a description of the BMC Command Line Interface (CLI).

Login

After the banner a prompt appears for an account name and a password:

```
Login:
Password:
```

There are four accounts and associated passwords:

`NULL` - No login name or password

`Operator` - Login name is `Operator`, password is `Operator`

`Administrator` - Login name is `Administrator`, default password is `Administrator`

`OEM` - Login name is `OEM`, default password is `OEM`

NULL and Operator Account Commands

The following commands are available to the NULL and Operator accounts:

`I` <ipmb command data> <enter> - "IPMICommand" executes the IPMI command as if it came in on the IPMB

`SD` <enter> - "SDRRead" displays the Sensor Data Records (SDRs)

`SE` <enter> - "SELRead" displays the contents of the System Event Log (SEL)

`D` <enter> - "D" displays the raw sensor readings

`H` <enter> - "HELP" displays the list of commands

`Q` <enter> - "QUIT" quits the command line interface and prompts for login information

Administrator Account Commands

The following commands are available to the Administrator account:

`C` <enter> - "ChangePassword" changes the password

`I` <ipmb command data> <enter> - "IPMICommand" executes the IPMI command as if it came in on the IPMB

`SD` <enter> - "SDRRead" displays the Sensor Data Records (SDRs)

`SE` <enter> - "SELRead" displays the contents of the System Event Log (SEL)

`D` <enter> - "D" displays the raw sensor readings

`H` <enter> - "HELP" displays the list of commands

`Q` <enter> - "QUIT" quits the command line interface and prompts for login information

OEM Account Commands

The following commands are available to the OEM account:

C <enter> - “ChangePassword” changes the password

P <enable(0,1)> <enter> - “POWER”. "P" displays the current power state. "P 0" turns off power to the board. "P 1" turns on power to the board.

I <ipmb command data> <enter> - "I NetFn/LUN cmd <data>" executes the IPMI command as if it came in on the IPMB

SD <enter> - “SDRRead” displays the Sensor Data Records (SDRs)

SE <enter> - “SELRead” displays the contents of the System Event Log (SEL)

MU <enter> - “MU” displays memory usage data for the various program threads

MP [<block offset>] <enter> - “MP,” memory pool, displays 16 bytes of data (starting at the specified offset) from each used allocated block of the memory pool

MR [<address> [<type> [<n>]]] <enter> - “MR,” memory read. "MR <address>" displays one byte of data from memory location <address>. "MR <address> <type>" displays one quantum of data from memory location <address>; <type> is B (byte), S (short/word), or L (long). "MR <address> <type> <n>" displays n quanta of data from memory starting at location <address>. "MR" repeats the previous MR command at the next memory location.

MW <address> <type> <value> <enter> - “MW,” memory write. Writes <value> to memory location <address>. <type> is B (byte), S (short/word), or L (long).

ST <enter> - “STATISTICS” displays IPMI message statistics for the KCS and IPMB interfaces

A <enter> - “Assert” asserts NMI to the host processor

D <enter> - “D” displays the raw sensor readings

H <enter> - “HELP” displays the list of commands

Q <enter> - QUIT quits the command line interface and prompts for login information

Section

8 Connectors

As shown in the "Connector Locations" figure, the CPC5505 includes several connectors to interface with application-specific devices. A brief description of each connector is given in the "Connector Assignments" table. A detailed description and pinout for each connector is given in the following topics.

Table 4. Connector Assignments

Connector	Location	Function
J1	Backplane	CompactPCI Bus Connector (125-pin, 2 mm x 2 mm, female)
J2	Backplane	CompactPCI Bus Connector (110-pin, 2 mm x 2 mm, female)
J3	Backplane	Rear-Panel Gigabit Ethernet Connector (95-pin 2 mm x 2 mm, female)
J5	Backplane	Rear-Panel User I/O Connector (110-pin, 2 mm x 2 mm, female)
J6	Faceplate	Universal Serial Bus Connector (4-pin, USB, Port 0)
J7, J8	Faceplate	Ethernet A and B Connectors (RJ-45)
J9	Faceplate	Keyboard/Mouse Connector (6-pin DIN)
J10	Faceplate	COM1 Serial Port (RJ-45)
J11	Faceplate	Video Interface (15-pin, D-Shell)
J12	Internal	Hot Swap Ejector Switch Connector (3-pin surface-mount)
J13	Internal	On-board EIDE Interface (50-pin female vertical)
J14, J15	Internal	SDRAM Connectors (200-pin SO-DIMM)
J21-J24	Internal	PTMC Interface

Figure 16. Connector Locations

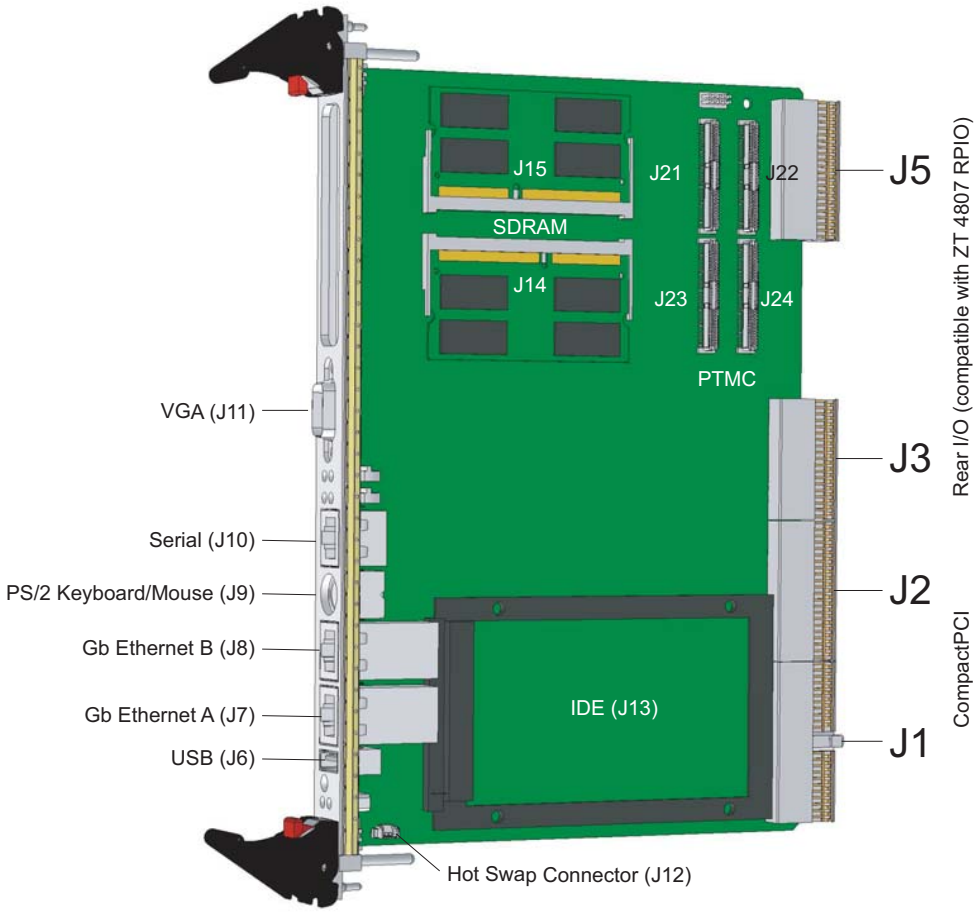
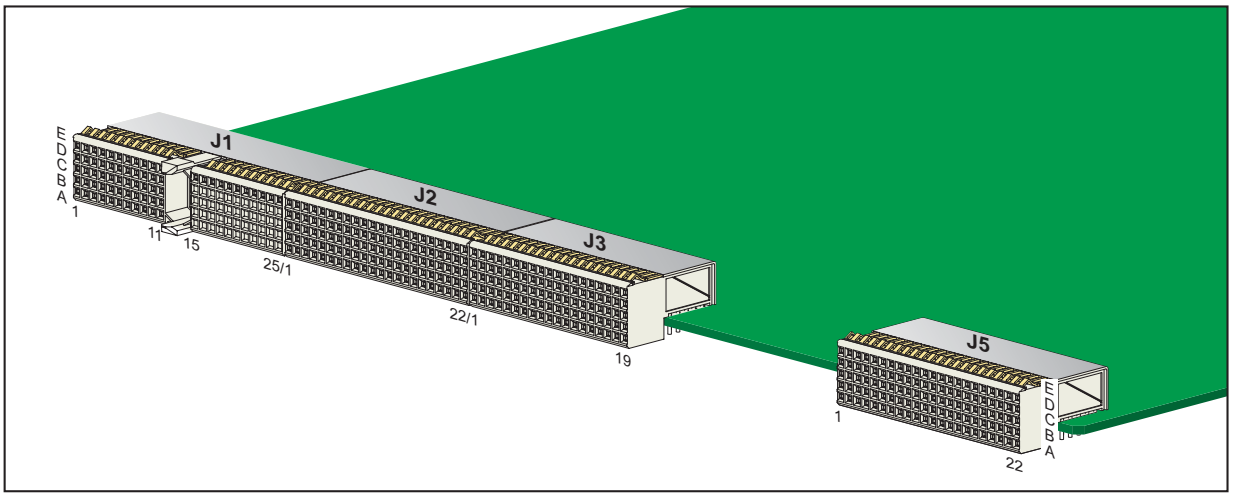


Figure 17. Backplane Connectors Pin Locations



8.1 Backplane Connectors

J1 (CompactPCI Bus Connector)

J1 is a 125-pin, 2 mm x 2 mm, female, 32-bit, CompactPCI connector. Rows 12-14 are used for connector keying. See the "J1 CompactPCI Bus Connector Pinout" table for pin definitions and the "Backplane Connectors Pin Locations" figure for pin placement.

Table 5. J1 CompactPCI Bus Connector Pinout

Pin	A	B	C	D	E	F
25	5V	REQ64#	ENUM#	3.3V	5V	Ground
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	
23	3.3V	AD[4]	AD[3]	5V	AD[2]	
22	AD[7]	GND	3.3V	AD[6]	AD[5]	
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	
19	3.3V	AD[15]	AD[14]	GND	AD[13]	
18	SERR#	GND	3.3V	PAR	C/BE[1]#	
17	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	
16	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	
15	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	
12-14	KEY AREA					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	Shield
10	AD[21]	GND	3.3V	AD[20]	AD[19]	
9	C/BE[3]#	IDSEL (NC)	AD[23]	GND	AD[22]	
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	
6	REQ#	PCI_PRESENT#	3.3V	CLK	AD[31]	
5	BRSVP1A5 (NC)	BRSVP1B5 (NC)	RST#	GND	GNT#	
4	IPMB_PWR	HEALTHY#	V(I/O)	INTP (NC)	INTS (NC)	
3	INTA#	INTB#	INTC#	5V	INTD#	
2	TCK (NC)	5V	TMS (NC)	TDOx (NC)	TDIx (NC)	
1	5V	-12V	TRST# (NC)	+12V	5V	
Pin	**A**	**B**	**C**	**D**	**E**	**F**

= long pins = short pins All others = medium-length pins

NOTE: Row F GND pins are long length, as is standard for CompactPCI.

J2 (CompactPCI Bus Connector)

J2 is a 110-pin, 2 mm x 2 mm, right-angle, female, 64-bit, CompactPCI connector. See the "J2 CompactPCI Bus Connector Pinout" table for pin definitions and the "Backplane Connectors Pin Locations" figure for pin placement.

Table 6. J2 CompactPCI Bus Connector Pinout

Pin #	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	Ground Shield
21	CLK6	GND	RSV (NC)	RSV (NC)	RSV (NC)	
20	CLK5	GND	ALT_SYSEN	GND	RSS_ARB_OUT#	
19	GND	GND	IPMB_SDA	IPMB_SCL	RSS_HS_IN#	
18	BRSVP2A18 (NC)	BRSVP2B18 (NC)	BRSVP2C18 (NC)	GND	BRSVP2E18 (NC)	
17	BRSVP2A17 (NC)	GND	PRST#	REQ6#	GNT6#	
16	BRSVP2A16 (NC)	BRSVP2B16 (NC)	DEG#	GND	BRSVP2E16 (NC)	
15	BRSVP2A15 (NC)	GND	FAL#	REQ5#	GNT5#	
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]	
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	
5	C/BE[5]#	64EN# (NC)	V(I/O)	C/BE[4]#	PAR64	
4	V(I/O)	BRSVP2B4 (NC)	C/BE[7]#	GND	C/BE[6]#	
3	CLK4	GND	GNT3#	REQ4#	GNT4#	
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	
1	CLK1	GND	REQ1#	GNT1#	REQ2#	
Pin #	**A**	**B**	**C**	**D**	**E**	**F**

J3 (Rear-Panel Gigabit Ethernet Connector)

J3 is a 95-pin, 2 mm x 2 mm, female connector providing rear-panel access to Ethernet A and Ethernet B. See the “J3 Rear-Panel Gigabit Ethernet Connector Pinout” table for pin definitions and the “Backplane Connectors Pin Locations” figure for pin placement.

Table 7. J3 Rear-Panel Gigabit Ethernet Connector Pinout

Pin #	A	B	C	D	E	F
19	NC	NC	NC	NC	NC	Ground Shield
18	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	
17	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	
16	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	
15	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	
14	RSV	RSV	RSV	RSV	RSV	
13	RSV	RSV	RSV	RSV	RSV	
12	RSV	RSV	RSV	RSV	RSV	
11	RSV	RSV	RSV	RSV	RSV	
10	RSV	RSV	RSV	RSV	RSV	
9	RSV	RSV	RSV	RSV	RSV	
8	RSV	RSV	RSV	RSV	RSV	
7	RSV	RSV	RSV	RSV	RSV	
6	RSV	RSV	RSV	RSV	RSV	
5	RSV	RSV	RSV	RSV	RSV	
4	RSV	RSV	RSV	RSV	RSV	
3	RSV	RSV	RSV	RSV	RSV	
2	RSV	RSV	RSV	RSV	RSV	
1	RSV	RSV	RSV	RSV	RSV	
Pin #	**A**	**B**	**C**	**D**	**E**	**F**

J5 (Rear-Panel User I/O Connector)

J5 is a 110-pin, 2 mm x 2 mm, female connector providing rear-panel access to the following:

- EIDE
- COM ports
- Ethernet LED
- Video
- Keyboard/Mouse
- Speaker
- USB
- Floppy
- RPIO Eject
- SMBus
- Power and Ground

See the “J5 Rear-Panel User I/O Connector Pinout” table for pin definitions and the “Backplane Connectors Pin Locations” figure for pin placement.

Table 8. J5 Rear-Panel User I/O Connector Pinout

Pin #	A	B	C	D	E	F
22	USBR1	USBR1#	VCC	USBR2	USBR2#	Ground Shield
21	VCC3	GND	GND	GND	GND	
20	RED	GND	H-SYNC	GND	SYS_SDA	
19	GND	VCC	GND	VCC	SYS_SCL	
18	GREEN	GND	V-SYNC	GND	BMC_SMBALERT#	
17	GND	RSV (NC)	RPIO_PRSNT#	RSV (NC)	IPMB_PWR	
16	BLUE	GND	DDCCLKIN	KBD_DAT	KBD_CLK	
15	GND	VCC	DDCDATIN	AUX_DAT	AUX_CLK	
14	S1RTS#	S1CTS#	S1RIN#	S1DTR#	GIG_LINKA#	
13	S1DCD#	S1TXD	S1RXD	S1DSR#	GIG_1000A#	
12	S2RTS#	S2CTS#	S2RIN#	S2DTR#	GIG_LINKB#	
11	S2DCD#	S2TXD	S2RXD	S2DSR#	GIG_1000B#	
10	TRK0#	WP#	RDATA#	HDSEL#	DSKCHG#	
9	MTR1#	DIR#	STEP#	WDATA#	WGATE#	
8	DENSEL	INDEX#	MTR0#	DR1#	DR0#	
7	CS1S#	CS3S#	DAS1	RP_BLUE_LED#	RP_EJECT#	
6	PWROK	SPKR	NMI#	DAS0	DAS2	
5	SDRQ#	SIORDY	SDI0W#	SDDACK#	SDIOR#	
4	DDS14	DDS0	SDASP	DDS15	IRQ15	
3	DDS3	DDS12	DDS2	DDS13	DDS1	
2	DDS9	DDS5	DDS10	DDS4	DDS11	
1	PBRST#	PWRGD	DDS7	DDS8	DDS6	
Pin #	**A**	**B**	**C**	**D**	**E**	**F**

8.2 Front Panel Connectors

J6 (USB Connectors)

J6 is a 4-pin, Port 0 USB Interface connector on the CPC5505's faceplate. USB (Port 1) is directed out rear-panel I/O connector J5. See the "J6 USB Connector Pinout" table for pin definitions.

Table 9. J6 USB Connector Pinout

Pin#	Function
1	+5V Fused
2	DATA-
3	DATA+
4	GND

J7, J8 (Ethernet Connectors)

J7 is a dual RJ-45 connector on the CPC5505's faceplate providing 10 Mbps (10Base-T), 100 Mbps (100Base-T), and 1000 Mbps (1000Base-T) protocols. Two LEDs are located inside each RJ-45 connector:

- Off = 10 Mbps
- Green = 100 Mbps
- Amber = 1000 Mbps
- Green = link
- Flashing green = activity

See the "J7 Ethernet Connectors Pinout" table for pin definitions.

These Ethernet signals can be directed out J3 to the backplane. See the ENUM, WD NMI Status, PWR Supply Status Register (E1h) for more information.

Table 10. J7 Ethernet Connectors Pinout

Pin#	Function	Pin#	Function
1	MDIO0	5	MDIO2#
2	MDIO0#	6	MDIO1#
3	MDIO1	7	MDIO3
4	MDIO2	8	MDIO3#

J9 (Keyboard/Mouse Connector)

J9 is a 6-pin, right angle, DIN connector providing for standard PS/2 style keyboard and mouse device connection on the CPC5505's faceplate. Keyboard and mouse signals are also directed out rear-panel I/O connector J5. See the "J9 Keyboard and Mouse Connector Pinout" table for pin definitions.

Table 11. J9 Keyboard and Mouse Connector Pinout

Pin#	Function	Pin#	Function
1	KBDAT	4	Vcc (Fused)
2	MSDAT	5	KBCLK
3	GND	6	MSCLK

J10 (COM1 Serial Port)

J10 is an 8-pin, RJ-45 connector providing the COM1 interface on the CPC5505's faceplate. COM1 interface signals are also directed out rear-panel I/O connector J5. See the "J10 COM1 Serial Port Pinout" table for pin definitions.

Table 12. J10 COM1 Serial Port Pinout

Pin#	Function	Pin#	Function
1	RTS	5	GND
2	DTR	6	RXD
3	TXD	7	DSR
4	GND	8	CTS

J11 (Video Interface)

J11 is an HD15, 15-pin, female, D-shell connector providing an interface for VGA signals on the CPC5505's faceplate. See the "J11 Video Interface Pinout" table for pin definitions.

Table 13. J11 Video Interface Pinout

Pin#	Signal	Pin #	Signal	Pin#	Signal
1	RED	6	RGND	11	NC
2	GRN	7	GGND	12	SDA
3	BLUE	8	BGND	13	HSYNC
4	NC	9	VCC	14	VSYNC
5	DGND	10	SGND	15	SCL

8.3 Internal Connectors

J12 (Hot Swap Ejector Switch Connector)

J12 is a 3-pin, vertical, 1.25 mm (.049 in), surface-mount connector linking the hot swap switch to the board's lower ejector mechanism. This switch is tied to logic on the CPC5505 to sense a board extraction or insertion. See the "J12 Hot Swap Ejector Switch Connector Pinout" for pin definitions.

Table 14. J12 Hot Swap Ejector Switch Connector Pinout

Pin#	Function
1	Common
2	Latched
3	Unlatched

J13 (EIDE Interface)

J13 is a dual-row, 50-pin, female, 2mm (.079 in) center, vertical socket providing an on-board EIDE interface. See the “J13 EIDE Interface Pinout” table for pin definitions.

Table 15. J13 EIDE Interface Pinout

Pin#	Signal	Pin#	Signal
1	Reset IDE#	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	NC
21	DDRQ	22	Ground
23	DIOW#	24	Ground
25	DIOR#	26	Ground
27	DRDY	28	CSEL
29	DDAK#	30	Ground
31	IRQ 14	32	Reserved
33	IDE_A1	34	Reserved
35	IDE_A0	36	IDE_A2
37	IDE_CS1#	38	IDE_A2
39	IDE_ACT#	40	Ground
41	VCC	42	VCC
43	Ground	44	NC

J14, J15 (DDR SO-DIMM Connectors)

J14 and J15 are 200-pin, right angle connectors that accommodate standard 3.3V unbuffered DDR small outline dual inline memory modules (SO-DIMMs) used for system memory.

J21-J24 (PTMC Interface)

J21-J24 are dual row, vertical stacking, 149 mm x 74 mm, mezzanine IEEE 1386 receptacles providing an on-board PTMC (PCI Telecom Mezzanine Card) interface conforming to the PICMG® 2.15 standard.

Table 16. J21-J24 PTMC Interface Pinout

Pin#	J21	J22	J23	J24
1	NC_TCK-PMCA	+12V	NC_PMCA_PCI_RSVD4	LPA_DA+
2	-12V	NC	GND	LPA_DC+
3	GND	NC	GND	LPA_DA-
4	PMC INTA-	NC	B4_CBE-7	LPA_DC-
5	PMC INTB	NC	B4_CBE-6	GND
6	PMC INTC-	GND	B4_CBE-5	GND
7	PMC1-BUSMODE1	GND	B4_CBE-4	LPa_DB+
8	VCC	NC_PMCA_PCI_RSVD1	GND	LPa_DD+
9	PMC INTD-	NC_PMCA_PCI_RSVD2	PTID2	LPa_DB-
10	NC_PMCA_PCI_RSVD0	NC_PMCA_PCI_RSVD3	B4_PAR64	LPa_DD-
11	GND	PMCA-BUSMODE2	B4_PAD63	GND
12	PMCA-3_3V-AUX	VCC3	B4_PAD62	GND
13	MEZ-PCIX-CLK_66	B0_PCIRST-	B4_PAD61	LPb_DA+
14	GND	PMCA-BUSMODE3	GND	LPb_DC+
15	GND	VCC3	GND	LPb_DA-
16	PMCA_GNT-	PMCA-BUSMODE4	B4_PAD60	LPb_DC-
17	PMCA_REQ-	NC_PMCA_PME-	B4_PAD59	GND
18	VCC	GND	B4_PAD58	GND
19	PMC_VIO	B4_PAD30	B4_PAD57	LPb_DB+
20	B4_PAD31	B4_PAD29	GND	LPb_DD+
21	B4_PAD28	GND	PTID0	LPb_DB-
22	B4_PAD27	B4_PAD26	B4_PAD56	LPb_DD-
23	B4_PAD25	B4_PAD24	B4_PAD55	GND
24	GND	VCC3	B4_PAD54	GND
25	GND	PMCA_IDSEL	B4_PAD53	NC_PMCA25
26	B4_CBE-3	B4_PAD23	GND	NC_PMCA26
27	B4_PAD22	VCC3	GND	NC_PMCA27
28	B4_PAD21	B4_PAD20	B4_PAD52	NC_PMCA28
29	B4_PAD19	B4_PAD18	B4_PAD51	NC_PMCA29
30	VCC	GND	B4_PAD50	NC_PMCA30

Pin#	J21	J22	J23	J24
31	PMC_VIO	B4_PAD16	B4_PAD49	NC_PMCA31
32	B4_PAD17	B4_CBE-2	GND	NC_PMCA32
33	B4_FRAME-	GND	GND	NC_PMCA33
34	GND	NC_PMCA_PMC_RSVD0	B4_PAD48	NC_PMCA34
35	GND	B4_TRDY-	B4_PAD47	NC_PMCA35
36	B4_IRDY-	VCC3	B4_PAD46	NC_PMCA36
37	B4_DEVSEL-	GND	B4_PAD45	NC_PMCA37
38	VCC	B4_STOP-	GND	NC_PMCA38
39	B4_PCIXCAP	B4_PERR-	PTENB-	NC_PMCA39
40	B4_LOCK-	GND	B4_PAD44	NC_PMCA40
41	PMCA_SCL	VCC3	B4_PAD43	NC_PMCA41
42	PMCA_SDA	B4_SERR-	B4_PAD42	NC_PMCA42
43	B4_PAR	B4_CBE-1	B4_PAD41	NC_PMCA43
44	GND	GND	GND	NC_PMCA44
45	PMC_VIO	B4_PAD14	GND	NC_PMCA45
46	B4_PAD15	B4_PAD13	B4_PAD40	NC_PMCA46
47	B4_PAD12	B4_M66EN	B4_PAD39	NC_PMCA47
48	B4_PAD11	B4_PAD10	B4_PAD38	NC_PMCA48
49	B4_PAD9	B4_PAD8	B4_PAD37	NC_PMCA49
50	VCC	VCC3	GND	NC_PMCA50
51	GND	B4_PAD7	GND	NC_PMCA51
52	B4_CBE-0	NC_PMCA_PMC_RSVD1	B4_PAD36	NC_PMCA52
53	B4_PAD6	VCC3	B4_PAD35	NC_PMCA53
54	B4_PAD5	NC_PMCA_PMC_RSVD2	B4_PAD34	NC_PMCA54
55	B4_PAD4	NC_PMCA_PMC_RSVD3	B4_PAD33	NC_PMCA55
56	GND	GND	GND	NC_PMCA56
57	PMC_VIO	NC_PMCA_PMC_RSVD4	PTID1	NC_PMCA57
58	B4_PAD3	NC_PMCA_PMC_RSVD5	B4_PAD32	NC_PMCA58
59	B4_PAD2	GND	NC_PMCA_PCI_RSVD5	NC_PMCA59
60	B4_PAD1	NC_PMCA_PMC_RSVD6	NC_PMCA_PCI_RSVD6	NC_PMCA60
61	B4_PAD0	B4_ACK64-	NC_PMCA_PCI_RSVD7	NC_PMCA61
62	VCC	VCC3	GND	NC_PMCA62
63	GND	GND	GND	NC_PMCA63
64	B4_REQ64-	NC_PMCA_PMC_RSVD7	NC_PMCA_PCI_RSVD8	NC_PMCA64

Section

9 Specifications

This section describes the electrical, environmental, and mechanical specifications of the CPC5505.

9.1 Electrical and Environmental Specifications

The subsequent topics provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

CPC5505 Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the CPC5505 at these maximums. See the "DC Operating Characteristics" topic in this section for operating conditions.

Supply Voltage, Vcc:	5.5 V
Supply Voltage, Vcc3:	4.5 V
Supply Voltage, AUX +:	15 V
Storage Temperature:	-40° to +85° C
Non-Condensing Relative Humidity:	<95% at 40° C
Ethernet Cable length:	Channel A and B: 100 meters

Operating Temperature

Operating temperature is processor dependent. The operating temperature range is 0° C to 50° C. The CPC5505 comes from the factory with an integrated heat sink for cooling the processor. The heat sink requires 250 LFM (linear feet per minute) of airflow. The maximum power dissipation of the CPU is 24.5 W.

Caution: External airflow must be provided at all times during operation to avoid damaging the CPU modules. Performance Technologies strongly recommends use of a fan tray below the card rack to supply the external airflow.

DC Operating Characteristics

Table 17. Power Consumption

Voltage (VDC)	1.80 GHz, 1GB DDR SDRAM	
	Power (W)	
	Typical	Max
5.00 V, +5%, -3%	10	14.1
3.30 V, +5%, -3%	18	29.8

NOTES: 5V and 3.3V maximum power requirements do not occur simultaneously.
Maximum total power consumption is 38.7W (while running CPU stress program).

Battery Backup Characteristics

Battery Voltage:	3 V
Battery Capacity:	220 mAh
Real-Time Clock Requirements:	5 µA max. (Vbat = 3 V, Vcc= 0 V)
Real-Time Clock Data Retention:	44,000 hrs/ 5.0 yrs min. (not powered), 7.5 yrs min. (with Vcc power applied 8 hrs/day)
Electrochemical Construction:	Manganese dioxide (CR series) Lithium battery

Caution: The CPC5505 contains a lithium battery. This battery is not a field-replaceable unit. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions. Return the CPC5505 to Performance Technologies for battery service.

9.2 CPC5505 Reliability

Board MTBF = TBD

MTTR: 3 min.

9.3 Mechanical Specifications

This section includes the following mechanical specifications for the CPC5505:

- Board dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)

Board Dimensions and Weight

The CPC5505 meets the *CompactPCI Specification, PICMG 2.0, Version 2.1* for all mechanical parameters.

Mechanical dimensions are shown in the “CPC5505 Board Dimensions” illustration and are outlined below.

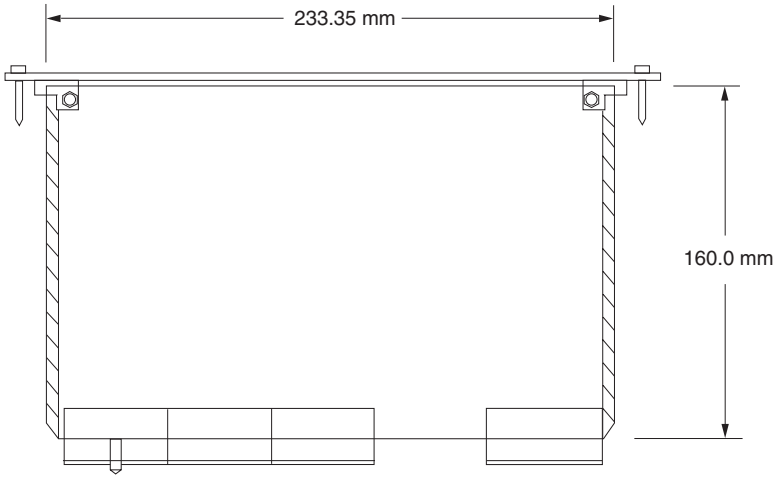
Board Length: 160 mm (6.24 in)

Board Width: 233.35 mm (9.1 in)

Board Height: 16.81 mm (0.622 in) typ., measuring from the tallest secondary side component to the tallest primary side component

Board Weight: with 1.8 GHz processor and hard disk: .65 kg (1.4 pounds)

Figure 18. CPC5505 Board Dimensions



CPC5505 Connectors

The CPC5505 includes several connectors to interface with application-specific devices. Connector location drawings, detailed descriptions and pinouts for these connectors are given in the “Connectors” section.

Section

10 System Registers

Several system registers control and monitor a variety of functions on the CPC5505. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Take care when modifying the contents of these registers: the system BIOS may be relying on the state of the bits under their control.

10.1 System Register Definitions

The system registers are accessible as follows:

I/O Address	Register Name	Default Value	Access	Size
78h	Flash Control	0x00	R/W	8 bits
79h	Watchdog	0x00	R/W	8 bits
80h	BIOS POST Codes	0x00	R/W	8 bits
E1h	ENUM, WD NMI Status, Ethernet Routing	0x00	R/W	8 bits
E2h	Board ID	0x00	RO	8 bits
E3h	Switch Monitors	0x80	RO	8 bits
E5h	Video/LED Control	0x00	R/W	8 bits
E6h	HCINDEX - Host Control Index	0x00	R/W	8 bits
E7h	HCDATA - Host Control Function Data	0x00	R/W	8 bits
E8h	INT- Interrupt Status and Mask Register	0x22	R/W	8 bits

Flash Control (78h)

I/O Address: 78h
Default Value: 0x00
Size: 8 bits
Attribute: R/W

NOTE: This register is reset to 00h on init or reset. The BIOS resides in page 000.

Bit	Description
7	**Flash Write Enable** 0=Write Protect 1=Write Enable
6	**BIOS Recovery Module Override Bit** This bit supersedes the Boot Source switch (SW3-2). If this bit is set to 1, then the Boot Source switch has no affect on the boot device, and the CPC5505 boots from onboard flash. See Section 6, "BIOS Recovery," for more information. 0=SW3-2 selects boot source 1= boot from onboard flash
5	**Reserved** This bit is reserved and always reads as 0. Write 0 to this bit.
4	**Reserved** This bit is reserved and always reads as 0. Write 0 to this bit.
3	**Reserved** This bit is reserved and always reads as 0. Write 0 to this bit.
2	**Page 2** Flash A24 (4 MB page)
1	**Page 1** Flash A23 (4 MB page)
0	**Page 0** Flash A22 (4MB page)

Watchdog (79h)

I/O Address: 79h
Default Value: 0x00
Size: 8 bits
Attribute: R/W

Bit	Description
7	**Stage 2 Monitor (Reset Monitor)** Monitors the second stage (Reset) timer status. Read Value: 0= Watchdog has not timed out since power up or since this bit was last set to 0 1= Watchdog reset timeout has occurred since power up or since this bit was last set to 0 Write Value: 0= Sets this bit to 0 1= No effect Power-Up Value: 0 This bit is not changed by a reset.
6	**Stage 1 Monitor (NMI Monitor)** Monitors the first stage (NMI) timer status. Read Value: 0= Watchdog has not timed out since power up or since this bit was last set to 0 1= Watchdog timed out and NMI output was asserted Write Value: 0= Sets this bit to 0 1= No effect Power-Up Value: 0 This bit is not changed by a reset.

Bit	Description
5	**Stage 2 Enable** Enables second stage (Reset) activation on timeout. Read Value: 0= Reset activation on timeout disabled (default) 1= Reset activation on timeout enabled Write Value: 0= Reset operation of the watchdog is not enabled. When the watchdog times out, the Stage 2 Monitor bit is not set to 1 and the Reset output is not asserted 1= Reset operation of the watchdog is enabled. When and if the watchdog times out: • The Reset output asserts • The Stage 2 Monitor bit is set to 1 and stays high until set to 0 by software • Reset action occurs approximately 250 ms after NMI Power-Up Value: 0 Value After Timeout: 0 (doesn't re-arm) A hard reset sets this bit to 0.
4	**Stage 1 Enable** Enables NMI activation on timeout. Read Value: 0= Disabled (default) 1= Enable NMI activation on timeout Write Value: 0= Disable NMI operation of the watchdog. When the watchdog times out, the Stage 1 Monitor bit is not set to 1 and the NMI output is not asserted 1= Enable NMI operation of the watchdog. When and if the watchdog times out: • The Stage 1 output (NMI) occurs after the period of time specified by the Terminal Count bits • The Stage 1 Monitor bit is set to 1 and stays high until set to 0 by software • The Stage 2 Reset occurs approximately 250 ms after Stage 1 output, allowing the system software to take action before the reset occurs Power-Up Value: 0 Post Time-Out Value: 0 A hard reset sets this bit to 0.
3	**Reserved** This bit is reserved and always reads as 0. Write 0 to this bit.

Bit	Description
2:0	**Terminal Count (TermCnt2…TermCnt0)** Read Value: Reflects the value written to bits 2 through 0 Write Value: These bits determine the terminal count of the watchdog The minimum timeout period is given. The watchdog times out in no less than the minimum value. The nominal timeout period is 30% longer than the minimum: 000 = 250 ms 100 = 32 s 001 = 500 ms 101 = 64 s 010 = 1 s 110 = 128 s 011 = 8 s 111 = 256 s Power-Up Value: 000 A hard reset sets this bit to 000.

BIOS POST Codes (80h)

I/O Address:	80h
Default Value:	0x00
Size:	8 bits
Attribute:	R/W

Bit	Description
7:0	**D7-D0** These are Port 80 bits that report the BIOS POST (diagnostic) codes. These bits correspond to eight green LEDs (labeled D0 through D7) on the bottom side of the PCB. These LEDs may not be visible if a hot-swap shield is installed on the bottom side on the PCB. BIOS POST errors are also logged into the IPMI System Event Log (SEL) as unique codes. POST errors can be identified by viewing these codes. SEL entries can be viewed in the BIOS setup utility by selecting the *Advanced* | *IPMI 1.5 Configuration* | *View BMC System Event Log* menu item. The BIOS POST error codes are logged as the first byte of the three-byte *Event Data* displayed in IPMI SEL entries with Event Sensor Types: • 0F (POST Error) • 06 (Platform Security) The Error codes and their meanings are listed in the System Event Log BIOS POST Error Codes table below.

Table 18. System Event Log BIOS POST Error Codes

Error Code	POST Error
00	Timer Error
03	CMOS Battery Low
04	CMOS Settings Wrong
05	CMOS Checksum Bad
08	Unlock Keyboard
09	PS2 Keyboard not found
0A	KBC BAT Test failed
0B	CMOS Memory Size Wrong
0C	RAM R/W test failed
0E	A: Drive Error
0F	B: Drive Error
10	Floppy Controller Failure
12	CMOS Date/Time Not Set
40	Refresh timer test failed
41	Display memory test failed
42	CMOS Display Type Wrong
43	~<INS> Pressed
44	DMA Controller Error
45	DMA-1 Error
46	DMA-2 Error
47	POST Memory Manager Allocation Error
48	Password check failed
49	Segment Register Error
4A	Error in ADM initialization
4B	Language Module Error
4C	Keyboard/Interface Error
4D	Primary Master Hard Disk Error
4E	Primary Slave Hard Disk Error
4F	Secondary Master Hard Disk Error
50	Secondary Slave Hard Disk Error
55	Primary Master Drive - ATAPI Incompatible
56	Primary Slave Drive - ATAPI Incompatible
57	Secondary Master Drive - ATAPI Incompatible
58	Secondary Slave Drive - ATAPI Incompatible
5D	S.M.A.R.T. Command Failed
5E	Password check failed

ENUM, WD NMI Status, ENET Routing (E1h)

I/O Address: 0xE1h

Default Value: 0x00

Size: 8 bits

Attribute: R/W

Bit	Description
7	**WD NMI Status (Read Only)**
6	**ENUM**- This bit reports that a hot swappable peripheral card has been installed or removed from the system: 0 = ENUM- is not asserted on the backplane 1 = ENUM- is asserted on the backplane.
5	**RTM NMI Status**
4	**Reserved** This bit is reserved and should not be modified by the user.
3	**Ethernet A Backplane/PTMC Select.** 0 = Backplane (default) 1 = PTMC
2	**Ethernet A Front/Rear Select** 0 = Front (default) 1 = Rear
1	**Ethernet B Backplane/PTMC Select** 0 = Backplane (default) 1 = PTMC
0	**Ethernet B Front/Rear Select** 0 = Front (default) 1 = Rear

Board ID (E2h)

Address Offset: E2h
Default Value: 0x00
Size: 8 bits
Attribute: RO

Bit	Description
7:4	**Reserved** These bits are reserved and should not be modified by the user.
3:0	**Board Revision** This port is used to read the status of cuttable traces CT17, CT18, CT19, CT20 to determine the current board revision (Revision 0 = Fh). Do not change these cuttable traces since these values may be used by the system BIOS. These bits should be written as logical 0s when this register is modified.

Switch Monitors (E3h)

Address Offset: E3h
Default Value: 0x80
Size: 8 bits
Attribute: RO

Bit	Description
7	**Flash Write-Protect Status** This bit corresponds to the status of Flash Write Protect/Write Enable switch SW3-1: 0 = Flash is write-protected by SW3-1 1 = Flash is *not* write-protected by SW3-1
6	**Boot Source Monitor** This bit allows software to monitor the boot source as selected by SW3-2: 0 = SW3-2 is closed (boot from BIOS Recovery socket U42) 1 = SW3-2 is open (boot from the BIOS contained in on-board flash)
5:4	**Reserved** These bits are reserved and should not be modified by the user.
3:0	**Software Configuration** These bits are used to provide configuration information to the user's software by monitoring the status of the Software Configuration switch SW4: 0 = Open switch 1 = Closed switch The bits correspond to switch segments as follows: **SW4-2** = Bit 1, **SW4-3** = Bit 2; **SW4-4** = Bit 3

Video/LED Control (E5h)

Address Offset: E5h
Default Value: 0x00
Size: 8 bits
Attribute: R/W

Bit	Description
7	**Video Select Front/Rear.** This bit toggles video connection between the faceplate and the rear panel. This bit can be set in the BIOS setup screen. 0 = video routed to the faceplate connector J11 1 = video routed to the rear-panel connector J5 **Note:** DIP switch SW2-3 can override this function and send video to the faceplate.
6:4	**Reserved** These bits are reserved and should not be modified by the user.
3:2	**User LED 1** These bits set the status of User LED 1. Bit 3 affects the green LED as follows: 0=off 1=on Bit 2 affects the amber LED as follows: 0=off 1=on
1:0	**User LED 2** These bits set the status of User LED 2. Bit 1 affects the green LED as follows: 0=off 1=on Bit 0 affects the amber LED as follows: 0=off 1=on

HCINDEX - Host Control Index (E6h)

I/O Address: E6h
Reset: PCIRST
Default Value: 0x00
Size: 8 bits
Attribute: R/W

Bit	Description
7:2	**Reserved** Reserved for future use.
1:0	**Host Control Index** This register provides the address offset for the HCDATA registers. This is the number listed in the HCINDEX Offset column in the Host Control Function Register table.

HCDATA - Host Control Function Data (E7h)

I/O Address: E7h
Reset: PCIRST
Default Value: NA
Size: 8 bits
Attribute: R/W

Bit	Description
7:0	This register provides access to the Host Control Function Registers. The particular register accessed is determined by the offset value in the HCINDEX register.

INT- Interrupt Status and Mask Register (E8h)

I/O Address: E8h
Reset: PCIRST
Default Value: 22h
Size: 8 bits
Attribute: R/W

Bit	Description
7:6	**Reserved**
5	**ENUM Interrupt Mask** 0 = external interrupt issued when a backplane device asserts ENUM 1 = external interrupt not issued when a backplane device asserts ENUM
4	**ENUM Interrupt Flag (RO)** 0 = no interrupt has been issued because of ENUM being asserted by a backplane device 1 = an interrupt has been issued because of ENUM being asserted by a backplane device. Clear at the source device.
3:2	**Reserved**
1	**Reserved** This bit always reads back as 1. Writes have no effect.
0	**Reserved** This bit always reads back as 0. Writes have no effect.

Section
11 Reset

This section discusses the various reset types and reset sources on the CPC5505. Because many embedded systems have different requirements for board reset functions, the incorporation of this sub-system on the CPC5505 has been designed to provide maximum flexibility.

11.1 Reset Types and Sources

The CPC5505's three reset types are listed below. The sources for each reset type are detailed in the following topics.

- **Backend Power Down:** The backend logic is powered off. All on-board devices are reset. If the CPC5505 is acting as a system master PCIRST# is driven on the system backplane.
- **General Reset:** All on-board devices are reset and PCIRST# is driven on the system backplane.
- **NMI:** Non-maskable interrupt. Though not a reset in the strict sense, an NMI can have the same effect as other resets.

Backend Power Down Sources

Board Extraction

When a board is extracted from an enclosure (specifically, when the short, board select pin is disengaged), the hot swap controller unconditionally removes backend power from the board and holds the CPC5505 in reset.

Low Voltage

When the 3.3 V, 5 V, and 12 V supply voltages are detected as being below an acceptable operating limit, the Hot Swap controller unconditionally removes backend power and holds the CPC5505 in reset.

Overcurrent Fault

If a power fault condition (overcurrent) is detected, the Hot Swap controller removes backend power and lights the amber Power/Reset LED indicator. The CPC5505 is held in reset.

General Reset Sources

Push-Button Reset

When the System Reset button (SW1) on the faceplate is pressed, the CPC5505 resets itself and drives PCIRST on the CompactPCI bus. Sources for push-button reset include:

- Faceplate push-button reset switch (SW1)
- Programmable watchdog timer. The watchdog timer is discussed in Section 5.
- CompactPCI bus push-button reset signal, PRST# (J2-C17)
- PBRST- generated by an optional RPIO transition board, for example by pressing the ZT 4807*e* Rear Transition Module's push button-switch SW2.

NMI Sources

The Watchdog Timer (Port 79h)

The watchdog timer can be programmed through the watchdog register (Port 79h, bit 4) to generate a non-maskable interrupt if it is not strobed within a given time-out period. The watchdog timer is discussed in Section 5.

Rear Transition Module NMI Push Button

An NMI push button may be available on an optional Rear Transition Module (such as SW3 on the ZT 4807*e* Rear Transition Module). Pressing this button causes the CPC5505 to generate a non-maskable interrupt.

Section

12 Thermal Considerations

This section describes the thermal requirements to reliably operate a CPC5505 processor board with Pentium M Processor installed.

12.1 Thermal Requirements

The maximum processor core temperature allowed by the Pentium M Processor on the CPC5505 is 100° C.

Caution: To avoid damaging the CPU, *do not exceed the maximum processor core temperature!*

The CPC5505 comes from the factory with integrated heat sinks to help dissipate the heat generated by the processor. The maximum ambient air temperature required by the heat sink to maintain core temperature below the maximum is 50° C. The maximum ambient air temperature assumes an airflow of 250 linear feet per minute past the heat sink.

Caution: External airflow must be provided at all times during operation to avoid damaging the CPU. Performance Technologies strongly recommends use of a fan tray below the card rack to supply the external airflow.

12.2 Temperature Monitoring

Because reliable long-term operation of the CPC5505 depends on maintaining proper temperature, Performance Technologies strongly recommends that you verify the operating temperature of the processor (core) in your final system configuration.

The Pentium M Processor incorporates an on-die thermal diode that can be used to monitor the processor's die temperature. The CPC5505 includes an ADM1026 device that is monitored through the BMC. This device checks the die temperature of the processor for thermal management purposes.

Section

13 Agency Approvals

This section presents agency approval and certification information for the CPC5505 Processor Board.

13.1 UL 60950 Certification

Underwriters Laboratories, Inc.®

Safety: UL Safety of Information Technology Equipment, including Electrical Business Equipment IEC 60950 and UL 60950 (UL file # E179737)

13.2 CE Certification

The CPC5505 meets the intent of *Directive 89/336/EEC* for electromagnetic compatibility and the *Low-Voltage Directive 73/23/EEC* for product safety. Compliance was demonstrated to the following specifications as listed in the *Official Journal of the European Communities*:

EN 50081-1 Emissions:

FCC 15B, Class A	AC Line Conducted Emissions Test
EN55022, Class A	Radiated Radio Frequency (RF) Emissions Tests
EN55022, (1998)	Telecommunications Port Conducted Emissions Test
EN 61000-3-2 (1995)	Power Line Harmonics Test
EN61000-3-3 (1995)	Power Line Fluctuation/Flicker Test

EN 55024: 1998 Immunity:

IEC 61000 4-2 (1995)	Electrostatic Discharge
IEC 61000 4-3 (1995)	RF Radiated Fields
IEC 61000 4-4 (1995)	Electrical Fast Transients/Burst
IEC 61000 4-6 (1996)	RF Common Mode

BELLCORE GR-1089-CORE:

Sect. 2	Electrostatic Discharge
Sect. 3.2.2	Radiated RF Emissions
Sect. 3.2.3	AC Line Conducted Emissions
Sect. 3.3.1	RF Radiated Fields
Sect. 3.3.3	RF Common Mode

Low Voltage Directive 73/23/EEC:

UL 60950/EN 60950	Safety of Information Technology Equipment, Including Electrical Business Equipment

13.3 FCC Regulatory Information

Regulatory information: Federal Communications Commission (FCC) (USA only). FCC Class A certification is pending.

Caution: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to FCC 47 CFR Part 15, Subpart B, Class A of the FCC Rules. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Performance Technologies system RFI and Radiated Immunity tests were conducted with a specific configuration representing an anticipated general application. Changes or modifications to peripheral devices and shielded cables not expressly approved by Performance Technologies could result in EMI interference.

FCC compliance was achieved under the following conditions:

- Shielded signal cables and a shielded power cord
- Shielded cables on all I/O ports
- Cable shields connected to earth ground via metal shell connectors
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground
- Faceplate screws properly tightened

For minimum RF emissions, it is essential that the conditions above are implemented; failure to do so could compromise the FCC compliance of the equipment containing the system.

Section
14

Data Sheet and Device Driver Reference

This section provides links to data sheets, standards, and specifications for the technology designed into the CPC5505.

14.1 Chipset

The CPC5505 incorporates the Intel 855GME Graphics Memory Controller Hub (GMCH-M) as the North Bridge and the Intel 6300ESB I/O Controller Hub (ICH) as the South Bridge Chip.

More information on the Intel 855GME GMCH-M and 6300ESB ICH may be found on Intel's Web site at:
http://www.intel.com/design/chipsets/embedded/docs/855gme.htm

The latest graphics drivers may be downloaded from the following Web site:

http://downloadfinder.intel.com/scripts-df/Product_Filter.asp?ProductID=922

The latest 6300ESB ICH drivers may be downloaded from the following Web site:

http://downloadfinder.intel.com/scripts-df/Product_Filter.asp?ProductID=1706

14.2 CompactPCI

The CPC5505 is compliant with the following CompactPCI specifications:

- *CompactPCI Specification, PICMG 2.0, R 2.1*
- *CompactPCI Hot Swap Specification, PICMG 2.1, R 2.0*
- *PMC Specification IEEE P1386.1*
- *CompactPCI System Management Specification, PICMG 2.9, R 1.0*
- *PCI Telecom Mezzanine/Carrier Card Specification, PICMG 2.15 R1.0*
- *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, R 1.0*

These specifications can be purchased from PICMG (PCI Industrial Computers Manufacturers Group). A short form specification in Adobe Acrobat format (PDF) is also available on PICMG's web site at:

https://www.picmg.org

14.3 Ethernet

Gigabit Ethernet is implemented on the CPC5505 via the Intel 82546EB Gigabit Ethernet PCI Controller. Refer to the *Intel 82546EB Dual Port Gigabit Ethernet Controller* data sheet for more information. The data sheet is in HTML format and available online at:

http://www.intel.com/design/network/products/lan/controllers/82546.htm

The latest 82546EB drivers may be downloaded from the following Web site:

http://downloadfinder.intel.com/scripts-df/Product_Filter.asp?ProductID=991

14.4 Intelligent Platform Management Interface (IPMI)

See the Intel IPMI home page for information concerning the Intelligent Platform Management Interface, including the *Intelligent Platform Management Interface v1.5 Specification* and the *Intelligent Platform Management Interface Implementer's Guide*:

http://developer.intel.com/design/servers/ipmi/spec.htm

14.5 Pentium M Processor

For more information about the Low Power Intel Pentium M Processor, see the Intel Web site at:

http://developer.intel.com/products/notebook/processors/pentiumm/index.htm

14.6 I/O Controller

The following CPC5505 functions reside on the National Semiconductor PC87417 I/O controller:

- Serial port controller
- Floppy disk controller
- Keyboard and mouse controller
- Real-time clock and CMOS memory
- Access Bus Interface to the BIOS
- Intelligent power management

National Semiconductor's Advanced PC division has been purchased by Winbond Electronics Corp. Contact Winbond Electronics Corp. for more information on the PC87417 I/O controller:

http://www.winbond.com

14.7 User Documentation

The latest IPnexus product information and manuals are available on the Performance Technologies Web site. BIOS and driver updates are also available from this site:

http://www.pt.com

Information specific to the CPC5505 is available at this URL:

http://www.pt.com/products/prod_CPC5505.html

Section
15

In Case of Difficulty

If you encounter difficulty in using this Performance Technologies product, you can contact our support personnel in several ways. Please have the product model and serial number handy before contacting Product Support.

Internet

www.pt.com

Email

support@pt.com

Describe your problem in detail. Please include your return email address and telephone number.

FAX

(805) 541-5088

Mark your FAX “Attention: Product Support.” Describe your problem in detail. Please include your return FAX number and telephone number.

Telephone

(805) 541-0488

Request Product Support. Our offices are open between 8:00 am and 5:00 pm Pacific Time, Monday through Friday.

If you are located outside North America, we encourage you to contact the local Performance Technologies distributor or agent for support. Many of our distributors or agents maintain technical support staffs.

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