MOSIS Scalable CMOS Design Rules

(revision 7)

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1 Introduction

1.1 SCMOS Design Rules

This document defines the official layout design rules for MOSIS scalable CMOS (SCMOS) design technology. It supercedes all previous revisions.

In SCMOS technology, circuit geometries are drawn according to Mead and Conway's λ-based methodology [3]. The unit of measurement, λ, can easily be scaled to different fabrication processes as semiconductor technology advances.

A user design submitted to MOSIS in SCMOS technology should be in either Calma GDSII format [1] or Caltech Intermediate Form (CIF version 2.0) [3]. Each design has a technology *designation* that goes with it for the purpose of MOSIS's data prep. At the moment, three designations are used to specify CMOS processes. Each designation may have one or more *options* associated for the purpose of either (1) special features for the target process or (2) the presence of novel device in the design. At the time of writing, MOSIS is offering six CMOS processes from three different foundries with drawn feature sizes ranging from 2.0 μm down to 0.6 μm.

A list of the things that have either been revised or added since our last release can be found in Appendix A. Please refer to the specific sections for detailed descriptions.

2 Standard SCMOS

The standard CMOS technology accessed by MOSIS is a single polysilicon, double metal, bulk CMOS process with enhancement-mode n-MOSFET and p-MOSFET devices [4].

2.1 Well Flavor

Three types of *designation* are used to indicate the flavor of the well (substrate) used for fabrication as shown in Table 1.

Designation	Description
SCN	Scalable CMOS N-well
SCP	Scalable CMOS P-well
SCE	Scalable CMOS Either-well

Table 1: SCMOS well flavor designations

The SCN and SCP designations with a submitted project are designed for fabrication of the specified well only. For convenience, in both cases, a project may include the 'other' well, but it will always be ignored. SCE projects are used for fabrication in any CMOS process, N-well or P-well (*either*). A project with SCE designation must include *both* wells (and correspondingly, well/substrate contacts for proper bias). For any given fabrication process, the 'other' well will be ignored during the mask generation. If twin-tub processes are offered in the future, both wells will be used.

2.2 SCMOS Options

SCMOS options are used to designate projects which use additional layers beyond the standard CMOS technology. Each option is named by a designator that is tacked onto the basic designator for its well flavor. Reader should note that not all possible combinations (with well flavor) are actually available. The currently available SCMOS options are listed in Table 2.

In addition to the options in Table 2, two undeclared options also exist. One with respect to the existence of *high voltage* MOSFET devices; the other, a *tight metal* rule for high-density metal interconnections. For options available to specific process, please refer to Table 3 for the current MOSIS offerings.

2.3 SCMOS Offerings

MOSIS is currently offering the fabrication processes as shown in Table 3. For each process, the list of appropriate SCMOS technology designations is listed. Note that whenever SCNxx appears in the table, SCExx is also appropriate. Likewise, whenever SCPxx appears, SCExx is also appropriate.

[2]CCD layer not included.

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Designation	Long form	Description
E	Electrode	Adds a second polysilicon layer (**electrode**) that can serve as either one of electrode of a poly capacitor or as a gate for transistors. A contact layer (**electrode_contact**) to metal also exists.
A	Analog	Adds electrode layer (as in E option) plus a **pbase** layer for the construction of vertical NPN transistor. A **buried_ccd** layer is also present. for buried-channel CCD applications
3M	Triple Metal	Adds second via (**via2**) and third metal (**metal3**) layers.
LC	Linear Capacitor	Adds a **cap_well** layer for the implementation of linear capacitors.
_MEMS	Micromechanical Systems	Adds two new layers, **mems_open** and **mems_etch_stop** for the purpose of micro-mechanical device construction.

Table 2: SCMOS technology options

Foundry	Process	Lambda	Options
Orbit	2.0 μm N-well	1.0 μm	SCNA, SCNE, SCN, SCNA_MEMS
Orbit	2.0 μm P-well	1.0 μm	SCPE, SCP, SCPE_MEMS
AMI	1.5 μm N-well	0.8 μm	SCNA[1], SCNE, SCN, High Voltage
Orbit	1.2 μm N-well	0.6 μm	SCNA[2]
HP	AMOSI/CMOS34	0.6 μm	SCNLC, SCN, Tight Metal
HP	CMOS26B/G	0.5 μm	SCN3M, SCN, Tight Metal

Table 3: MOSIS SCMOS technology offerings

3 CIF and GDS Layer Specification

Design geometries (or mask features) can be represented either in GDS-II or Caltech Intermediate Form (CIF Version 2.0). While the former is coded in binary format, the latter is a plain text file and can be easily interpreted. For detailed syntax and semantic specifications of Calma/GDS-II or CIF, please refer to [1] and [3] respectively.

In GDS II format, a mask layer is specified by a layer number between 0 and 63. MOSIS now reserves layers numberd from 21 to 62 for mask specification and future extension. Layers defined out of this range can be used by customers for their own purpose. MOSIS will ignore all geometry information on these layers (0 to 20 and 63) and map it to the CIF comment layer (CX) if necessary. In this revision, 6 new layers are added starting from layer number 21.

- CVP (layer 21) is used to indicate high-voltage p-type area. More comprehensive information can be found in [2].
- CVN (layer 22) is used to indicate high-voltage p-type area.
- COP (layer 23) is used to indicate substrate pit opening area for MEMS devices.
- CPS (layer 24) is used to indicate substrate p^+ etching-stop area for MEMS devices.
- CCC (layer 25) is used for generic contact.
- XP (layer 26) is used to indicated pad location.

Users should be aware that there exist only *one* type of physical contact (i.e. between first metal and poly or active), though several have been defined for historical reason and are retained for backward compatibility. A complete list of SCMOS layers can be found in Table 4 on next page.

4 Sub-micron Rules

The SCMOS design rules have been historically designed for 1.0 - 3.0 micron CMOS technology. To take full advantage of advanced submicron process technology, a set of rules have been selected to be modified to fit our foundry's rules.

Table 5 lists those rules in MOSIS's HP CMOS26G process that are different between SCN3M and SCN3M_26G technology specification with λ equals to 0.5 and 0.4 μm respectively.

SCMOS layer	CIF name	GDS II number	GDS II type
P_HIGH_VOLTAGE	CVP	21	-
N_HIGH_VOLTAGE	CVN	22	-
MEMS_OPEN	COP	23	-
MEMS_ETCH_STOP	CPS	24	-
PADS	XP	26	-
P_WELL	CWP	41	-
N_WELL	CWN	42	-
ACTIVE	CAA	43	-
P_PLUS_SELECT	CSP	44	-
N_PLUS_SELECT	CSN	45	-
POLY	CPG	46	-
CONTACT	CCC, CCP, CCA, CCE	25, 47, 48, 55	-
METAL1	CMF	49	-
VIA	CVA	50	-
METAL2	CMS	51	-
GLASS	COG	52	-
ELECTRODE	CEL	56	-
BURIED_CCD	CCD	57	-
PBASE	CBA	58	-
CAP_WELL	CWC	59	-
VIA2	CVS	61	-
METAL3	CMT	62	-
COMMENT	CX	0 - 20, 63	-

Table 4: SCMOS technology CIF and GDS layers

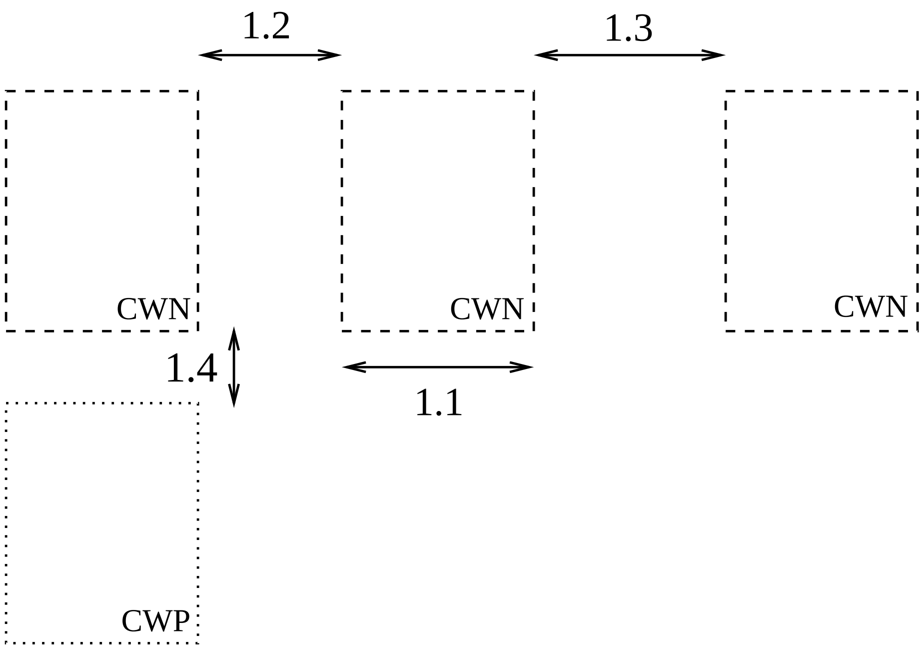
Description	Rule	SCMOS $\lambda = 0.5\mu$m	SCMOS (Tight Metal) $\lambda = 0.5\mu$m	SCMOS_26G $\lambda = 0.4\mu$m
WELL_W	1.1	10	10	12
WELL_S_DIFF	1.2	9	9	18
WELL_O_ACT_XTOR	2.3	5	5	6
WELL_S_ACT_XTOR	2.3	5	5	6
POLY_S	3.2	2	2	3
CON_S	5B.3,6B.3	2	2	3
M1_W	7.1	3	3	3
M1_S	7.2	3	2	3
M2_W	9.1	3	3	3
M2_S	9.2	4	3	3
M3_W	15.1	6	6	5
M3_S	15.2	4	4	3

Table 5: SCMOS options for CMOS26G

5 SCMOS Design Rules

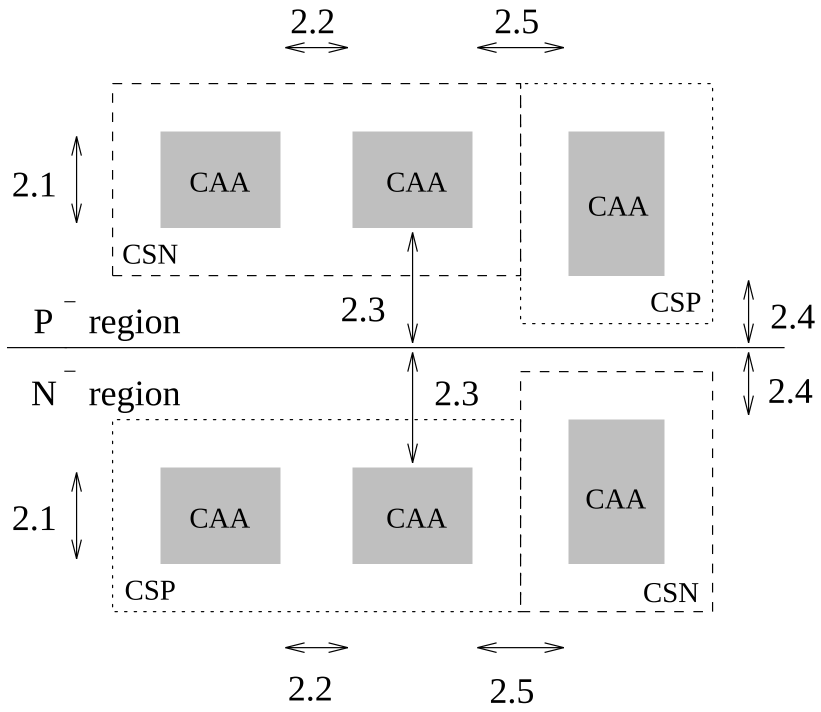
Well (CWN, CWP)

1.1	Minimum width	10
1.2	Minimum spacing between wells at different potential	9
1.3	Minimum spacing between wells at same potential	0 or 6
1.4	Minimum spacing between wells of different type (if both are drawn)	0



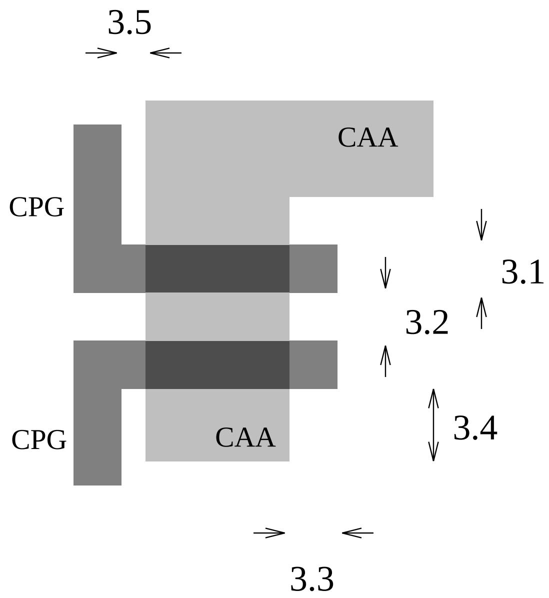
Active (CAA)

2.1	Minimum width	3
2.2	Minimum spacing	3
2.3	Source/drain active to well edge	5
2.4	Substrate/well contact active to well edge	3
2.5	Minimum spacing between active of different implant	0 or 4



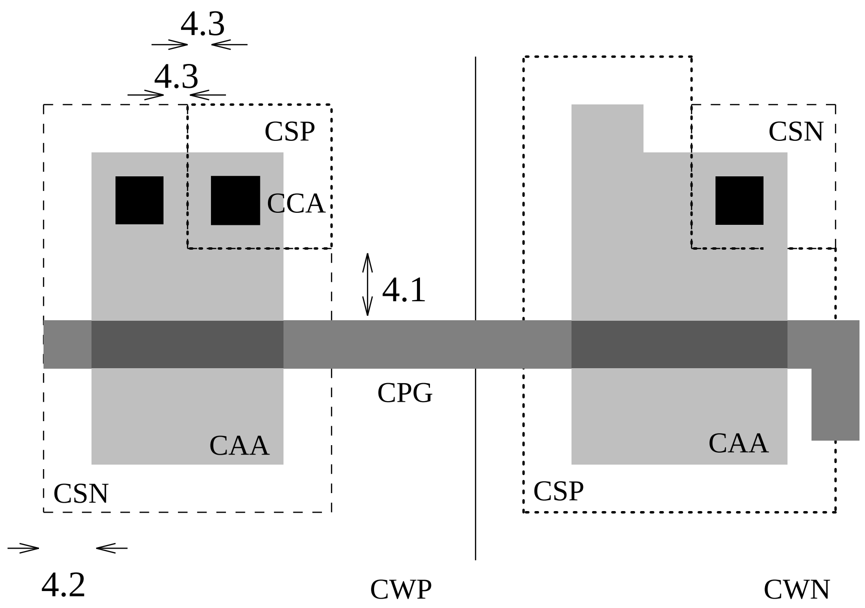
Poly (CPG)

3.1	Minimum width	2
3.2	Minimum spacing	2
3.3	Minimum gate extension of active	2
3.4	Minimum active extension of ploy	3
3.5	Minimum field poly to active	1



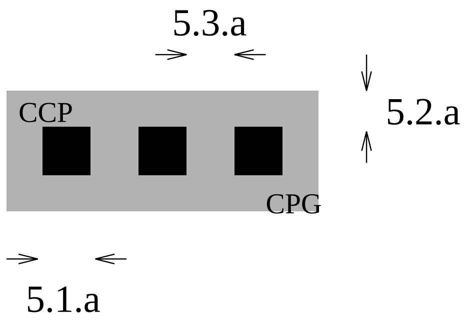
Select (CSN, CSP)

4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3
4.2	Minimum select overlap of active	2
4.3	Minimum select overlap of contact	1
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap)	2



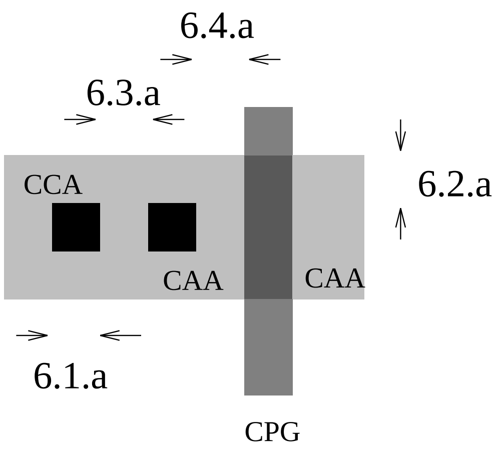
Simple Contact to Poly (CCP)

5.1.a	Exact contact size	2×2
5.2.a	Minimum poly overlap	1.5
5.3.a	Minimum contact spacing	2



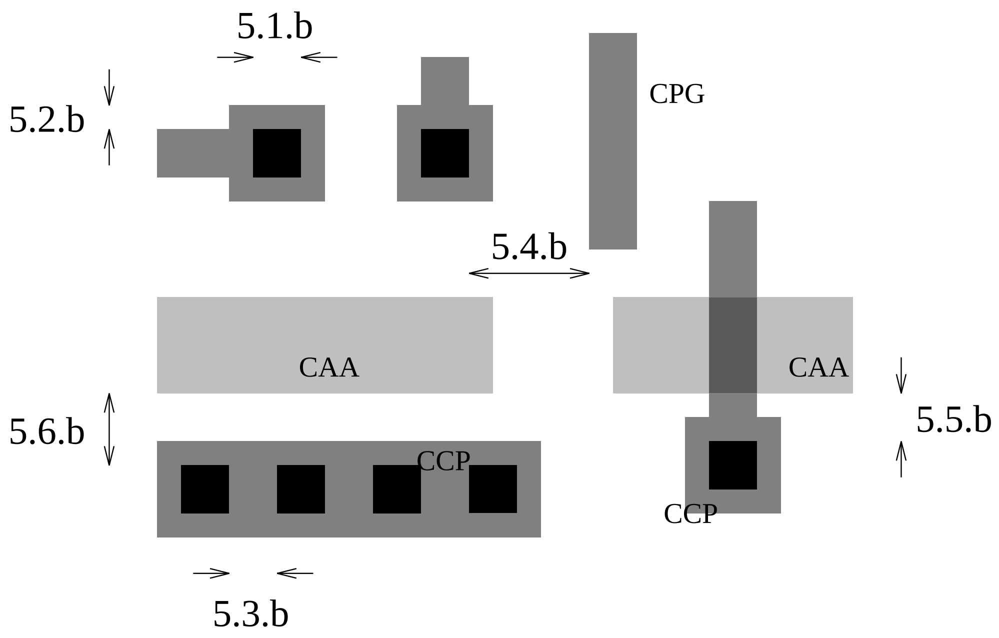
Simple Contact to Active (CCA)

6.1.a	Exact contact size	2×2
6.2.a	Minimum active overlap	1.5
6.3.a	Minimum contact spacing	2
6.4.a	Minimum spacing to gate of transistor	2



Alternative[3] Contact to Poly (CCP)

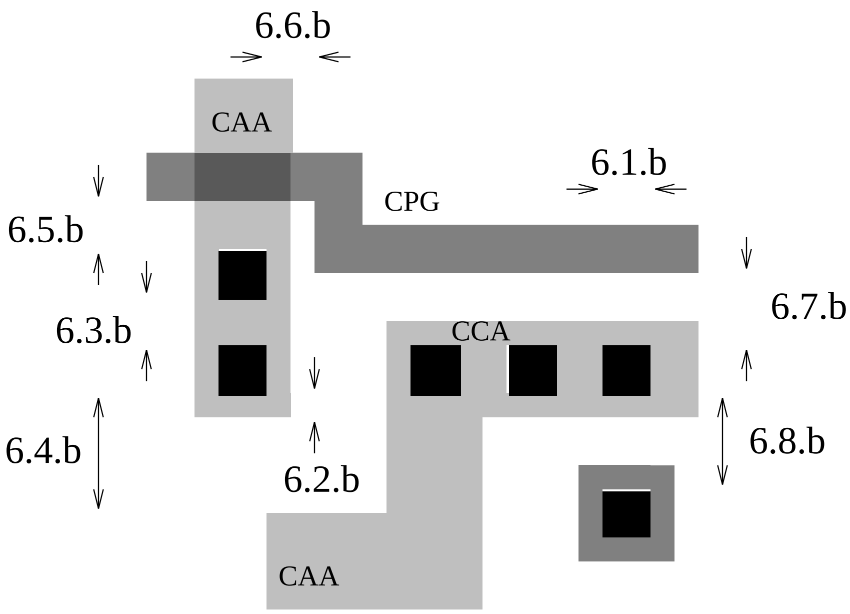
5.1.b	Exact contact size	2×2
5.2.b	Minimum poly overlap	1
5.3.b	Minimum contact spacing	2
5.4.b	Minimum spacing to other poly	4
5.5.b	Minimum spacing to active (one contact)	2
5.6.b	Minimum spacing to active (many contacts)	3



[3]If you have difficulties with half lambda rule.

Alternative[4] Contact to Active (CCA)

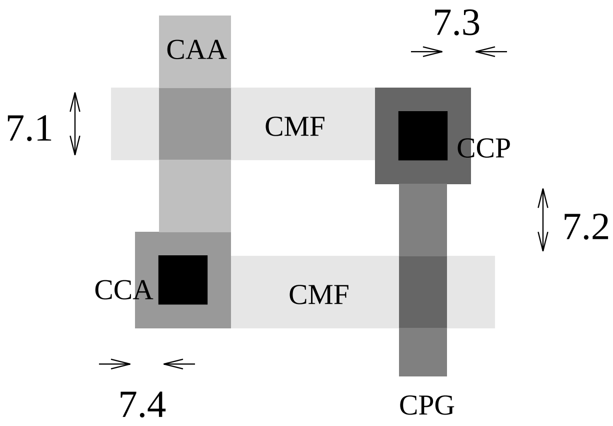
6.1.b	Exact contact size	2×2
6.2.b	Minimum active overlap	1
6.3.b	Minimum contact spacing	2
6.4.b	Minimum spacing to diffusion active	5
6.5.b	Minimum spacing to gate of transistor	2
6.6.b	Minimum sapcing to field poly (one contact)	2
6.7.b	Minimum spacing to field poly (many contacts)	3
6.8.b	Minimum spacing to poly contact	4



[4] If you have difficulties with half lambda rule.

Metal1 (CMF)

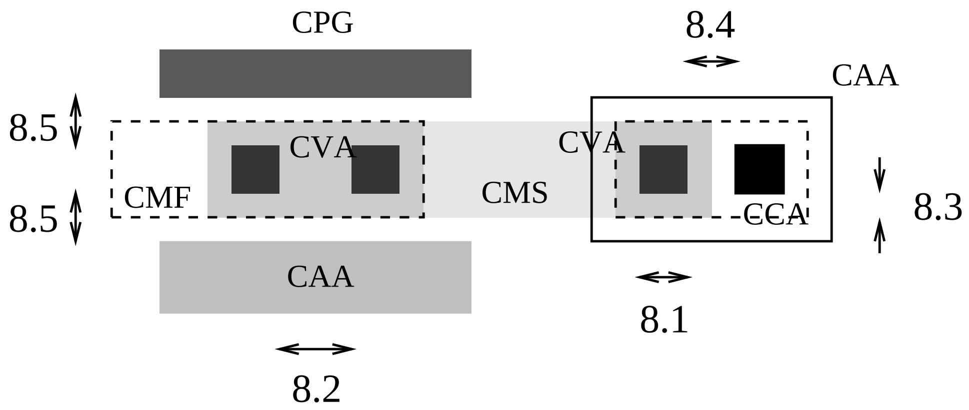
7.1	Minimum width	3
7.2.a	Minimum spacing	3
7.2.b[5]	Minimum tight metal spacing	2
7.3	Minimum overlap of poly contact	1
7.4	Minimum overlap of active contact	1



[5] Only allowed between minimum width wires, otherwise use regular spacing rule.

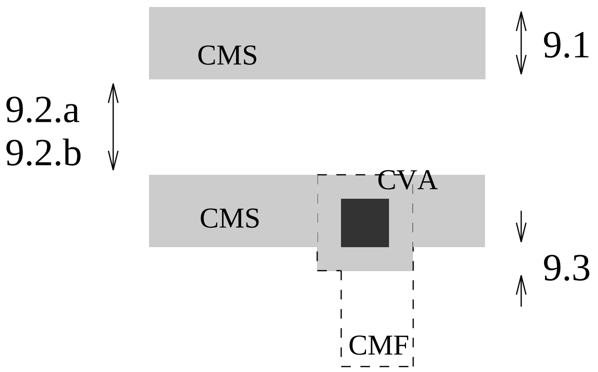
Via1 (CVA)

8.1	Exact size	2 × 2
8.2	Minimum via1 spacing	3
8.3	Minimum overlap by metal1	1
8.4	Minimum spacing to contact	2
8.5	Minimum spacing to poly or active edge	2



Metal2 (CMS)

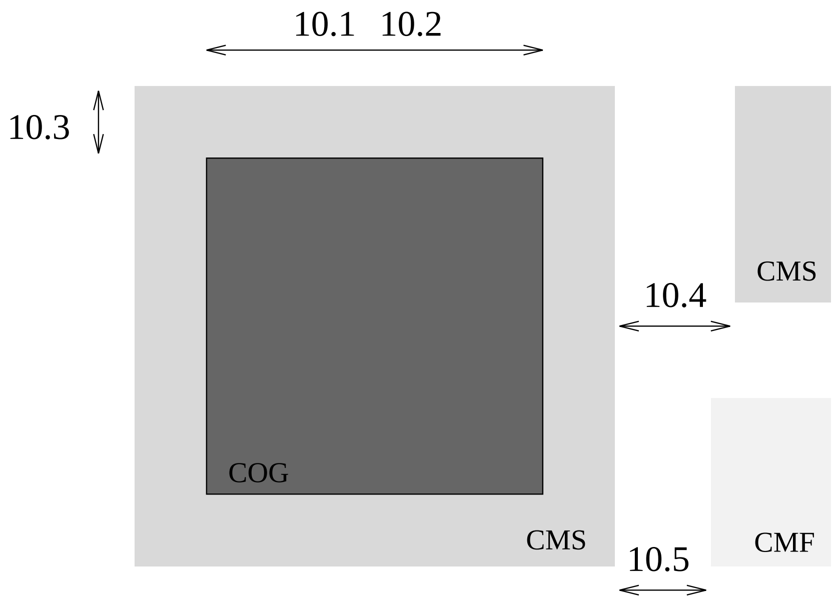
9.1	Minimum width	3
9.2.a	Minimum spacing	4
9.2.b[6]	Minimum tight metal spacing	3
9.3	Minimum overlap of via1	1



[6] Only allowed between minimum width wires, otherwise use regular spacing rule.

Overglass[7] (COG)

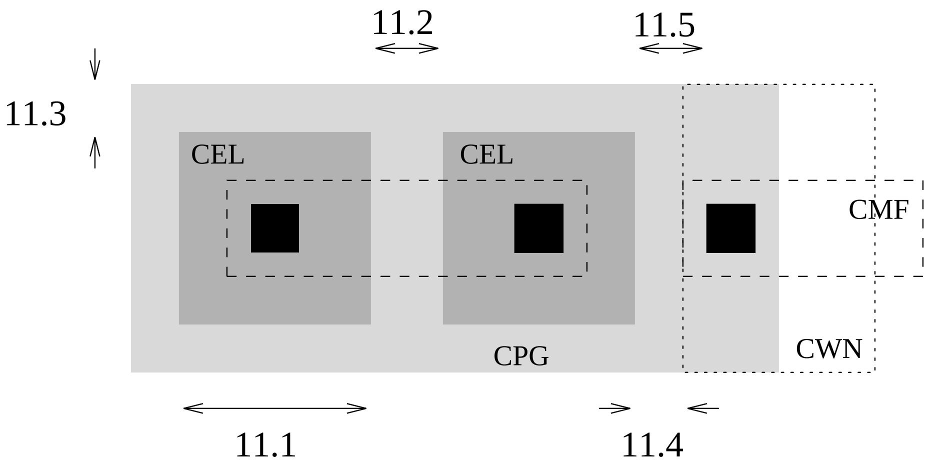
		μm
10.1	Minimum bonding pad width	100×100
10.2	Minimum probe pad width	75×75
10.3	Pad overlap of glass opening	6
10.4	Minimum pad spacing to unrelated metal2[8]	30
10.5	Minimum pad spacing to unrelated metal1, poly, electrode or active	15



[7]Rules in this section are in unit of μm.
[8]And metal3 if triple metal used.

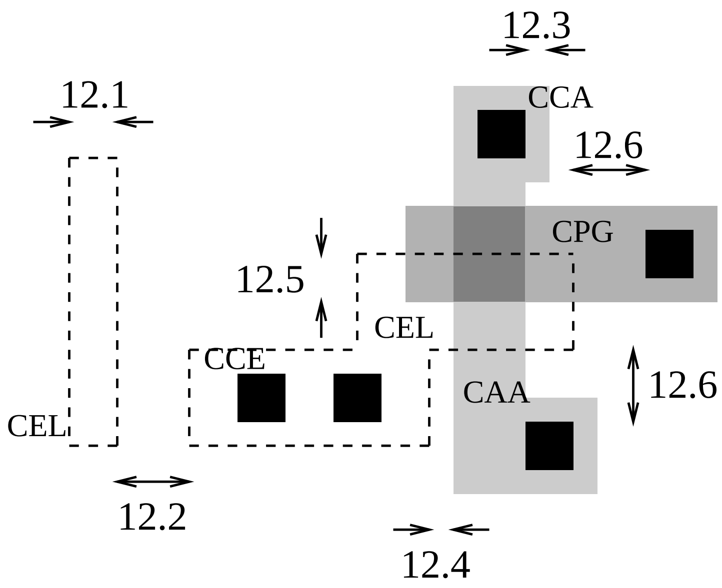
Electrode for Capacitor (CEL - Analog Option)

11.1	Minimum width	3
11.2	Minimum spacing	3
11.3	Minimum poly overlap	2
11.4	Minimum spacing to active or well edge	2
11.5	Minimum spacing to poly contact	3



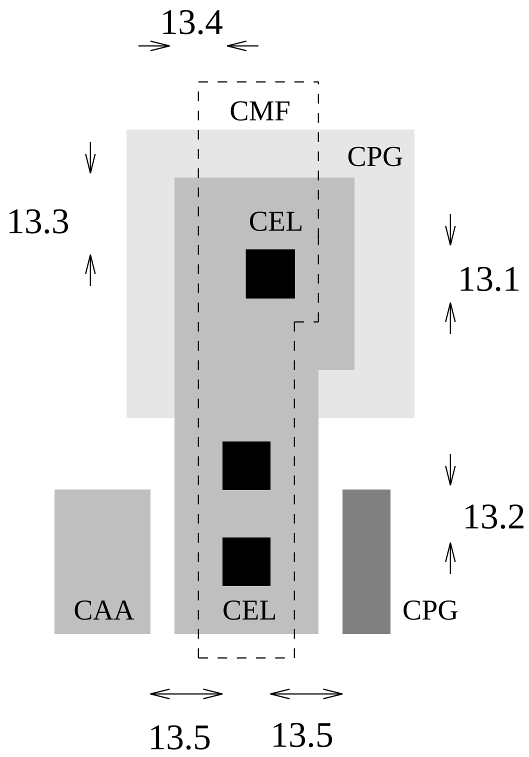
Electrode for Transistor (CEL - Analog Option)

12.1	Minimum width	2
12.2	Minimum spacing	3
12.3	Minimum electrode gate overlap of active	2
12.4	Minimum spacing to active	1
12.5	Minimum spacing or overlap of poly	2
12.6	Minimum spacing to poly or active contact	3



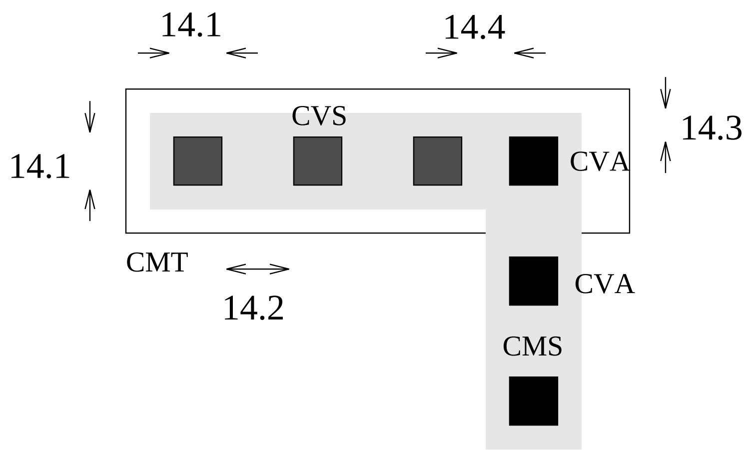
Electrode Contact (CCE - Analog Option)

13.1	Exact contact size	2×2
13.2	Minimum contact spacing	2
13.3	Minimum electrode overlap (on capacitor)	3
13.4	Minimum electrode overlap (not on capacitor)	2
13.5	Minimum spacing to poly or active	3



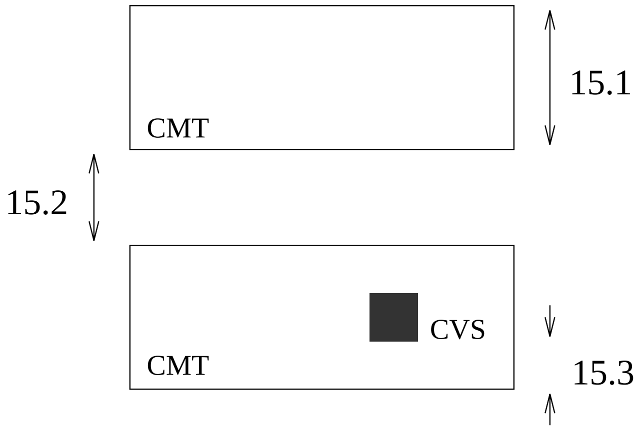
Via2 (CVS - Triple Metal Option)

14.1	Exact size	2×2
14.2	Minimum spacing	3
14.3	Minimum overlap by metal2	1
14.4	Minimum spacing to via1	2



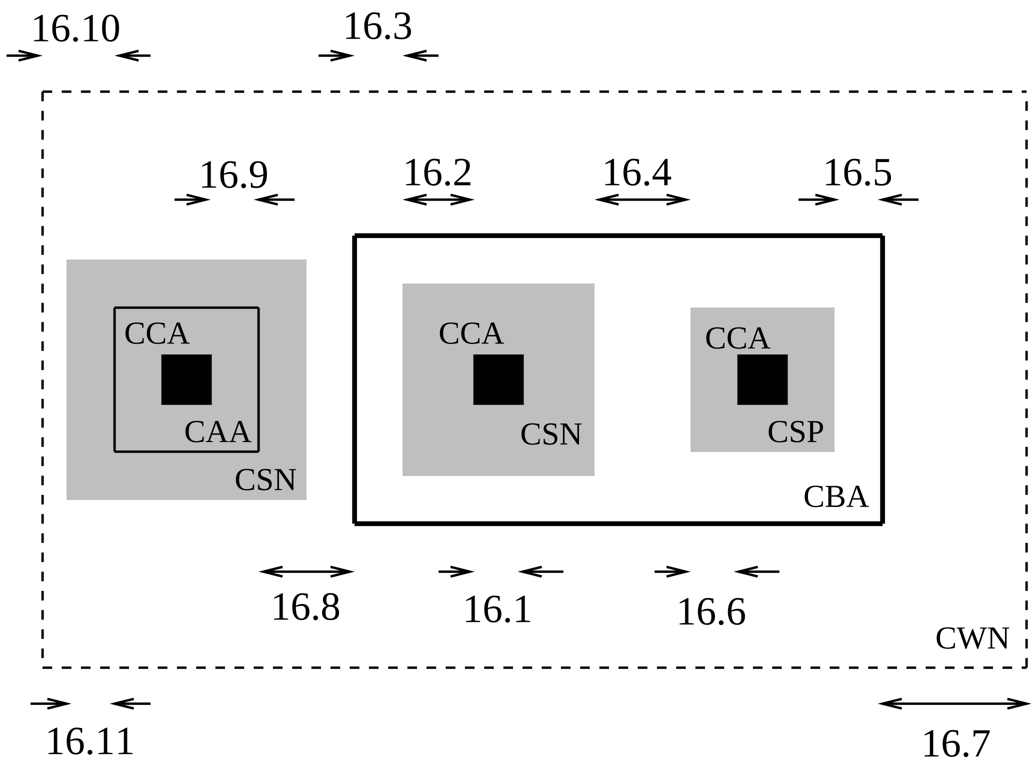
Metal3 (CMT - Triple Metal Option)

15.1	Minimum width	6
15.2	Minimum spacing to metal3	4
15.3	Minimum overlap of via2	2



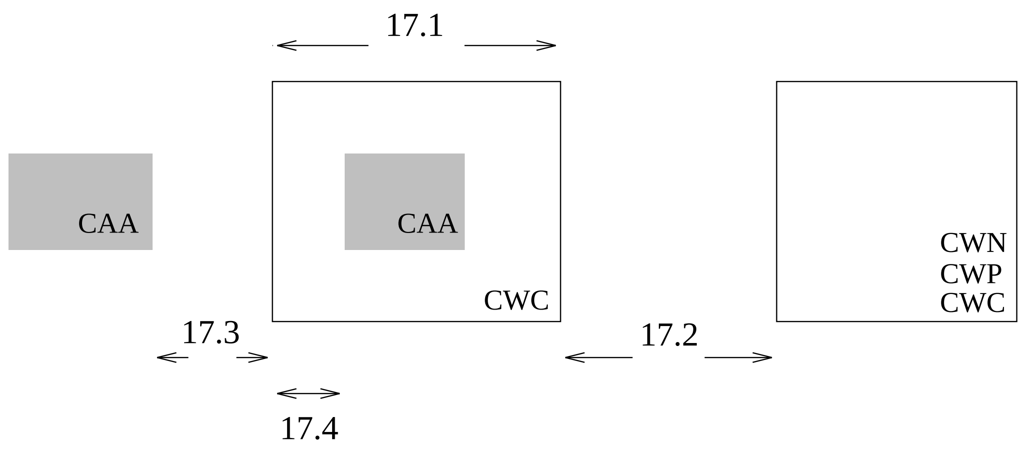
NPN Bipolar Transistor (CBA - Analog Option)

16.1	All active contact	2×2
16.2	Minimum select overlap of emitter contact	3
16.3	Minimum pbase overlap of emitter select	2
16.4	Minimum spacing between emitter select and base select	4
16.5	Minimum pbase overlap of base select	2
16.6	Minimum select overlap of base contact	2
16.7	Minimum nwell overlap of pbase	6
16.8	Minimum spacing between pbase and collector active	4
16.9	Minimum active overlap of collector contact	2
16.10	Minimum nwell overlap of collector active	3
16.11	Minimum select overlap of collector active	2



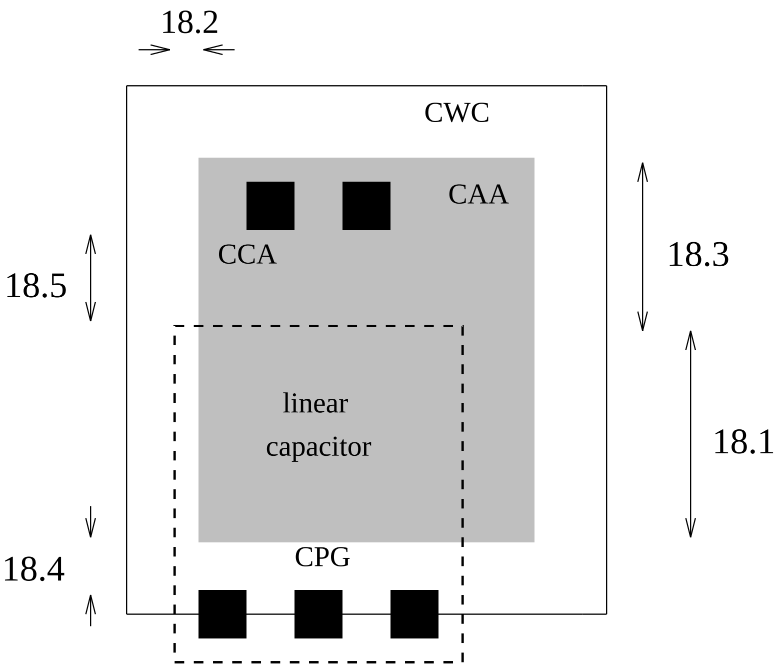
Capacitor Well (CWC - Linear Capacitor Option)

17.1	Minimum width	10
17.2	Minimum spacing	9
17.3	Minimum spacing to external active	5
17.4	Minimum overlap of active	3



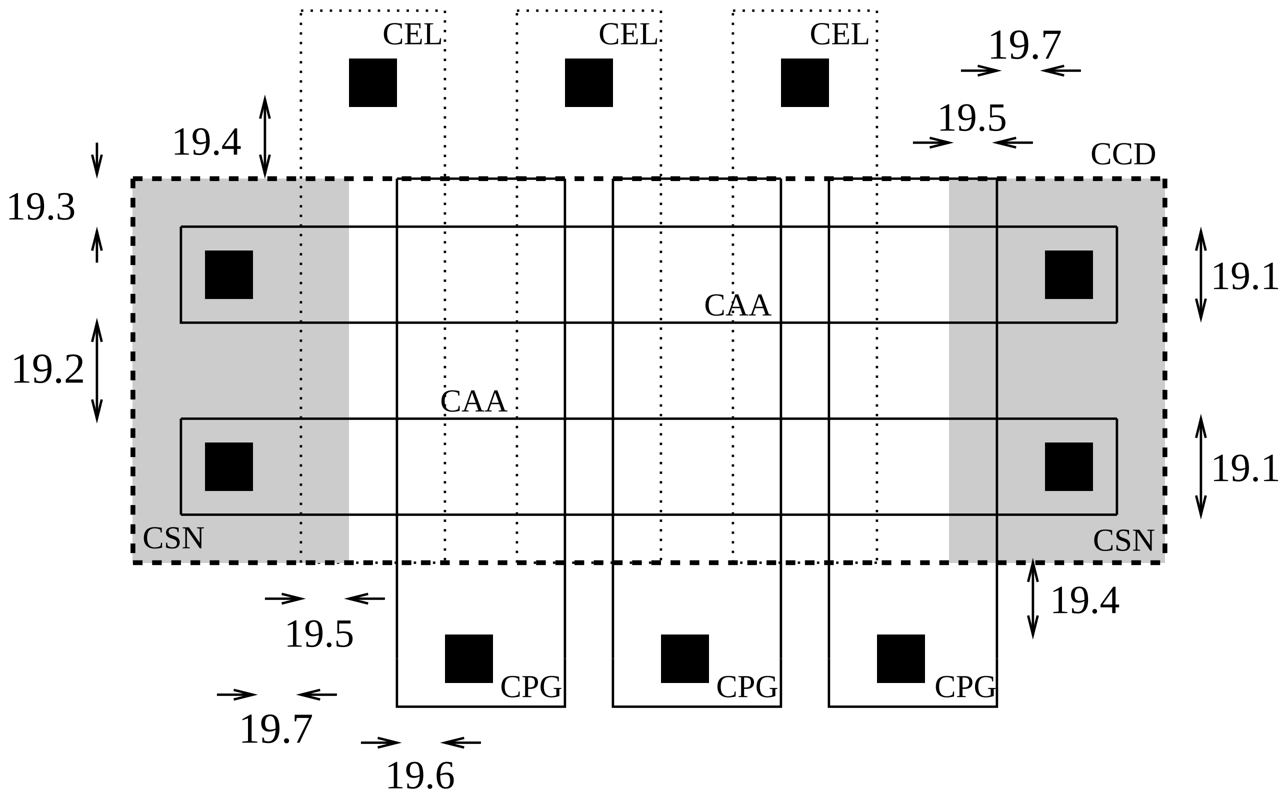
Linear Capacitor (Linear Capacitor Option)

18.1	Minimum width	3
18.2	Minimum poly extension of active	1
18.3	Minimum active overlap of poly	3
18.4	Minimum poly contact to active	2
18.5	Minimum active contact to poly	4



Buried Channel CCD (CCD - Analog Option[9])

19.1	Minimum CCD channel active width	4
19.2	Minimum CCD channel active spacing	4
19.3	Minimum CCD implant overlap of channel active	2
19.4	Minimum outside contact to CCD implant	3
19.5	Minimum select overlap of electrode (or poly)	2
19.6	Minimum poly/electrode overlap within channel active	2
19.7	Minimum contact to channel electrode (or poly)	2



[9]Not for all processes

References

[1] Cadence Design Systems, Inc./Calma. *GDSII Stream Format Manual*, Feb. 1987. Release 6.0, Documentation No.: B97E060.

[2] J. Marshall, M. Gaitan, M. Zaghloul, D. Novotny, V. Tyree, J.-I. Pi, C. Piñá, and W. Hansford. Realizing suspended structures on chips fabricated by CMOS foundry processes through the MOSIS service. Technical Report NISTIR-5402, National Institute of Standards and Technology, U.S. Department of Commerce, Gaithersburg, MD, 1994.

[3] C. Mead and L. Conway. *Introduction to VLSI Systems.* Addison-Wesley, 1980.

[4] N. H. E. Weste and K. Eshraghian. *Principles of CMOS VLSI Design: A System Perspective.* Addison-Wesley, 2nd. edition, 1993.