

$$\begin{aligned}
i_{p_i}(t) &= i_{R,pi}(v_{p_1}(t), \dots, v_{p_n}(t)) + \frac{d}{dt} Q_{C,pi}(v_{p_1}(t), \dots, v_{p_n}(t)) \\
&= i_{R,pi}(v_{p_1}(t), \dots, v_{p_n}(t)) + \sum_{j=1}^n \frac{\partial Q_{C,pi}}{\partial v_{p_j}} \frac{dv_{p_j}}{dt}
\end{aligned} \tag{6}$$

MCSM requires stamping of only two voltage-controlled elements per cell port in the circuit matrices. The resultant matrices are significantly smaller than those resulting from stamping all the transistors, diodes, and parasitic RCs that are part of the fully extracted cell. Consequently, MCSM simulation is much faster. For an inverter, our unoptimized MCSM simulator using table-lookup models takes  $\sim 400\mu\text{s}$  on a Pentium 4 3GHz machine (4GB RAM) running Linux. (A custom MCSM simulator is under active development.)

#### 4.5 Advantages of MCSMs

Existing cell characterization methodologies characterize gate input capacitances as functions of input waveforms and output loading [1]. During the delay calculation phase, any complex input waveform has to be approximated by a waveform for which the cell delay has been characterized. Moreover, complex interconnect loads and nonlinear receiver input capacitances have to be converted to one linear capacitance value,  $C_{eff}$  [2], which is used to look up gate delay from pre-characterized tables or equations. Both of these steps can introduce significant error. The  $C_{eff}$  techniques are known to introduce large error in slews at receiver inputs at the end of long  $RC/RLC$  interconnect. CSMs in general do not suffer from these drawbacks as they are simulation-based models. If speed is desired over accuracy, existing linear model order reduction techniques can be applied to reduce the linear interconnect and the resultant reduced interconnect model can be used with CSMs.

MCSM essentially inherits the desirable properties of all CSMs. These include the ability to model cross-capacitance effects, complex waveforms, noise, power-droop, etc. For example, power-droop effects may be captured by modeling Vcc and Vss pins as additional ports in MCSM. In this case,  $i_R$  and  $Q_C$  would be characterized as functions of voltages at Vcc, Vss, as well as logic pins. MCSM is also well suited for noise analysis tools as it can handle arbitrary input waveforms. For noise analysis, exact noise waveforms may be propagated from stage to stage using MCSMs.

### 5. RESULTS

We have characterized thousands of single-CCC cells (inverters, and multi-input nands, nors, and-or-invert, etc.) from a 65 nm static CMOS cell library with our MCSM model. In this section, we show the error of the MCSM model with respect to transistor-level circuit simulation for various timing analysis scenarios.

#### 5.1 Library-level MCSM accuracy studies

In this section, we present MCSM errors for cells loaded with linear capacitors. For our study, we performed 5000 cell-level simulations by applying an arbitrary input waveform(s) to a cell randomly picked from our library driving a load that varied within the typical characterization range (for the default delay models).

We begin by showing that the MCSM models are applicable to typical SIS delay calculation. We then show the error for MIS assumptions.

**Single-input switching (SIS):** Figure 5 shows that MCSM can easily capture SIS situations, even for a complex, noisy input. In this case, the MCSM and transistor-level output waveforms are almost identical. Figure 6 shows a histogram of SIS delay (50% of Vcc) and slew (20%-80% of Vcc) errors obtained with the MCSM model (transistor-level simulation is the reference). It is clear from the data that MCSM captures SIS situations well. Delay error is

within  $\pm 5\%$  for 97% of the samples. Moreover, only 0.4% of the samples have delay error larger than  $\pm 10\%$ . Slew error is within  $\pm 5\%$  for 99.6% of the samples. Most of the larger errors are due to switching patterns that cause the output to switch via a long stack of transistors when the cell is lightly loaded.

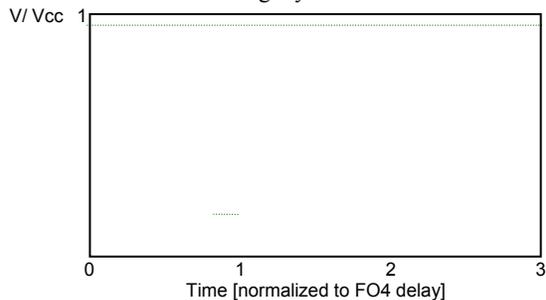


Figure 5. MCSM captures SIS well for a NAND2

Figure 6. SIS delay/slew errors with the MCSM model

**Multiple-input switching (MIS):** Figure 7 shows an illustrative example of MCSM's ability to capture MIS situations. We repeated the same experiment for MIS situations. In addition to varying the parameters in the SIS experiment, the input waveforms at all inputs to a cell and their relative offsets (50% of Vcc) were also generated randomly. Figure 8 shows the histogram of MIS delay and slew errors. The delay was calculated with respect to the latest (earliest) controlling input for MAX (MIN) analysis. Results indicate that MCSM also captures MIS situations well. Delay error is within  $\pm 5\%$  for 89.1% of the samples. Slew error is within  $\pm 5\%$  for 97.6% of the samples. Only 1.6% of the samples have delay error larger than  $\pm 10\%$ . Again, larger errors are associated with longer stacks.

Next, we demonstrate MCSM's application to a production level industrial design.

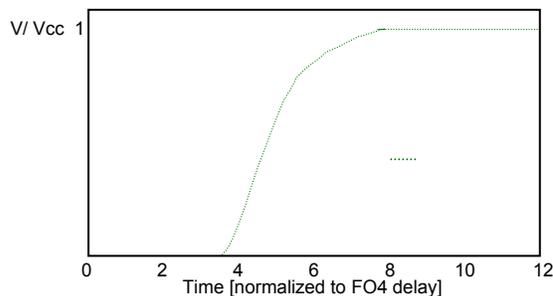


Figure 7. MCSM captures MIS well for a NAND2